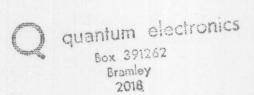




MECL DEVICE DATA

This book presents technical data for a broad line of MECL integrated circuits. Complete specifications for the individual circuits are provided in the form of data sheets. In addition, selector guides are included to simplify the task of choosing the best combination of circuits for optimum system architecture.

The information in this book has been carefully checked and is believed to be reliable; however, no responsibility is assumed for inaccuracies. Furthermore, this information does not convey to the purchaser of microelectronic devices any license under the patent right of any manufacturer.

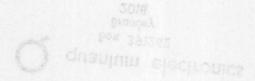


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Principal of Experiment (2007)

			editA		

SUPPLEMENTARY INFORMATION

AC parameters for the following 18 devices have been improved since this book was prepared for printing. These parameters should therefore be read in place of those printed in the main text of the book.

SUPERSEDES AC PARAMETERS LISTED IN DL122 REV 2, PAGE 2-10

	12				



MOTOROLA

M	C10H100		0 De	eg. C	+25 [Deg. C	+75 [Deg. C	
AC Parameters	Symbol	Pins	Min	Max	Min	Max	Min	Max	Units
Propagation Delay	tpd								
	t+-	9	0.75	1.60	0.80	1.50	0.90	1.70	ns
	t-+	9	0.60	1.60	0.65	1.50	0.70	1.70	ns
	t+-	All others	0.55	1.20	0.60	1.25	0.70	1.35	ns
	t-+	All others	0.40	1.15	0.40	1.15	0.50	1.20	ns
Rise & Fall Time	tr, tf								
	t+, t-	9	0.50	1.75	0.50	1.80	0.55	1.95	ns
	t+, t-	All others	0.60	1.45	0.65	1.50	0.70	1.60	ns

AC parameters for the following 18 devices have been improved since this book was prepared for printing. These parameters should therefore be read in these printed in the main text of the book.

M	C10H101		0 De	eg. C	+25 [Deg. C	+75 [Deg. C	
AC Parameters	Symbol	Pins	Min	Max	Min	Max	Min	Max	Units
Propagation Delay	tpd								
	t++	4,7,10,13	0.50	1.45	0.50	1.50	0.50	1.55	ns
	t	4,7,10,13	0.50	1.40	0.50	1.40	0.50	1.45	ns
	t+-	4,7,10,13	0.50	1.40	0.50	1.45	0.50	1.55	ns
	t-+	4,7,10,13	0.50	1.35	0.50	1.40	0.50	1.40	ns
	t++	12	0.50	1.60	0.50	1.50	0.50	1.70	ns
	t	12	0.50	1.60	0.50	1.50	0.50	1.70	ns
	t+-	12	0.50	1.50	0.50	1.50	0.50	1.70	ns
	t-+	12	0.50	1.50	0.50	1.50	0.50	1.55	ns
Rise & Fall Time	tr, tf								
	t+, t-	4,7,10,13	0.50	1.65	0.50	1.70	0.50	1.80	ns
	t+, t-	12	0.50	2.10	0.50	2.00	0.50	2.10	ns



o .oM	C10H102	9.0		0 D	0 Deg. C		+25 Deg. C		Deg. C	
AC Parameters	Symbo	ol x	Pins	Min	Max	Min	Max	Min	Max	Units
Propagation Delay	tpd							bq1	n Delay	pagatic
1.50 os	t++	1.80		0.40	1.20	0.50	1.25	0.45	1.40	ns
an 08.7	t-+	08.1		0.40	1.15	0.40	1.15	0.40	1.20	ns
	t++			0.40	1.25	0.50	1.25	0.55	1.35	ns
	t			0.40	1.25	0.40	1.15	0.40	1.25	ns
Rise & Fall Time	tr, tf	1.50		1.50	08.0			-1,+1		
	t+, t-			0.50	1.45	0.50	1.50	0.55	1.60	ns

	+75 Deg. C		+25 Deg. C		0 Deg. C			C10H105	MC		
Units	Max	Min	Max	Min	Max	Min	Pins	N SIN	Symbol	eters	AC Param
MISSEQ	VERSIA OF	1003							tpd	on Delay	Propagati
				4,8,14	0,40	03.1		1,40	0.45	1,40	an
				4.9.14	08.0	1.40		1.40		1.40	
ns	1.30	0.45	1.20	0.45	1.20	0.45		00.1	t+-	1.40	
ns	1.20	0.40	1.15	0.40	1.10	0.40		05.1	t-+	1.40	
ns	1.20	0.45	1.15	0.45	1.10	0.45		0,40	t++	1,40	
ns	1.15	0.40	1.05	0.40	1.05	0.40		ONE	t	1,40	
				8,7,6	0.45	OFLT		00.1		1,40	
				5,7,15	00,00	1.40		05.7	tr, tf	I Time	Rise & Fal
ns	1.50	0.50	1.40	0.50	1.40	0.50			t+, t-		

O MC	C10H106			0 D	eg. C	+25 [Deg. C	+75	Deg. C	
AC Parameters	Symbol	Max	Pins	Min	Max	Min	Max	Min	Max	Units
Propagation Delay	tpd							bqi	yaleQ n	pagadi
1.40 ns	t+-	125		0.55	1.25	0.55	1.50	0.65	1.50	ns
2.1 05.1	t-+	1.18		0.45	1.25	0.45	1.50	0.50	1.30	ns
en 26.1 1		1.18		ES. 1	09.0			++1		7-57
Rise & Fall Time	tr, tf	1.15		1.25	0.40			3		
	t+, t-			0.50	1.50	0.50	1.50	0.55	1.50	ns

M	C10H107			0 De	eg. C	+25 I	Deg. C	+75 [Deg. C	
AC Parameters	Symbol	10.75	Pins	Min	Max	Min	Max	Min	Max	Units
Propagation Delay	tpd							Service Service		
	t++		4,9,14	0.40	1.40	0.40	1.40	0.45	1.40	ns
	t		4,9,14	0.40	1.40	0.40	1.40	0.40	1.40	ns
1.30 ns	t+-	1.00	4,9,14	0.40	1.40	0.40	1.40	0.45	1.40	ns
an 05.1	t-+	1.1	4,9,14	0.40	1.40	0.40	1.40	0.40	1.40	ns
1.20 ns P	t++	1.1	5,7,15	0.55	1.40	0.60	1.40	0.65	1.40	ns
1 an 31.7	t	0.1	5,7,15	0.45	1.40	0.50	1.40	0.50	1.40	ns
	t+-		5,7,15	0.45	1.40	0.50	1.40	0.50	1.40	ns
	t-+		5,7,15	0.40	1.40	0.40	1.40	0.50	1.40	ns
Rise & Fall Time	tr, tf	1,40		08.0	08.0			-2,13		
	t+, t-			0.50	1.40	0.50	1.40	0.50	1.40	ns

O pa(MC10	H116		0 De	eg. C	+25 [Deg. C	+75 [Deg. C	
AC Parameters	s S	ymbol	Pins	Min	Max	Min	Max	Min	Max	Units
Propagation D	elay tr	bd					be	d lyele	G neitsp	Préps
	ar t	++100	4,9,12	0.45	1.05	0.45	1.05	0.45	1.05	ns
	08 g t	00.0	4,9,12	0.40	0.95	0.40	1.00	0.55	1.15	ns
	as t	+	4,9,12	0.40	1.00	0.45	1.05	0.45	1.10	ns
		-+20 +	4,9,12	0.40	0.90	0.40	1.00	0.40	1.10	ns
	t-	++	5,10,13	0.40	1.00	0.45	1.05	0.45	1.05	ns
	t-		5,10,13	0.40	0.95	0.40	1.00	0.50	1.15	ns
		+-	5,10,13	0.45	1.00	0.40	1.00	0.45	1.10	ns
	80.F.t	108.1	5,10,13	0.40	0.90	0.40	1.00	0.50	1.10	ns
Rise & Fall Tim	ne tr	, tf								
	t-	+, t-		0.50	1.15	0.50	1.20	0.50	1.25	ns

Mo	C10H117		0 De	eg. C	+25 [Deg. C	+75 C	eg. C	
AC Parameters	Symbol	Pins OK	Min	Max	Min	Max	Min .	Max	Units
Propagation Delay	tpd	88.0 08.1	08.0	07	bulan		3		
en 00 F 00	t++08.1	4,5,12,13	0.55	1.15	0.60	1.15	0.50	1.30	ns
.05 1.50 n	t	4,5,12,13	0.45	1.15	0.45	1.15	0.50	1.25	ns
85 1.70 n	t+-	4,5,12,13	0.60	1.25	0.65	1.25	0.60	1.35	' ns
95 1 40 1	t-+	4,5,12,13	0.50	1.20	0.50	1.20	0.55	1.25	ns
	t++	6,7,10,11	0.40	1.10	0.45	1.10	0.40	1.20	ns
	t	6,7,10,11	0.40	0.95	0.40	0.95	0.40	1.00	ns
	t+-	6,7,10,11	0.50	1.15	0.50	1.15	0.50	1.30	ns
70 1.70 no	t-+	6,7,10,11	0.40	1.05	0.40	1.10	0.40	1.15	ns
.BO 1.40 ns	t++	9 08.1	0.50	1.10	0.55	1.15	0.50	1.25	ns
	t	9	0.40	1.00	0.40	1.00	0.40	1.05	ns
	t+-	9	0.55	1.25	0.60	1.25	0.60	1.40	ns
	t-+	9	0.45	1.10	0.40	1.10	0.40	1.15	ns
Rise & Fall Time	tr, tf								
	t+, t-		0.50	1.35	0.50	1.35	0.50	1.40	ns

O gad oMC	C10H119	3 85+ 0.	0 De	g. C	+25 E	Deg. C	+75 [Deg. C	
AC Parameters	Symbol	Pins	Min	Max	Min	Max	Min	Max	Units
Propagation Delay	tpd					100	a yale	G nodsy	Propi
A5 1.05 ns	t++	1.05 010.45	1.00	2.15	1.05	2.25	1.15	2.35	ns
n ci.i 68.	t00.F	10	0.75	1.95	0.75	2.00	0.80	2.10	ns
an 0/4 - 24	t++70.1	xclud 10	1.00	1.95	1.10	2.00	1.25	2.15	ns
40 1.10 ns	0 t= _00.1	xclud 10	1.00	1.90	1.00	1.95	1.10	2.05	ns
Rise & Fall Time	tr, tf	0.95 9.40	0.40	Er es	5,10				
2 03	t+, t-		0.95	1.80	1.00	1.80	1.05	1.90	ns

IV	IC10H121	RAMETERS	0 De	eg. C	+25 [Deg. C	+75 [Deg. C	
AC Parameters	Symbol	Pins (13	Min	Max	Min	Max	Min	Max	Units
Propagation Delay	tpd								
	t++0 .99	xclud 10	0.65	1.70	0.75	1.70	0.70	1.80	ns
	tcslvt	xclud 10	0.70	1.70	0.75	1.80	0.80	1.80	ns
	t+-	xclud 10	0.80	1.50	0.65	1.50	0.70	1.85	ns
	t-+	xclud 10	0.55	1.50	0.60	1.60	0.70	1.70	ns
	t++	08.010	0.85	1.60	0.90	1.80	0.90	1.90	ns
	t	10	0.55	1.40	0.55	1.40	0.65	1.50	ns
	t+-35	10	0.75	1.60	0.80	1.60	0.85	1.70	ns
	1 1	10 00.0	0.45	1.30	0.45	1.30	0.55	1.40	ns
	01,1	1,10 0.45		11 11	6,7,1	1			
Rise & Fall Time	tr, tf	0.95 0.40		THE REAL	6,7,11				
	t+, t-	08.0 81.1 08.0 2 80.1	0.60	1.70	0.65	1.70	0.70	1.70	ns
	t+, t-	3	0.50	1.30	0.50	1.30	0.50	1.40	ns

o Mo	C10H123			0 D	eg. C	+25 I	Deg. C	+75 [Deg. C	
AC Parameters	Symbol	CLAVA-	Pins	Min	Max	Min	Max	Min	Max	Units
Propagation Delay	tpd					FREE		bqf	yeled no	itsgaq
3.20 ns	t+-	25		0.75	1.40	075	1.40	0.75	1.50	ns
20 08.5	t-+	2.00		0.70	1.50	0.75	1.50	0.80	1.60	ns
2.95 ns		2.10		2.65	00.1 0	1,51,01,12,1	3,5,	++1	15711 2	
Rise & Fall Time	tr, tf	2,00		2.70	BT.J.] #	1,10,12,1	3,5,	+-1		
3.10 ns	t+, t-	3.80		0.70	1.60	0.70	1.65	0.70	1.75	ns

Me	C10H124		0 D	eg. C	+25 [Deg. C	+75 [Deg. C	
AC Parameters	Symbol	Pins	Min	Max	Min	Max	Min	Max	Units
Propagation Delay	tpd								
	t++	6	0.75	1.50	0.75	1.65	0.85	1.65	ns
	t	6	0.70	1.70	0.75	2.05	1.15	2.90	ns
E 2-49	t++ SV	6	0.75	1.55	0.80	1.60	0.90	1.70	ns
	t-+	6	0.75	1.70	0.75	2.05	1.15	2.95	ns
Deg. C	t++	xclud 6	0.80	1.55	0.80	1.60	0.90	1.70	ns
	t	xclud 6	0.55	1.65	0.55	2.00	0.85	2.70	ns
Max Units	t+-	xclud 6	0.80	1.55	0.80	1.55	0.95	2.70	ns
	t-+	xclud 6	0.55	1.60	0.55	1.95	0.85	2.80	ns
Rise & Fall Time	tr, tf		1,90	08.0	7,8,14		4-93		
THIS CAT AN TIME	000		138.1	08.0	57,9,14			S. T. E.	
1.75 ns	t+, t-		0.50	1.30	0.50	1.30	0.50	1.35	ns

2 a Mo	C10H160	+25 Deg. C	0 De	g. C	+25 [Deg. C	+75 [Deg. C	
AC Parameters	Symbol	Pins	Min	Max	Min	Max	Min	Max	Units
Propagation Delay	tpd						bqt	on Delay	pagali
1.50 ps	t++	3,5,7,10,12,14	1.35	2.80	1.40	2.90	1.55	3.20	ns
en 06.1	t=0 0	3,5,7,10,12,14	1.25	2.60	1.30	2.60	1.55	2.80	ns
	t+-	3,5,7,10,12,14	1.40	2.65	1.45	2.70	1.70	2.95	ns
	t-+	3,5,7,10,12,14	1.15	2.70	1.20	2.80	1.35	3.00	ns
an at I	t++	4,6,9,11,13,15	1.10	2.90	1.10	3.00	1.25	3.10	ns
	t	4,6,9,11,13,15	1.15	2.45	1.20	2.50	1.45	2.65	ns
	t+-	4,6,9,11,13,15	1.10	2.50	1.15	2.50	1.35	2.60	ns
	t-+	4,6,9,11,13,15	1.05	2.65	1.10	2.70	1.25	2.90	ns
Rise & Fall Time	tr, tf								
	t+, t-		0.55	1.30	0.55	1.35	0.75	1.45	ns

SUPERSEDES AC PARAMETERS LISTED IN DL122 REV 2, PAGE 2-24

MC10H161			0 Deg. C		+25 Deg. C		+75 [Deg. C	
AC Parameters	Symbol	Pins	Min	Max	Min	Max	Min	Max	Units
Propagation Delay	tpd	1 88.0	08.7	0.50	8 bulos		+-3		
	t++	7,9,14	0.80	1.70	0.85	1.75	1.05	1.95	ns
	t	7,9,14	0.60	1.50	0.65	1.50	0.70	1.55	ns
an de t	t++ 0	7,9,14	0.75	1.55	0.80	1.65	1.00	1.75	ns
	t-+	7,9,14	0.70	1.50	0.75	1.55	0.85	1.60	ns
	t++	2,15	1.15	2.00	1.25	2.10	1.40	2.30	ns
	t	2,15	0.80	1.65	0.80	1.70	0.90	1.75	ns
Rise & Fall Time	tr, tf								
	t+, t-		0.55	1.35	0.55	1.40	0.60	1.50	ns

MC10H174			0 Deg. C		+25 [Deg. C	+75 Deg. C		
AC Parameters	Symbol	Pins	Min	Max	Min	Max	Min	Max	Units
Propagation Delay	tpd						ogt ve	eG noise	pagora
n 07.1 0	t+- 02.1	7,9	1.60	2.60	1.65	2.70	1.90	2.95	ns
88.1 0	t 68.1	7,9	1.15	2.25	1.20	2.30	1.30	2.45	ns
	t++	Xn,Yn	1.15	1.95	1.20	2.00	1.30	2.20	ns
	t	Xn,Yn	0.90	1.70	0.90	1.75	1.00	1.85	ns
	t+-	14	0.60	1.30	0.60	1.35	0.50	1.45	ns
6 2.20 ns	t-+	14	0.45	1.45	0.45	1.45	0.50	1.50	ns
Rise & Fall Time	tr, tf								
	t+,t-		0.50	1.30	0.50	1.35	0.50	1.45	ns

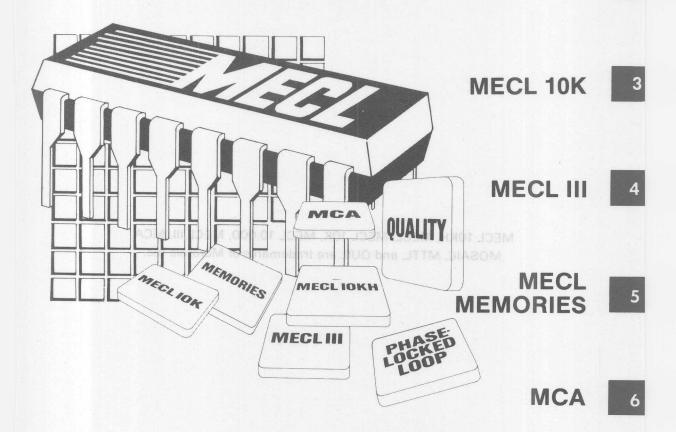
MC10H210			0 Deg. C		+25 Deg. C		+75 Deg. C			
AC Parameters	Symbol	Pins	Min	Max	Min	Max	Min	Max	Units	
Propagation Delay	tpd	90.7 500	1 68			1				
- en 00.5 t	t++		0.75	1.55	0.80	1.50	0.90	1.70	ns	
	t		0.50	1.55	0.55	1.55	0.60	1.55	ns	
Rise & Fall Time	tr, tf		00.		-11.8-5		+1			
sa lenz le	t+, t-		0.75	1.75	0.75	1.80	0.80	1.90	ns	

O god N	IC10H211		. 0	0 De	g. C	+25 [Deg. C	+75 [Deg. C	
AC Parameters	Symbol	Pins	xe?	Min	Max	Min	Max	Min	Max	Units
Propagation Delay	tpd							ay tps	ation De	Propag
	2.70 -+t.S		08.	0.80	1.60	0.85	1.50	1.00	1.70	ns
	2.30 +-t.3		25	0.75	1.60	0.75	1.50	0.80	1.65	ns
	2.00 1.30		36			Y,nX	1			
Rise & Fall Time	tr, tf		7.0			Y,nX		-1		
	t+, t-		30	0.95	1.95	0.90	2.00	0.95	2.20	ns

M	C10H423	AMETERS	0 De	g. C	+25 [Deg. C	+75 [Deg. C	
AC Parameters	Symbol	Pins	Min	Max	Min	Max	Min	Max	Units
Propagation Delay	tpd								
5 Deg. C	t+- 0 4	4-6,9-14	0.70	1.35	0.75	1.40	0.80	1.50	ns
ation! I wall s	int-+ xem	4-6,9-14	0.70	1.35	0.75	1.50	0.85	1.60	ns
	t+-	7	0.95	1.70	1.00	1.75	1.10	1.80	ns
0 1.70 ns	t-+	7 08.0 aa	0.95	1.75	1.00	1.90	1.10	2.00	ns
Rise & Fall Time	etr, tf 38.1	88.0 88		0			1		
	t+, t-	4-6,11-14	0.60	1.50	0.65	1.60	0.65	1.70	ns
	t+, t-	7	0.55	1.75	0.55	1.80	0.60	2.00	ns

GENERAL INFORMATION

MECL 10KH 2



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GENERAL

MECL 10KH

MECL 10K

MECLIII

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MEMORIES

MCA

PHASE-LOCKED LOOP

AND RELIABILITY

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MC10H103	
Wie Toll 100	Quad 2-Input "OR" Gate
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MC10H106	Triple 4-3-3 Input "NOR" Gate
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MC10H124	Quad TTL-to-MECL Translator
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MC10H130	
MC10H131	Dual Latch
MC10H135	
	Dual J-K Master-Slave Flip-Flop
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MC10H141	Four-Bit Universal Shift Register
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MC10115 0 3 - 10 VS 3 -) y/k MC10116 MC10117 MC10118 MC10119	Triple Line Receiver Dual 2-Wide 2-3-Input Dual 2-Wide 3-Input "C	"OR-AND/OR-AND-INVER OR-AND" Gate OR-AND" Gate	
MC10121 MC10123 MC10124 MC10125 MC10128	Triple 4-3-3-Input Bus I Quad TTL to MECL Tran Quad MECL to TTL Tran Bus Driver	AND-INVERT" Gate	
MC10129 MC10130 MC10131 MC10132 MC10133	Dual Latch Dual Type D Master-Sla Dual Multiplexer with L Quad Latch	ave Flip-Flop	
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NOUNE IS -- OPERATING TEMPERATURE RANGE

GENERAL INFORMATION SECTION 1 — HIGH-SPEED LOGICS

High speed logic is used whenever improved system performance would increase a product's market value. For a given system design, high-speed logic is the most direct way to improve system performance and emitter-coupled logic (ECL) is today's fastest form of digital logic. Emitter-coupled logic offers both the logic speed and logic features to meet the market demands for higher performance systems.

MECL PRODUCTS

Motorola introduced the original monolithic emittercoupled logic family with MECL I (1962) and followed this with MECL II (1966). These two families are now obsolete and have given way to the MECL III (MC1600 series), MECL 10K, PLL (MC12000 series) and the new MECL 10KH families.

Chronologically the third family introduced, MECL III (1968) is a higher power, higher speed logic. Typical 1 ns edge speeds and propagation delays along with greater than 500 MHz flip-flop toggle rates, make MECL III useful for high-speed test and communications equipment. Also, this family is used in the high-speed sections and critical timing delays of larger systems. For more general purpose applications, however, trends in large high-speed systems showed the need for an easy-to-use logic family with propagation delays on the order of 2 ns. To match this requirement, the MECL 10,000 Series was introduced in 1971.

An important feature of MECL 10K is its compatibility with MECL III to facilitate using both families in the same system. A second important feature is its significant power economy — MECL 10K gates use less than one-half the power of MECL III. Finally, low gate power and advanced circuit design techniques have permitted a new level of complexity for MECL 10K circuits. For example, the complexity of the MC10901 8X8-Bit Multiplier Function compares favorably to that of any bipolar integrated circuit on the market.

Motorola introduced the MECL 10KH product family in 1981. This latest MECL family features 100% improvements in propagation delay and clock speeds while maintaining power supply currents equal to MECL 10K. MECL 10KH is voltage compensated allowing guaranteed dc and switching parameters over a $\pm\,5\%$ power supply range. Noise margins have been improved by 75% over the MECL 10K series.

Compatibility with MECL 10K and MECL III is a key element in allowing users to enhance existing systems by increasing the speed in critical timing areas. Also, many MECL 10KH devices are pin out/functional duplications of the MECL 10K series devices. The emphasis of this new family will be placed on more powerful logic functions having more complexity and greater performance. With 1.0 ns propagation delays and 25 mW per gate, MECL 10KH features the best speed-power product of any ECL logic family available today.

MECL FAMILY COMPARISONS

		MEC	L 10K	
Feature	MECL 10KH	10,100 Series 10,500 Series	10,200 Series 10,600 Series	MECL III
Gate Propagation Delay	1.0 ns	2 ns	1.5 ns	1 ns
2. Output Edge Speed	1.5 ns	3.5 ns	2.5 ns	1 ns
3. Flip-Flop Toggle Speed	250 MHz min	125 MHz min	200 MHz min	300-500 MHz min
4. Gate Power	25 mW	25 mW	25 mW	60 mW
5. Speed Power Product	25 pJ	50 pJ	37 pJ	60 pJ

FIGURE 1a — GENERAL CHARACTERISTICS

Ambient Temperature Range	MECL 10KH	MECL 10K	MECL III	PLL
0° to 75°C	MC10H100 Series		MC1697P	MC12000 Series
-30°C to +85°C		MC10100 Series MC10200 Series	MC1600 Series	MC12000 Series
−55°C to 125°C	-	MC10500 Series MC10600 Series MCM10500 Series	MC1648M	MC12500 Series

FIGURE 1b — OPERATING TEMPERATURE RANGE

MECL IN PERSPECTIVE

In evaluating any logic line, speed and power requirements are the obvious primary considerations. Figure 1 provides the basic parameters of the MECL 10KH, MECL 10K, and MECL III families. But these provide only the start of any comparative analysis, as there are a number of other important features that make MECL highly desirable for system implementation. Among these:

Complementary Outputs cause a function and its complement to appear simultaneously at the device outputs, without the use of external inverters. It reduces package count by eliminating the need for associated invert functions and, at the same time, cuts system power requirements and reduces timing differential problems arising from the time delays introduced by inverters.

High Input Impedance and Low Output Impedance permit large fan out and versatile drive characteristics.

Insignificant Power Supply Noise Generation, due to differential amplifier design which eliminates current spikes even during signal transition period.

Nearly Constant Power Supply Current Drain simplifies power-supply design and reduces costs.

Low Cross-Talk due to low-current switching in signal path and small (typically 850 mV) voltage swing, and to relatively long rise and fall times.

Wide Variety of Functions, including complex functions facilitated by low power dissipation (particularly in MECL 10KH and MECL 10K series). A basic MECL 10K gate consumes less than 8 mW in on-chip power in some complex functions.

Wide Performance Flexibility due to differential amplifier design which permits MECL circuits to be used as linear as well as digital circuits.

Transmission Line Drive Capability is afforded by the open emitter outputs of MECL devices. No "Line Drivers" are listed in MECL families, because *every* device is a line driver.

Wire-ORing reduces the number of logic devices required in a design by producing additional OR gate functions with only an interconnection.

Twisted Pair Drive Capability permits MECL circuits to drive twisted-pair transmission lines as long as 1000 feet.

Wire-Wrap Capability is possible with MECL 10KH and the MECL 10K family because of the slow rise and fall time characteristic of the circuits.

Open Emitter-Follower Outputs are used for MECL outputs to simplify signal line drive. The outputs match any line impedance and the absence of internal pulldown resistors saves power.

Input Pulldown Resistors of approximately 50 k Ω permit unused inputs to remain unconnected for easier circuit board layout.

MECL APPLICATIONS

Motorola's MECL product lines are designed for a wide range of systems needs. Within the computer market, MECL 10K is used in systems ranging from special purpose peripheral controllers to large mainframe computers. Big growth areas in this market include disk and communication channel controllers for larger systems and high performance minicomputers.

The industrial market primarily uses MECL for high performance test systems such as IC or PC board testers.

However, the high bandwidths of MECL 10KH, MECL 10K, MECL III, and MC12,000 are required for many frequency synthesizer systems using high speed phase lock loop networks. MECL will continue to grow in the industrial market through complex medical electronic products and high performance process control systems.

MECL 10K and MECL III have been accepted within the Federal market for numerous signal processors and navigation systems. Full military temperature range MECL 10K is offered in the MC10500 and MC10600 Series, and in the PLL family as the MC12500 Series.

BASIC CONSIDERATIONS FOR HIGH-SPEED LOGIC DESIGN

High-speed operation involves only four considerations that differ significantly from operation at low and medium speeds:

- 1. Time delays through interconnect wiring, which may have been ignored in medium-speed systems, become highly important at state-of-the-art speeds.
- 2. The possibility of distorted waveforms due to reflections on signal lines increases with edge speed.
- 3. The possibility of "crosstalk" between adjacent signal leads is proportionately increased in high-speed systems.
- 4. Electrical noise generation and pick-up are more detrimental at higher speeds.

In general, these four characteristics are speed- and frequency-dependent, and are virtually independent of the type of logic employed. The merit of a particular logic family is measured by how well it compensates for these deleterious effects in system applications.

The interconnect-wiring time delays can be reduced only by reducing the length of the interconnecting lines. At logic speeds of two nanoseconds, an equivalent "gate delay" is introduced by every foot of interconnecting wiring. Obviously, for functions interconnected within a single monolithic chip, the time delays of signals travelling from one function to another are insignificant. But for a great many externally interconnected parts, this can soon add up to an appreciable delay time. Hence, the greater the number of functions per chip, the higher the system speed. MECL circuits, particularly those of the MECL 10K and MECL 10KH Series are designed with a propensity toward complex functions to enhance overall system speed.

Waveform distortion due to line reflections also becomes troublesome principally at state-of-the-art speeds. At slow and medium speeds, reflections on interconnecting lines are not usually a serious problem. At higher speeds, however, line lengths can approach the wavelength of the signal and improperly terminated lines can result in reflections that will cause false triggering (see Figure 2). The solution, as in RF technology, is to employ "transmission-line" practices and properly terminate each signal line with its characteristic impedance at the end of its run. The low-impedance, emitter-follower outputs of MECL circuits facilitate transmission-line practices without upsetting the voltage levels of the system.

The increased affinity for crosstalk in high-speed circuits is the result of very steep leading and trailing edges (fast rise and fall times) of the high-speed signal. These steep wavefronts are rich in harmonics that couple readily to adjacent circuits. In the design of MECL 10K and

MECL 10KH, the rise and fall times have been deliberately slowed. This reduces the affinity for crosstalk without compromising other important performance parameters.

From the above, it is evident that the MECL logic line is not simply capable of operating at high speed, but has been specifically designed to reduce the problems that are normally associated with high-speed operation.

TRANSMISSION LINE

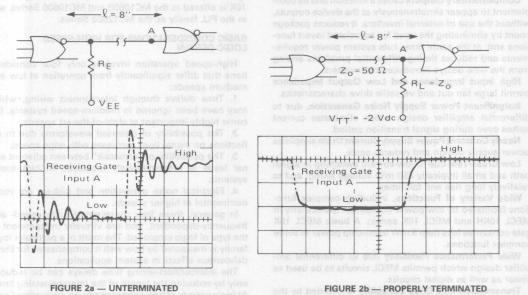
(No Ground Plane Used)

CIRCUIT DESCRIPTION

The typical MECL 10K circuit, Figure 3, consists of a differential-amplifier input circuit, a temperature and voltage compensated bias network, and emitter-follower outputs to restore dc levels and provide buffering for transmission line driving. High fan-out operation is possible be-

TRANSMISSION LINE

(Ground Plane Added)



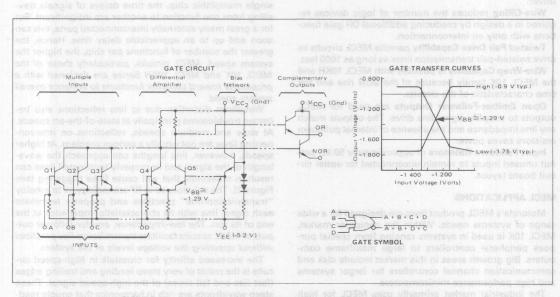


FIGURE 3 — MECL 10K GATE STRUCTURE AND SWITCHING BEHAVIOR

follower outputs. Power-supply noise is virtually eliminated by the nearly constant current drain of the differential amplifier, even during the transition period. Basic gate design provides for simultaneous output of both the OR function and its complement, the NOR function. The design of the MECL 10KH gate is unchanged, with two exceptions. The bias network has been replaced with a voltage regulator, and the differential amplifier source resistor has been replaced with a constant current source. (See section 2 for additional MECL 10KH information.)

Power-Supply Connections — Any of the power supply levels, V_{TT} , V_{CC} , or V_{EE} may be used as ground; however, the use of the V_{CC} node as ground results in best noise immunity. In such a case: $V_{CC} = 0$, $V_{TT} = -2.0 \text{ V}$, $V_{EF} = -5.2 \text{ V}$.

System Logic Specifications — The output logic swing of 0.85 V, as shown by the typical transfer characteristics curve, varies from a LOW state of $V_{OL} = -1.75$ V to a HIGH state of $V_{OH} = -0.9$ V with respect to ground.

Positive logic is used when reference is made to logical "0's" or "1's." Then

$$"0" = -1.75 \text{ V} = \text{LOW}$$
 typical $"1" = -0.9 \text{ V} = \text{HIGH}$

output when measuring the output HIGH level

voltage.

Circuit Operation — Beginning with all logic inputs LOW (nominal -1.75 V), assume that $\Omega1$ through $\Omega4$ are cut off because their P-N base-emitter junctions are not

Current:

by the VBB network, its emitter will be one diode drop (0.8 V) more negative than its base, or -2.09 V. (The 0.8 V differential is a characteristic of this P-N junction.) The base-to-emitter differential across $\Omega 1 - Q4$ is then the difference between the common emitter voltage (-2.09 V) and the LOW logic level (-1.75 V) or 0.34 V. This is less than the threshold voltage of $\Omega 1$ through Q4 so that these transistors will remain cut off.

When any one (or all) of the logic inputs are shifted upward from the -1.75 V LOW state to the -0.9 V HIGH state, the base voltage of that transistor increases beyond the threshold point and the transistor turns on. When this happens, the voltage at the common-emitter point rises from -2.09 V to -1.7 (one diode drop below the -0.9 V base voltage of the input transistor), and since the base voltage of the fixed-bias transistor (Q5) is held at -1.29 V, the base-emitter voltage Q5 cannot sustain conduction. Hence, this transistor is cut off.

This action is reversible, so that when the input signal(s) return to the LOW state, Q1 – Q4 are again turned off and Q5 again becomes forward biased. The collector voltages resulting from the switching action of Q1 – Q4 and Q5 are transferred through the output emitter-follower to the output terminal. Note that the differential action of the switching transistors (one section being off when the other is on) furnishes simultaneous complementary signals at the output. This action also maintains constant power supply current drain.

HIGH level output current: the current flowing

DEFINITIONS OF LETTER SYMBOLS AND ABBREVIATIONS

HO

Icc	Total power supply current drawn from the positive supply by a MECL unit under test.		into the output, at a specified HIGH level output voltage.
Ісво	Leakage current from input transistor on MECL devices without pulldown resistors when test voltage is applied.	IOL	LOW level output current: the current flowing into the output, at a specified LOW level output voltage.
ICCH	Current drain from V _{CC} power supply with all	los	Output short circuit current.
	inputs at logic HIGH level.	lout	Output current (from a device or circuit, under
ICCL	Current drain from V _{CC} power supply with all	.aneitiano	such conditions mentioned in context).
	inputs at logic LOW level.	IR	Reverse current drawn from a transistor input of a test unit when VFF is applied at that input.
IE .	Total power supply current drawn from a MECL test unit by the negative power supply.	Isc	Short-circuit current drawn from a translator
l _F	Forward diode current drawn from an input	Judino a	saturating output when that output is at
	of a saturated logic-to-MECL translator when		ground potential. Hangou man O AHOV
	that input is at ground potential.	Voltage:	
lin	Current into the input of the test unit when a maximum logic HIGH (VIH max) is applied at	V _{BB}	Reference bias supply voltage.
	that input.	VBE	Base-to-emitter voltage drop of a transistor
INH	HIGH level input current into a node with a		at specified collector and base currents.
HALL	specified HIGH level (VIH max) logic voltage	VCB	Collector-to-base voltage drop of a transistor
	applied to that node. (Same as I _{in} for positive	egettov sr	at specified collector and base currents.
	logic.) our ama qui se belas etto	VCC	General term for the most positive power sup-
INL	LOW level input current, into a node with a		ply voltage to a MECL device (usually ground, except for translator and interface circuits).
	specified LOW level (V _{IL min}) logic voltage applied to that node.	V _{CC1}	Most positive power supply voltage (output
h	Load current that is drawn from a MECL circuit	• 661	devices). (Usually ground for MECL devices.)
.L	Load darron that is drawn non a will cold that		da menseme dans proposed umbustativas. VISA

Voltage (cont.): Most positive power supply voltage (current VCC2 switches and bias driver). (Usually ground for MECL devices.) Most negative power supply voltage for a cir-VEE cuit (usually -5.2 V for MECL devices). VF Input voltage for measuring IF on TTL interface circuits. Input logic HIGH voltage level (nominal value). VIH Maximum HIGH level input voltage: The most VIH max positive (least negative) value of high-level input voltage, for which operation of the logic element within specification limits is guaranteed. Input logic HIGH threshold voltage level. VIHA VIHA min Minimum input logic HIGH level (threshold) voltage for which performance is specified. VIH min Minimum HIGH level input voltage: The least positive (most negative) value of HIGH level input voltage for which operation of the logic element within specification limits is guaranteed. V_{IL} Input logic LOW voltage level (nominal value). VIL max Maximum LOW level input voltage: The most positive (least negative) value of LOW level input voltage for which operation of the logic element within specification limits is quaranteed. Input logic LOW threshold voltage level. VIIA VILA max Maximum input logic LOW level (threshold) voltage for which performance is specified. Minimum LOW level input voltage: The least VIL min positive (most negative) value of LOW level input voltage for which operation of the logic element within specification limits is guaranteed. Input voltage (to a circuit or device). Vin Maximum (most positive) supply voltage, permitted under a specified set of conditions. VOH Output logic HIGH voltage level: The voltage level at an output terminal for a specified output current, with the specified conditions applied to establish a HIGH level at the output. Output logic HIGH threshold voltage level. VOHA VOHA min Minimum output HIGH threshold voltage level for which performance is specified. Maximum output HIGH or high-level voltage VOH max for given inputs. Minimum output HIGH or high-level voltage VOH min for given inputs. Output logic LOW voltage level: The voltage VOL level at the output terminal for a specified output current, with the specified conditions applied to establish a LOW level at the output. Output logic LOW threshold voltage level. VOLA VOLA max Maximum output LOW threshold voltage level for which performance is specified.

VOL max Maximum output LOW level voltage for given inputs. Accominanted walleds bigs regal with Minimum output LOW level voltage for given VOL min inputs. Insure instance when entitle betar Line load-resistor terminating voltage for outputs from a MECL device. VOLS1 Output logic LOW level on MECL 10,000 line receiver devices with all inputs at VFF voltage Output logic LOW level on MECL 10,000 line VOLS2 receiver devices with all inputs open. Time Parameters: Waveform rise time (LOW to HIGH), 10% to t+ on at 90%, or 20% to 80%, as specified. Waveform fall time (HIGH to LOW), 90% to t-10%, or 80% to 20%, as specified. Same as t+ Same as t-may war o - = HOV to stars NOTE tf Rosen t +s+solor Propagation Delay, see Figure 9. Propagation Delay, see Figure 9. Propagation delay, input to output from the tnd 50% point of the input waveform at pin × (falling edge noted by - or rising edge noted by +) to the 50% point of the output waveform at pin y (falling edge noted by - or rising edge noted by +). (Cf Figure 9.) Output waveform rise time as measured from 10% to 90% or 20% to 80% points on waveform (whichever is specified) at pin x with input conditions as specified. Output waveform fall time as measured from 90% to 10% or 80% to 20% points on waveform (whichever is specified) at pin x, with input conditions as specified. Toggle frequency of a flip-flop or counter fTog device. Shift rate for a shift register. fshift

Read Mode (Memories)

Chip Select Access Time **tACS** tRCS. Chip Select Recovery Time Address Access Time tAA

Write Mode (Memories)

Write Pulse Width Data Setup Time Prior to Write tWSD Data Hold Time After Write **tWHD** Address setup time prior to write tWSA Address hold time after write tWHA Chip select setup time prior to write twscs Chip select hold time after write twHCS. Write disable time tws Write recovery time tWR

Temper	ature: ATAG (AOMAG)
T _{stg}	Maximum temperature at which device may be stored without damage or performance degradation.
TJ	Junction (or die) temperature of an integrated circuit device.
TA	Ambient (environment) temperature existing in the immediate vicinity of an integrated cir- cuit device package.
θ JA	Thermal resistance of an IC package, junction to ambient.
θJC	Thermal resistance of an IC package, junction to case.
Ifpm	Linear feet per minute.
θ CA	Thermal resistance of an IC package, case to

ambient.

Miscellaneous:

eg	Signal generator inputs to a test circuit.
TPin	Test point at input of unit under test.
TPout	Test point at output of unit under test.
D.U.T.	Device under test.
Cin	Input capacitance.
Cout	Output capacitance.
Zout	Output impedance.
PD	The total dc power applied to a device, not including any power delivered from the device to a load.
RL	Load Resistance.
RT	Terminating (load) resistor.
Rp	An input pull-down resistor (i.e., connected to the most negative voltage).
P.U.T.	Pin under test.

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MECL FOR		

SECTION II — TECHNICAL DATA

GENERAL CHARACTERISTICS AND SPECIFICATIONS

(See pages 1-5 through 1-7 for definitions of symbols and abbreviations.)

In subsequent sections of this Data Book, the important MECL parameters are identified and characterized, and complete data provided for each of the functions. To make this data as useful as possible, and to avoid a great deal of repetition, the data that is common to all functional blocks in a line is not repeated on each individual sheet. Rather, these common characteristics, as well as the application information that applies to each family, are discussed in this section.

In general, the common characteristics of major importance are:

Maximum Ratings, including both dc and ac characteristics and temperature limits;

Transfer Characteristics, which define logic levels and switching thresholds;

DC Parameters, such as output levels, threshold levels, and forcing functions.

AC Parameters, such as propagation delays, rise and fall times and other time dependent characteristics.

In addition, this section will discuss general layout and design guides that will help the designer in building and testing systems with MECL circuits.

LETTER SYMBOLS AND ABBREVIATIONS

Throughout this section, and in the subsequent data sheets, letter symbols and abbreviations will be used in discussing electrical characteristics and specifications. The symbols used in this book, and their definitions, are listed on the preceding pages.

MAXIMUM RATINGS

The limit parameters beyond which the life of the devices may be impaired are given in Figure 4a. In addition, Table 4b provides certain limits which, if exceeded, will not damage the devices, but could degrade the performance below that of the guaranteed specifications.

FIGURE 4a — LIMITS BEYOND WHICH DEVICE LIFE MAY BE IMPAIRED

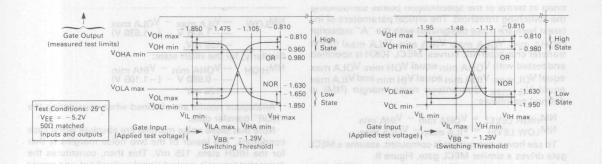
Characteristic	Symbol	Unit	MECL 10KH	MECL 10K	MECL III
Power Supply	VEE	Vdc	-8.0 to 0	-8.0 to 0	-8.0 to 0
Input Voltage (V _{CC} = 0)	Vin	Vdc	0 to VEE	0 to VEE	0 to VEE
Output Source Current Continuous	lout	mAdc	50	50	40
Output Source Current Surge	lout	mAdc	100	100	
Storage Temperature	T _{stg}	°C	- 55 to + 150	-55 to +150	- 55 to + 150
Junction Temperature Ceramic Package ①	TJ	°C	165	165	165②
Junction Temperature Plastic Package ③	TJ	°C	140	140	140

- NOTES: 1. Maximum T_J may be exceeded (≤ 250°C) for short periods of time (≤ 240 hours) without significant reduction in device life.
 - 2. Except MC1666 MC1670 which have maximum junction temperatures = 145°C.
 - 3. For long term (≥ 10 yrs.) max T_J of 110°C required. Max T_J may be exceeded (≤ 175°C) for short periods of time (≤ 240 hours) without significant reduction in device life.

FIGURE 4b — LIMITS BEYOND WHICH PERFORMANCE MAY BE DEGRADED

Characteristics	Symbol	Unit	MECL 10KH	MECL 10K	MECL III
Operating Temperature Range Commercial ①	ТА	°C	0 to +75	-30 to +85	-30 to +85
Operating Temperature Range MIL ①	TA	°C		-55 to +125	-55 to +125 (MC1648M)
Supply Voltage (V _{CC} = 0)	VEE	Vdc	-4.94 to -5.46 ⑤	-4.68 to -5.72 ②	-4.68 to -5.72 ²
Supply Voltage (V _{CC} = 0)	VTT	Vdc			
Output Drive Commercial	_	Ω	50 Ω to -2.0 Vdc	50 Ω to -2.0 Vdc	50 Ω to -2.0 Vdc4
Output Drive MIL		Ω		100 Ω to -2.0 Vdc	_
Maximum Clock Input Rise and Fall Time (20% to 80%)	t _r , t _f	ns	-	-	3

- NOTES: 1. With airflow ≥ 500 lfpm.
 - 2. Functionality only. Data sheet limits are specified for $-5.2 \text{ V} \pm 0.010 \text{ V}$.
 - 3. 10 ns maximum limit for MC1690, MC1697, and MC1699.
 - 4. Except MC1648 which has an internal output pulldown resistor.
 - 5. Functional and Data sheet limits.



MECL TRANSFER CURVES

For MECL logic gates, the dual (complementary) outputs must be represented by two transfer curves: one to describe the OR switching action and one to describe the NOR switching action. Typical transfer curves and associated data for the MECL 10K/10KH family are shown in Figure 5.a and 5.b respectively.

It is not necessary to measure transfer curves at all points of the curves. To guarantee correct operation it is sufficient merely to measure two sets of min/max logic level parameters.

The first set is obtained for 10K by applying test voltages, VIL min and VIH max (sequentially) to the gate inputs, and measuring the OR and NOR output levels to make sure they are between VOL max and VOL min, and VOH max and VOH min specifications.

The second set of logic level parameters relates to the switching thresholds. This set of data is distinguished by an "A" in symbol subscripts. A test voltage, V_{ILA} max is applied to the gate and the NOR and OR outputs are measured to see that they are above the V_{OHA} min and below the V_{OLA} max levels, respectively. Similar checks are made using the test input voltage V_{IHA} min.

The result of these specifications insures that:

a) The switching threshold (\approx V_{BB}) falls within the darkest rectangle; i.e. switching does not begin outside this rectangle;

b) Quiescent logic levels fall in the lightest shaded ranges;

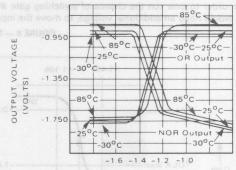
c) Guaranteed noise immunity is met.

As shown in Figure 6, MECL 10K outputs rise with increasing ambient temperature. All circuits in each

family have the same worst-case output level specifications regardless of power dissipation or junction temperature differences to reduce loss of noise margin due to thermal differences.

All of these specifications assume $-5.2 \,\mathrm{V}$ power supply operation. Operation at other power-supply voltages is possible, but will result in further transfer curve changes. Figure 7 gives rate of change of output voltages as a function of power supply.

FIGURE 6 — TYPICAL TRANSFER
CHARACTERISTICS AS A FUNCTION
OF TEMPERATURE (MECL 10K)



INPUT VOLTAGE (VOLTS)

FIGURE 7 — TYPICAL LEVEL CHANGE RATES

Voltage	MECL 10KH	MECL 10K*	MECL III
ΔVOH/ΔVEE	0.008	0.016	
ΔV _{OL} /ΔV _{EE}	0.020	0.250	0.270
ΔVΒΒ/ΔVΕΕ	0.010	0.148	0.140

^{*} and subsets: 10,200; 10,500; 10,600.

NOISE MARGIN

"Noise margin" is a measure of logic circuit's resistance to undesired switching. MECL noise margin is defined in terms of the specification points surrounding the switching threshold. The critical parameters of interest here are those designated with the "A" subscript (VOHA min, VOLA max, VIHA min, VILA max) in the transfer characteristic curves. MECL 10KH is specified and tested with VOHA min equal VOH min, VOLA max equal VOL max, VIHA min equal VIH min and VILA max equal VIL max. Guaranteed noise margin (NM) is defined as follows:

NMHIGH LEVEL = VOHA min - VIHA min NMLOW LEVEL = VILA max - VOLA max

To see how noise margin is computed, assume a MECL gate drives a similar MECL gate, Figure 8.

At a gate input (point B) equal to V_{ILA max}, MECL gate #2 can begin to enter the shaded transition region.

This is a "worst case" condition, since the V_{OLA} max specification point guarantees that no device can enter the transition region before an input equal to V_{ILA} max is reached. Clearly then, V_{ILA} max is one critical point for noise margin computation, since it is the edge of the transition region.

To find the other critical voltage, consider the output from MECL gate #1 (point A). What is the most positive value possible for this voltage (considering worst case specifications)? From Figure 8 it can be observed that the VOLA max specification insures that the LOW state OR output from gate #1 can be no greater than VOLA max.

Note that V_{OLA} max is more negative than V_{ILA} max-Thus, with V_{OLA} max at the input to gate #2, the transition region is not yet reached. (The input voltage to gate #2 is still to the left of V_{ILA} max on the transfer curve.)

In order to ever run the chance of switching gate #2, we would need an additional voltage, to move the input

from V_{OLA max} toV_{ILA max}. This constitutes the "safety factor" known as noise margin. It can be calculated as the magnitude of the difference between the two specification voltages, or for the MECL 10K levels shown:

$$\begin{array}{cccc} \text{NM}_{\text{LOW}} & -\text{V}_{\text{ILA max}} - \text{V}_{\text{OLA max}} \\ & -1.475 \text{ V} - (-1.630 \text{ V}) \\ & -155 \text{ mV}. \\ \text{Similarly, for the HIGH state:} \\ \text{NM}_{\text{HIGH}} & -\text{V}_{\text{OHA min}} - \text{V}_{\text{IHA min}} \\ & -0.980 \text{ V} - (-1.105 \text{ V}) \\ & -125 \text{ mV} \end{array}$$

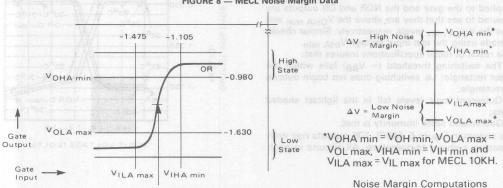
Analogous results are obtained when considering the "NOR" transfer data.

Note that these noise margins are absolute worst case conditions. The lessor of the two noise margins is that for the HIGH state, 125 mV. This then, constitutes the guaranteed margin against signal undershoot, and power or thermal disturbances.

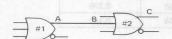
As shown in the table, typical noise margins are usually better than guaranteed — by about 75 mV. For MECL 10KH the "noise margin" is 150 mV for NM low and NM high. (See Section 3 for details.)

Noise margin is a dc specification that can be calculated, since it is defined by specification points tabulated on MECL data sheets. However, by itself, this specification does not give a complete picture regarding the noise immunity of a system built with a particular set of circuits. Overall system noise immunity involves not only noise-margin specifications, but also other circuit-related factors that determine how difficult it is to apply a noise signal of sufficient magnitude and duration to cause the circuit to propagate a false logic state. In general, then, noise immunity involves line impedances, circuit output impedances, and propagation delay in addition to noise-margin specifications. This subject is discussed in greater detail in Application Note AN-592.

FIGURE 8 — MECL Noise Margin Data



Specification Points for Determining Noise Margin



V_{BB} (switching threshold)

Family	Guaranteed Worst-Case dc Noise Margin (V)	Typical dc Noise Margin (V)		
MECL 10kH	0.150	0.270		
MECL 10k	0.125	0.210		
MECL III	0.115	0.200		

AC OR SWITCHING PARAMETERS

Time-dependent specifications are those that define the effects of the circuit on a specified input signal, as it travels through the circuit. They include the time delay involved in changing the output level from one logic state to another. In addition, they include the time required for the output of a circuit to respond to the input signal,

designated as propagation delay, MECL waveform and propagation delay terminologies are depicted in Figure 9. Specific rise, fall, and propagation delay times are given on the data sheet for each specific functional block, but like the transfer characteristics, ac parameters are temperature and voltage dependent. Typical variations for MECL 10K are given in the curves of Figure 10.

FIGURE 9 — TYPICAL LOGIC WAVEFORMS

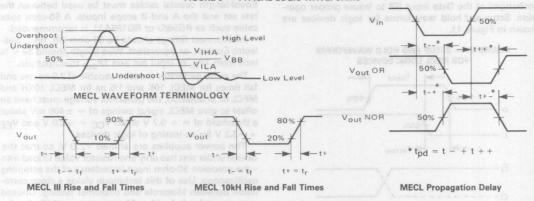


FIGURE 10a — TYPICAL PROPAGATION DELAY t- - versus VEE AND TEMPERATURE (MECL 10K)

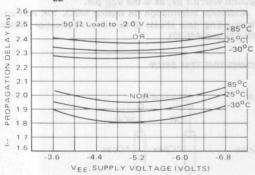


FIGURE 10c — TYPICAL FALL TIME (90% to 10%) versus TEMPERATURE AND SUPPLY VOLTAGE (MECL 10K)

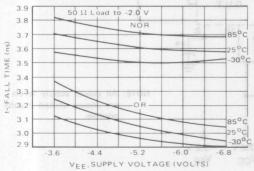


FIGURE 10b — TYPICAL PROPAGATION DELAY t++ versus
VEE AND TEMPERATURE (MECL 10K)

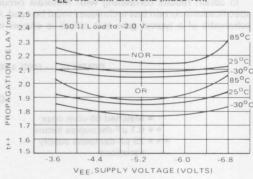
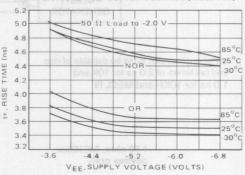


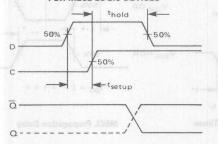
FIGURE 10d — TYPICAL RISE TIME (10% to 90%) versus
TEMPERATURE AND SUPPLY VOLTAGE (MECL 10K)



SETUP AND HOLD TIMES

Setup and hold times are two ac parameters which can easily be confused unless clearly defined. For MECL logic devices, $t_{\rm Setup}$ is the minimum time (50% - 50%) before the positive transition of the clock pulse (C) that information must be present at the Data input (D) to insure proper operation of the device. The t_{hold} is defined similarly as the minimum time after the positive transition of the clock pulse (C) that the information must remain unchanged at the Data input (D) to insure proper operation. Setup and hold waveforms for logic devices are shown in Figure 11.

FIGURE 11 — SETUP AND HOLD WAVEFORMS FOR MECL LOGIC DEVICES



TESTING MECL 10KH, MECL 10K and MECL III

To obtain results correlating with Motorola circuit specifications certain test techniques must be used. A schematic of a typical gate test circuit is shown in

Figure 12. This test circuit is the standard ac test configuration for most MECL devices. (Exceptions are shown with the device specification.)

A solid ground plane is used in the test setup, and capacitors bypass V_{CC1} , V_{CC2} , and V_{EE} pins to ground. All power leads and signal leads are kept as short as possible.

The sampling scope interface runs directly to the 50-ohm inputs of Channel A and B via 50-ohm coaxial cable. Equal-length coaxial cables must be used between the test set and the A and B scope inputs. A 50-ohm coax cable such as RG58/U or RG188A/U, is recommended.

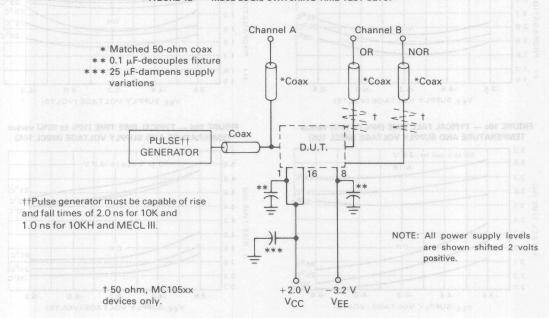
Interconnect fittings should be 50-ohm GR, BNC, Sealectro Conhex, or equivalent. Wire length should be $< \ensuremath{\mathcal{V}}_4$ inch from TP in to input pin and TP out to output pin.

The pulse generator must be capable of 2.0 ns rise and fall times for MECL 10K and 1.5 ns for MECL 10KH and MECL III. In addition, the generator voltage must have an offset to give MECL signal swings of $\approx \pm 400$ mV about a threshold of $\approx +$ 0.7 V when VCC = +2.0 V and VEE = -3.2 V for ac testing of logic devices.

The power supplies are shifted ± 2.0 V, so that the device under test has only one resistor value to load into – the precision 50-ohm input impedance of the sampling oscilloscope. Use of this technique yields a close correlation between Motorola and customer testing. Unused outputs are loaded with a 50-ohm resistor (100-ohm for MC105XX devices) to ground. The positive supply (VCC) should be decoupled from the test board by RF type 25µF capacitors to ground. The VCC pins are bypassed to ground with 0.1 µF, as is the VEE pin.

Additional information on testing MECL 10K and understanding data sheets is found in Application Notes AN-579 and AN-701.

FIGURE 12 — MECL LOGIC SWITCHING TIME TEST SETUP



ground potential and the V_{EE} point at -5.2 V. While this MECL convention is not necessarily mandatory, it does result in maximum noise immunity. This is so because any noise induced on the V_{EE} line is applied to the circuit as a common-mode signal which is rejected by the differential action of the MECL input circuit. Noise induced into the V_{CC} line is not cancelled out in this fashion. Hence, a good system ground at the V_{CC} bus is required for best noise immunity. Also, MECL 10KH circuits may be operated with V_{EE} at -4.5 V with a negligible loss of noise immunity.

Power supply regulation which will achieve 10% regulation or better at the device level is recommended. The –5.2 V power supply potential will result in best circuit speed. Other values for VEE may be used. A more negative voltage will increase noise margins at a cost of increased power dissipation. A less negative voltage will have just the opposite effect. (Noise margins and performance specifications of MECL 10KH are unaffected by variations in VEE because of the internal voltage regulation.)

On logic cards, a ground plane or ground bus system should be used. A bus system should be wide enough to prevent significant voltage drops between supply and device and to produce a low source inductance.

Although little power supply noise is generated by MECL logic, power supply bypass capacitors are recommended to handle switching currents caused by stray capacitance and asymmetric circuit loading. A parallel combination of a 1.0 μF and a 100 pF capacitor at the power entrance to the board, and a 0.01 μF low-inductance capacitor between ground and the –5.2 V line every four to six packages, are recommended.

Most MECL 10KH, MECL 10K and MECL III circuits have two V_{CC} leads. V_{CC1} supplies current to the output transistors and V_{CC2} is connected to the circuit logic transistors. The separate V_{CC} pins reduce cross-coupling between individual circuits within a package when the outputs are driving heavy loads. Circuits with large drive capability, similar to the MC10110, have two V_{CC1} pins. All V_{CC} pins should be connected to the ground plane or ground bus as close to the package as possible.

For further discussion of MECL power supply considerations to be made in system designing, see MECL System Design Handbook.

POWER DISSIPATION

The power dissipation of MECL functional blocks is specified on their respective data sheets. This specification does not include power dissipated in the output devices due to output termination. The omission of internal output pulldown resistors permits the use of external terminations designed to yield best system performance. To obtain total operating power dissipation of a particular functional block in a system, the dissipation of the output transistor, under load, must be added to the circuit power dissipation.

The table in Figure 13 lists the power dissipation in the output transistors plus that in the external terminating

resistors, for the more commonly used termination values and circuit configurations. To obtain true package power dissipation, one output-transistor power-dissipation value must be added to the specified package power dissipation for each external termination resistor used in conjunction with that package. To obtain system power dissipation, the stated dissipation in the external terminating resistors must be added as well. Unused outputs draw no power and may be ignored.

FIGURE 13 — AVERAGE POWER DISSIPATION IN OUTPUT CIRCUIT WITH EXTERNAL TERMINATING RESISTORS

Terminating Resistor Value	Output Transistor Power Dissipation (mW)	Terminating Resistor Power Dissipation (mW)
150 ohms to -2.0 Vdc	5.0	4.3
100 ohms to -2.0 Vdc	7.5	6.5
75 ohms to -2.0 Vdc	10	8.7
50 ohms to -2.0 Vdc	15	13
2.0 k ohms to VEE	2.5	7.7
1.0 k ohm to VEE	4.9	15.4
680 ohms to VEE	7.2	22.6
510 ohms to VEE	9.7	30.2
270 ohms to VEE	18.3	57.2
82 ohms to V _{CC} and 130 ohms to V _{EE}	15	140 06

LOADING CHARACTERISTICS

The differential input to MECL circuits offers several advantages. Its common-mode-rejection feature offers immunity against power-supply noise injection, and its relatively high input impedance makes it possible for any circuit to drive a relatively large number of inputs without deterioration of the guaranteed noise margin. Hence, dc fanout with MECL circuits does not normally present a design problem.

Graphs showing typical output voltage levels as a function of load current for MECL 10KH, MECL 10K and MECL III shown in Figure 14. These graphs can be used to determine the actual output voltages for loads exceeding normal operation.

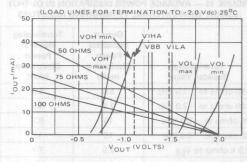
While dc loading causes a change in output voltage levels, thereby tending to affect noise margins, acloading increases the capacitances associated with the circuit and, therefore, affects circuit speed, primarily rise and fall times.

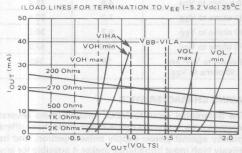
MECL circuits typically have a 7 ohm output impedance and are relatively unaffected by capacitive loading on a positive-going output signal. However, the negative-going edge is dependent on the output pulldown or termination resistor. Loading close to a MECL output pin will cause an additional propagation delay of 0.1 ns per fanout load with a 50 ohm resistor to -2.0 Vdc or 270 ohms to -5.2 Vdc. A 100 ohm resistor to -2.0 Vdc or

510 ohms to -5.2 Vdc results in an additional 0.2 ns propagation delay per fanout load.

Terminated transmission line signal interconnections are used for best system performance. The propagation delay and rise time of a driving gate are affected very little by capacitance loading along a matched parallel-terminated transmission line. However, the delay and characteristic impedance of the transmission line itself are affected by the distributed capacitance. Signal propagation down the line will be increased by a factor, $\sqrt{1+C_d/C_o}$. Here C_o is the normal intrinsic line capaci-

FIGURE 14 — OUTPUT VOLTAGE LEVELS Versus DC LOADING





tance, and C_d is the distributed capacitance due to loading and stubs off the line.

Maximum allowable stub lengths for loading off of a MECL 10K transmission line vary with the line impedance. For example, with $\rm Z_{\rm O}=50$ ohns, maximum stub length would be 4.5 inches (1.8 in. for MECL III). But when $\rm Z_{\rm O}=100$ ohms, the maximum allowable stub length is decreased to 2.8 inches (1.0 in. for MECL III).

The input loading capacitance of a MECL 10KH and MECL 10K gate is about 2.9 pF and 3.3 pF for MECL III. To allow for the IC connector or solder connection and a short stub length, 5 to 7 pF is commonly used in loading calculations.

UNUSED MECL INPUTS

The input impedance of a differential amplifier, as used in the typical MECL input circuit, is very high when the applied signal level is low. Under low-signal conditions, therefore, any leakage to the input capacitance of the gate could cause a gradual buildup of voltage on the input lead, thereby adversely affecting the switching characteristics at low repetition rates.

All single-ended input MECL logic circuits contain input pulldown resistors between the input transistor bases and VEE. As a result, unused inputs may be left unconnected (the resistor provides a sink for ICBO leakage currents, and inputs are held sufficiently negative that circuits will not trigger due to noise coupled into such inputs). Input pulldown resistor values are typically $50~\rm k\Omega$ and are not to be used as pulldown resistors for preceding open-emitter outputs.

MECL devices do not have input pulldowns. Examples are the differential line receivers. If a single differential receiver within a package is unused, one input of that receiver must be tied to the VBB pin provided, and the other input goes to VEE.

MECL circuits do not operate properly when inputs are connected to VCC for a HIGH logic level. Proper design practice is to set a HIGH level as about-0.9 volts below VCC with a resistor divider, a diode drop, or an unused gate output.

SECTION IV — SYSTEM DESIGN CONSIDERATIONS

THERMAL MANAGEMENT

Circuit performance and long-term circuit reliability are affected by die temperature. Normally, both are improved by keeping the IC junction temperatures low.

Electrical power dissipated in any integrated circuit is a source of heat. This heat source increases the temperature of the die relative to some reference point, normally the ambient temperature of 25°C in still air. The temperature increase, then, depends on the amount of power dissipated in the circuit and on the net thermal resistance between the heat source and the reference point.

The temperature at the junction is a function of the packaging and mounting system's ability to remove heat generated in the circuit — from the junction region to the ambient environment. The basic formula (a) for converting power dissipation to estimated junction temperature is:

$$T_{J} = T_{A} + P_{D}(\overline{\theta}_{JC} + \overline{\theta}_{CA}) \tag{1}$$

or $T_J = T_A + P_D(\overline{\theta}_{JA})$ (2)

where

T_J = maximum junction temperature T_A = maximum ambient temperature PD = calculated maximum power dissipation including effects of external loads (see Power Dissipation in section III).

 $\frac{\theta_{JC}}{\theta_{CA}}$ = average thermal resistance, junction to case average thermal resistance, case to ambient

 θ_{JA} = average thermal resistance, junction to ambient

This Motorola recommended formula has been approved by RADC and DESC for calculating a "practical" maximum operating junction temperature for MIL-M-38510 (JAN) MECL 10K devices.

Only two terms on the right side of equation (1) can be varied by the user — the ambient temperature, and the device case-to-ambient thermal resistance, $\overline{\theta}_{CA}$. (To some extent the device power dissipation can be also controlled, but under recommended use the V_{EE} supply and loading dictate a fixed power dissipation.) Both system air flow and the package mounting technique affect the $\overline{\theta}_{CA}$ thermal resistance term. $\overline{\theta}_{JC}$ is essentially independent of air flow and external mounting method, but is sensitive to package material, die bonding method, and die area.

FIGURE 15 — THERMAL RESISTANCE VALUES FOR STANDARD MECLI/C PACKAGES

THERMAL RESISTANCE IN STILL AIR											
PACKAGE DESCRIPTION PACKAGE						θJA		θЈС			
NO. BODY LEADS STYLE	BODY	BODY BODY	BODY DIE	DIE	DIE AREA	FLAG AREA	(°C/WATT)		(°C/WATT)		
	MATERIAL	WxL	BOND	(SQ. MILS)	(SQ. MILS)	AVG.	MAX.	AVG.	MAX		
8	DIL	EPOXY	1/4"x3/8"	EPOXY	2496	8100	102	133	50	80	
8	DIL	ALUMINA	1/4"x3/8"	GOLD	2496	N/A	140	182	35	56	
14	FLAT	ALUMINA	1/4"x1/4"	GOLD	4096	N/A	165	215	28	45	
14	DIL	EPOXY	1/4"x3/4"	EPOXY	4096	6400	84	109	38	61	
14	DIL	ALUMINA	1/4"x3/4"	GOLD	4096	N/A	100	130	25	40	
16	FLAT	BEO	1/4"x3/8"	GOLD	4096	N/A	88	114	13	21	
16	FLAT	ALUMINA	1/4"x3/8"	GOLD	4096	N/A	140	182	24	38	
16	DIL	EPOXY	1/4"x3/4"	EPOXY	4096	12100	70	91	34	54	
16	DIL	ALUMINA	1/4"x3/4"	GOLD	4096	N/A	100	130	25	40	
24	FLAT	BEO	3/8"x5/8"	GOLD	8192	N/A	40	52	6	10	
24	FLAT	ALUMINA	3/8"x5/8"	GOLD	8192	N/A	64	83	11	18	
24	DIL	EPOXY	1/2"x1-1/4"	EPOXY	8192	22500	67	87	31	50	
24	DIL	ALUMINA	1/2"x1-1/4"	GOLD	8192	N/A	50	65	10	16	

NOTES:

- 1. All plastic packages use copper lead frames—ceramic packages use alloy 42 frames.
- 2. Body style DIL is "Dual-In-Line"
- 3. BEO body material is only used for military temperature range products.
- 4. Standard Mounting Methods
 - a. Dual-In-Line In Socket or P/C board with no contact between bottom of package and socket or P/C board.
 - b. Flat Pack—Bottom of package in direct contact with non-metallized area of P/C board.

For applications where the case is held at essentially a fixed temperature by mounting on a large or temperature-controlled heat sink, the estimated junction temperature is calculated by:

$$T_{J} = T_{C} + P_{D}(\overline{\theta}_{JC})$$
 (3)

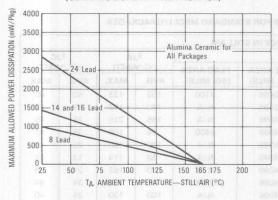
where T_C = maximum case temperature and the other parameters are as previously defined.

The maximum and average thermal resistance values for standard MECL IC packages are given in Figure 15. In Figure 16, this basic data is converted into graphs showing the maximum power dissipation allowable at various ambient temperatures (still air) for circuits mounted in the different packages, taking into account the maximum permissible operating junction temperature for long term life (≥ 100,000 hours).

AIR FLOW

The effect of air flow over the packages on $\overline{\theta}_{JA}$ (due to a decrease in $\overline{\theta}_{CA}$) is illustrated in the graphs of Figure 17. This air flow reduces the thermal resistance of the package, therefore permitting a corresponding increase in power dissipation without exceeding the maximum permissible operating junction temperature.

FIGURE 16A—AMBIENT TEMPERATURE DERATING CURVES
(CERAMIC DUAL-IN-LINE PACKAGE)



As an example of the use of the information above, the maximum junction temperature for a 16 lead ceramic dual-in-line packaged MECL 10K quad OR/NOR gate (MC10101L) loaded with four 50 ohm loads can be calculated. Maximum total power dissipation (including 4 output loads) for this quad gate is 195 mW. Assume for this thermal study that air flow is 500 linear feet per minute. From Figure 17, $\bar{\theta}_{JA}$ is 50°C/W. With T_A (air flow temperature at the device) equal to 25°C, the following maximum junction temperature results:

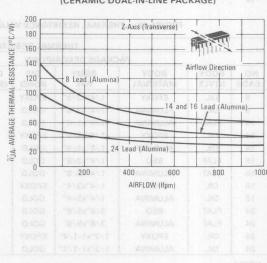
$$T_J = P_D(\overline{\theta}_{JA}) + T_A$$

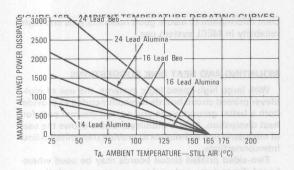
 $T_J = (0.195 \text{ W}) (50^{\circ}\text{C/W} + 25^{\circ}\text{C} = 34.8^{\circ}\text{C}$

Under the above operating conditions, the MECL 10k quad gate has its junction elevated above ambient temperature by only 9.8°C.

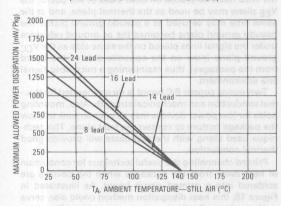
Even though different device types mounted on a printed circuit board may each have different power dissipations, all will have the same input and output levels provided that each is subject to identical air flow and the same ambient air temperature. This eases design, since the only change in levels between devices is due to the increase in ambient temperatures as the air passes over

FIGURE 17A—AIRFLOW VERSUS THERMAL RESISTANCE (CERAMIC DUAL-IN-LINE PACKAGE)









es yes vollege distribution of as a ground out, the cleannets should reminate into channel strips at each side or the rear of a plug-in type printed circuit board. The hear can then be remeved from the circuit board, or board silds rack, by means of wipers that come into thermal contact with the edge channels.

PIGURE 19 — CHANNEL/MIPOT HEAT CINKING ON DOI BLE



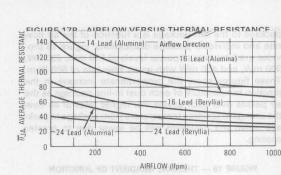
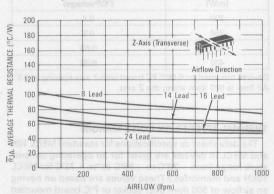


FIGURE 17C—AIRFLOW VERSUS THERMAL RESISTANCE (PLASTIC DUAL-IN-LINE PACKAGE)



operating junction remperatures below 145°C for All MECL device types. 1666-1670 and below 166°C for all other MECL device types.

The designer may want to use MECL devices under conditions other than those gives above. The majority at the low-power than those gives may be used without air and with higher 61A However, the designer must bear in mad that junction temperatures will be higher for another function temperatures will be higher for dighter \$1A. even though the ambient temperatures the

As an example, a 300 mW 16 lead dual-in line agrantic evide operated at $v_{\rm JA} = 160^{\circ}{\rm CeV}$ (in still air) shows a 15H logic level swift of about 21 mV above the HiGH gic level when operated with 560 firm air flow and a $y_{\rm A} = 50^{\circ}{\rm CeV}$. (Level shift = $4V_{\rm A} \times 1.4 \,{\rm mV}^{\circ}{\rm Ce}$) if togic levels of Individual devices shift by different

the devices, or differences in ambient temperature between two devices.

The majority of MECL 10KH, MECL 10K, and MECL III users employ some form of air-flow cooling. As air passes over each device on a printed circuit board, it absorbs heat from each package. This heat gradient from the first package to the last package is a function of the air flow rate and individual package dissipations. Figure 18 provides gradient data at power levels of 200 mW, 250mW, 300 mW, and 400 mW with an air flow rate of 500 lfpm. These figures show the proportionate increase in the junction temperature of each dual in-line package as the air passes over each device. For higher rates of air flow the change in junction temperature from package to package down the airstream will be lower due to greater cooling.

FIGURE 18 — THERMAL GRADIENT OF JUNCTION
TEMPERATURE
(16-Pin MECL Dual-In-Line Package)

Power Dissipation (mW)	Junction Temperature Gradient (°C/Package)
200	0.4
250	0.5
300	0.63
400	0.88

Devices mounted on 0.062" PC board with Z axis spacing of 0.5". Air flow is 500 Ifpm along the Z axis.

THERMAL EFFECTS ON NOISE MARGIN

The data sheet dc specifications for standard MECL 10K and MECL III devices are given for an operating temperature range from -30°C to $+85^{\circ}\text{C}$ (0° to $+75^{\circ}\text{C}$ for MECL 10KH and memories.) These values are based on having an airflow of 500 lfpm over socket or P/C board mounted packages with no special heat sinking (i.e., dual-in-line package mounted on lead seating plane with no contact between bottom of package and socket or P/C board and flat package mounted with bottom in direct contact with non-metallized area of P/C board). Under these conditions, adequate cooling is provided to keep the maximum operating junction temperatures below 145°C for MECL III device types 1666–1670 and below 165°C for all other MECL device types.

The designer may want to use MECL devices under conditions other than those given above. The majority of the low-power device types may be used without air and with higher $\overline{\theta}_{JA}$. However, the designer must bear in mind that junction temperatures will be higher for higher $\overline{\theta}_{JA}$, even though the ambient temperature is the same. Higher junction temperatures will cause logic levels to shift.

As an example, a 300 mW 16 lead dual-in-line ceramic device operated at $\bar{\theta}_{JA}=100^{\circ}\text{C/W}$ (in still air) shows a HIGH logic level shift of about 21 mV above the HIGH logic level when operated with 500 lfpm air flow and a $\bar{\theta}_{JA}=50^{\circ}\text{C/W}$. (Level shift = $\Delta T_J \times 1.4$ mV/°C).

If logic levels of individual devices shift by different amounts (depending on P_D and $\theta_{\rm JA}$), noise margins are

somewhat reduced. Therefore, the system designer must lay out his system bearing in mind that the mounting procedures to be used should minimize thermal effects on noise margin.

The following sections on package mounting and heat sinking are intended to provide the designer with sufficient information to insure good noise margins and high reliability in MECL system use.

MOUNTING AND HEAT SINK SUGGESTIONS

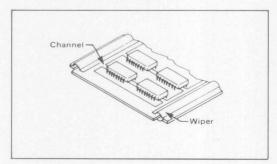
With large high-speed logic systems, the use of multilayer printed circuit boards is recommended to provide both a better ground plane and a good thermal path for heat dissipation. Also, a multilayer board allows the use of microstrip line techniques to provide transmission line interconnections.

Two-sided printed circuit boards may be used where board dimensions and package count are small. If possible, the V_{CC} ground plane should face the bottom of the package to form the thermal conduction plane. If signal lines must be placed on both sides of the board, the VEE plane may be used as the thermal plane, and at the same time may be used as a pseudo ground plane. The pseudo ground plane becomes the ac ground reference under the signal lines placed on the same side as the V_{CC} ground plane (now on the opposite side of the board from the packages), thus maintaining a microstrip signal line environment.

Two-ounce copper P/C board is recommended for thermal conduction and mechanical strength. Also, mounting holes for low power devices may be countersunk to allow the package bottom to contact the heat plane. This technique used along with thermal paste will provide good thermal conduction.

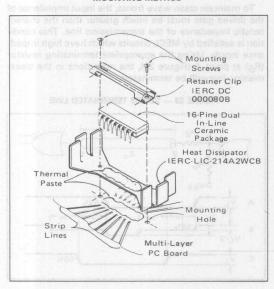
Printed channeling is a useful technique for conduction of heat away from the packages when the devices are soldered into a printed circuit board. As illustrated in Figure 19, this heat dissipation method could also serve as V_{EE} voltage distribution or as a ground bus. The channels should terminate into channel strips at each side or the rear of a plug-in type printed circuit board. The heat can then be removed from the circuit board, or board slide rack, by means of wipers that come into thermal contact with the edge channels.

FIGURE 19 — CHANNEL/WIPER HEAT SINKING ON DOUBLE LAYER BOARD



For operating some of the higher power device types*in 16 lead dual-in-line packages in still air, requiring $\bar{\theta}_{JA}$ <100°C/W, a suitable heat sink is the IERC LIC-214A2WCB shown in Figure 20. This sink reduces the still air $\bar{\theta}_{JA}$ to around 55°C/W. By mounting this heat sink directly on a copper ground plane (using silicone paste) and passing 500 lfpm air over the packages, $\bar{\theta}_{JA}$ is reduced to approximately 35°C/W, permitting use at higher ambient temperatures than +85°C (+75°C for MECL 10KH memories) or in lowering TJ for improved reliability.

FIGURE 20 — MECL HIGH-POWER DUAL-IN-LINE PACKAGE MOUNTING METHOD



It should be noted that the use of a heat sink on the top surface of the dual-in-line package is not very effective in lowering the $\bar{\theta}_{\rm JA}$. This is due to the location of the die near the bottom surface of the package. Also, very little (< 10%) of the internal heat is withdrawn through the package leads due to the isolation from the ceramic by the solder glass seals and the limited heat conduction from the die through 1.0 to 1.5 mil aluminum bonding wires.

INTERFACING MECL TO SLOWER LOGIC TYPES

MECL circuits are interfaceable with most other logic forms. For MECL/TTL/DTL interfaces, when MECL is operated at the recommended -5.2 volts and TTL/DTL at +5.0 V supply, currently available translator circuits, such as the MC10124 and MC10125, may be used.

For systems where a dual supply (-5.2 V and +5 V) is not practical, the MC12000 includes a single supply MECL to TTL and TTL to MECL translator, or a discrete component translator can be designed. For details, see MECL System Design Handbook. Such circuits can easily be made fast enough for any available TTL.

MECL also interfaces readily with MOS. With CMOS operating at +5 V, any of the MECL to TTL translators works very well. On the other hand, CMOS will drive MECL directly when using a common -5.2 V supply.

Specific circuitry for use in interfacing MECL families to other logic types is given in detail in the MECL System Design Handbook.

Complex MECL 10K devices are presently available for interfacing MECL with MOS logic, MOS memories, TTL three-state circuits, and IBM bus logic levels. See Application Note AN-720 for additional interfacing information.

CIRCUIT INTERCONNECTIONS

Though not necessarily essential, the use of multilayer printed circuit boards offers a number of advantages in the development of high-speed logic cards. Not only do multilayer boards achieve a much higher package density, interconnecting leads are kept shorter, thus minimizing propagation delay between packages. This is particularly beneficial with MECL III which has relatively fast (1 ns) rise and fall times. Moreover, the unbroken ground planes made possible with multilayer boards permit much more precise control of transmission line impedances when these are used for interconnecting purposes. Thus multilayer boards are recommended for MECL III layouts and are justified when operating MECL 10KH and MECL 10K at top circuit speed, when high-density packaging is a requirement, or when transmission line interconnects are used.

Point-to-point back-plane wiring without matched line terminations may be employed for MECL interconnections if line runs are kept short. At MECL 10K speeds, this applies to line runs up to 6 inches, for MECL 10KH up to 3.5", and for MECL III up to 1 inch (Maximum open wire lengths for less than 100 mV undershoot). But, because of the open-emitter outputs of MECL 10KH, MECL 10K and MECL III circuits, pull-down resistors are always required. Several ways of connecting such pull-down resistors are shown in Figure 21.

Resistor values for the connection in Figure 21a may range from 270 ohms to $k\Omega$ depending on power and load requirements. (See MECL System Design Handbook.) Power may be saved by connecting pull-down resistors in the range of 50 ohms (100 ohm minimum for MC10,500 and MC10,600 Series parts) to 150 ohms, to $-2.0\,\text{Vdc}$, as shown in Figure 22b. Use of a series damping resistor, Figure 22c, will extend permissible lengths of unmatched-impedance interconnections, with some loss of edge speed.

With proper choice of the series damping resistor, line lengths can be extended to any length,** while limiting overshoot and undershoot to a predetermined amount. Damping resistors usually range in value from 10 ohms to 100 ohms, depending on the line length, fanout, and line impedance. The open emitter-follower outputs of MECL 10KH, MECL III and MECL 10K give the system designer all possible line driving options.

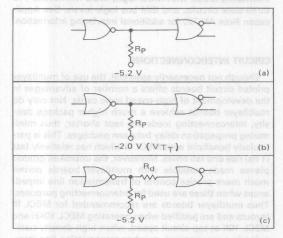
One major advantage of MECL over saturated logic is its capability for driving matched-impedance transmis-

^{*} MC1654, 1678, 1694, 10128, 10129, 10136, 10137, 10177, 10182, and 10804, MaxPD>800mW.

^{**} Limited only by line attenuation and band-width characteristics.

sion lines. Use of transmission lines retains signal integrity over long distances. The MECL 10KH and MECL 10K emitter-follower output transistors will drive a 50-ohm transmission line (100 ohms or greater MECL 10,500 and MC10,600 Series) terminated to -2.0 Vdc. This is the equivalent current load of 22 mA in the HIGH logic state and 6 mA in the LOW state.

FIGURE 21 — PULL-DOWN RESISTOR TECHNIQUES



Parallel termination of transmission lines can be done in two ways. One, as shown in Figure 22a, uses a single resistor whose value is equal to the impedance (Z_0) of the line. A terminating voltage (V_{TT}) of -2.0 Vdc must be supplied to the terminating resistor.

Another method of parallel termination uses a pair of resistors, R1 and R2. Figure 22b illustrates this method. The following two equations are used to calculate the values of R1 and R2:

$$R1 = 1.6 Z_0$$

 $R2 = 2.6 Z_0$

Another popular approach is the series-terminated transmission line (see Figure 23). This differs from parallel termination in that only one-half the logic swing is propagated through the lines. The logic swing doubles at the end of the transmission line due to reflection on an open line, again establishing a full logic swing.

FIGURE 22a — PARALLEL TERMINATED LINE

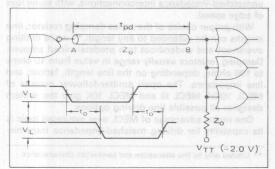
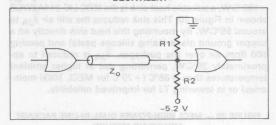
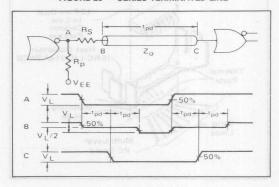


FIGURE 22b — PARALLEL TERMINATION—THEVENIN EQUIVALENT



To maintain clean wave fronts, the input impedance of the driven gate must be much greater than the characteristic impedance of the transmission line. This condition is satisfied by MECL circuits which have high impedance inputs. Using the appropriate terminating resistor (Rs) at point A (Figure 23), the reflections in the transmission line will be terminated.

FIGURE 23 — SERIES TERMINATED LINE



The advantages of series termination include ease of driving multiple series-terminated lines, low power consumption, and low cross talk between adjacent lines. The disadvantage of this system is that loads may not be distributed along the transmission line due to the one-half logic swing present at intermediate points.

For board-to-board interconnections, coaxial cable may be used for signal conductors. The termination techniques just discussed also apply when using coax. Coaxial cable has the advantages of good noise immunity and low attenuation at high frequencies.

Twisted pair lines are one of the most popular methods of interconnecting cards or panels. The complementary outputs of any MECL function may be connected to one end of the twisted pair line, and any MECL differential line receiver to the other as shown in the example, Figure 24. R_T is used to terminate the twisted pair line. The 1 to 1.5 V common-mode noise rejection of the line receiver ignores common-mode cross talk, permitting multiple twisted pair lines to be tied into cables. MECL signals may be sent very long distances (> 1000 feet) on twisted pair, although line attenuation will limit bandwidth, degrading edge speeds when long line runs are made.

If timing is critical, parallel signals paths (shown in Figure 25) should be used when fanout to several cards

is required. This will eliminate distortion caused by long stub lengths off a signal path.

Wire-wrapped connections can be used with MECL 10KH and MECL 10K. For MECL III, the fast edge speeds (1 ns) create a mismatch at the wire-wrap connections which can cause reflections, thus reducing noise immunity, The mismatch occurs also with MECL 10K, but the distance between the wire-wrap connections and the end of the line is generally short enough so the reflections cause no problem.

Series damping resistors may be used with wire-wrapped lines to extend permissible backplane wiring lengths. Twisted pair lines may be used for even longer distances across large wire-wrapped cards. The twisted pair gives a more defined characteristic impedance (than a single wire), and can be connected either single-ended, or differentially using a line receiver.

The recommended wire-wrapped circuit cards have a ground plane on one side and a voltage plane on the other side to insure a good ground and a stable voltage source for the circuits. In addition, the ground plane near the wire-wrapped lines lowers the impedance of those lines and facilitates terminating the line. Finally, the ground plane serves to minimize cross talk between parallel paths in the signal lines. Point-to-point wire routing is recommended because cross talk will be minimized and line lengths will be shortest. Commercial wire-wrap boards designed for MECL 10K are available from several vendors.

FIGURE 24 — TWISTED PAIR LINE DRIVER/RECEIVER

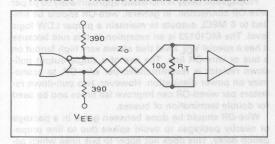
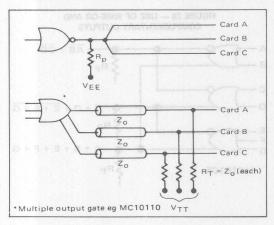


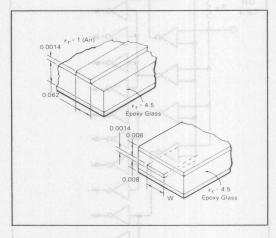
FIGURE 25 — PARALLEL FANOUT TECHNIQUES



Microstrip and Stripline

Microstrip and stripline techniques are used with printed circuit boards to form transmission lines. Microstrip consists of a constant-width conductor on one side of a circuit board, with a ground plane on the other side (shown in Figure 26). The characteristic impedance is determined by the width and thickness of the conductor, the thickness of the circuit board, and the dielectric constant of the circuit board material.

FIGURE 26 — PC INTERCONNECTION LINES FOR USE WITH MECL



Stripline is used with multilayer circuit boards as shown in Figure 26. Stripline consists of a constant-width conductor between two ground planes.

Refer to MECL System Design Handbook for a full discussion of the properties and use of these.

CLOCK DISTRIBUTION

Clock distribution can be a system problem. At MECL 10K speeds, either coaxial cable or twisted pair line (using the MC10101 and MC10115) can be used to distribute clock signals throughout a system. Clock line lengths should be controlled and matched when timing could be critical. Once the clocking signals arrive on card, a tree distribution should be used for large-fanouts at high frequency. An example of the application of ths technique is shown in Figure 27.

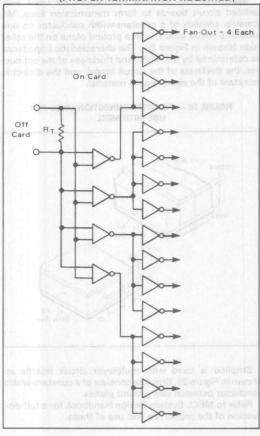
Because of the very high clock rates encountered in MECL III systems, rules for clocking are more rigorous than in slower systems.

The following guidelines should be followed for best results:

A. On-card Synchronous Clock Distribution via Transmission Line

- 1. Use the NOR output in developing clock chains or trees. Do not mix OR and NOR outputs in the chain.
 - 2. Use balanced fanouts on the clock drivers.
- 3. Overshoot can be reduced by using two parallel drive lines in place of one drive line with twice the lumped load.

FIGURE 27 — 64 FANOUT CLOCK DISTRIBUTION (PROPER TERMINATION REQUIRED)



- 4. To minimize clock skewing problems on synchronous sections of the system, line delays should be matched to within 1 ns.
- 5. Parallel drive gates should be used when clocking repetition rates are high, or when high capacitance loads occur. The bandwidth of a MECL III gate may be extended by paralleling both halves of a dual gate. Approximately 40 or 50 MHz bandwidth can be gained by paralleling two or three clock driver gates.
- 6. Fanout limits should be applied to clock distribution drivers. Four to six loads should be the maximum load per driver for best high speed performance. Avoid large lumped loads at the end of lines greater than 3 inches. A lumped load, if used, should be four or fewer loads.
- 7. For wire-OR (emitter dotting), two-way lines (busses) are recommended. To produce such lines, both ends of a transmission line are terminated with 100-ohms impedance. This method should be used when wire-OR connections exceed 1 inch apart on a drive line.

B. Off-Card Clock Distribution

1. The OR/NOR outputs of an MC1660 may be used to drive into twisted pair lines or into flat, fixed-impedance ribbon cable. At the far end of the twisted pair an MC1692 differential line receiver is used. The line should be terminated as shown in Figure 24. This method not only provides high speed, board-to-board clock distribution, but also provides system noise margin advantages. Since the line receiver operates independently of the VBB reference voltage (differential inputs) the noise margin from board to board is also independent of temperature differentials.

LOGIC SHORTCUTS

MECL circuitry offers several logic design conveniences. Among these are:

1. Wire-OR (can be produced by wiring MECL output emitters together outside packages).

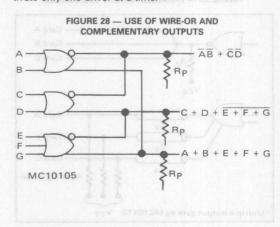
2. Complementary Logic Outputs (both OR and NOR are brought out to package pins in most cases).

An example of the use of these two features to reduce gate and package count is shown in Figure 28.

The connection shown saves several gate circuits over performing the same functions with non-ECL type logic. Also, the logic functions in Figure 29 are all accomplished with one gate propagation delay time for best system speed. Wire-ORing permits direct connections of MECL circuits to busses. (MECL System Design Handbook and Application Note AN-726).

Propagation delay is increased approximately 50 ps per wire-OR connection. In general, wire-OR should be limited to 6 MECL outputs to maintain a proper LOW logic level. The MC10123 is an exception to this rule because it has a special V_{OL} level that allows very high fanout on a bus or wire-OR line. The use of a single output pull-down resistor is recommended per wire-OR, to economize on power dissipation. However, two pull-down resistors per wired-OR can improve fall times and be used for double termination of busses.

Wire-OR should be done between gates in a package or nearby packages to avoid spikes due to line propagation delay. This does not apply to bus lines which activate only one driver at a time.

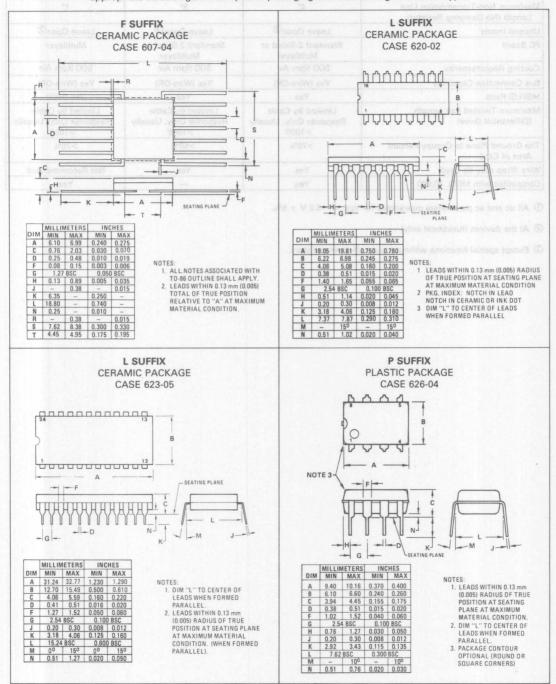


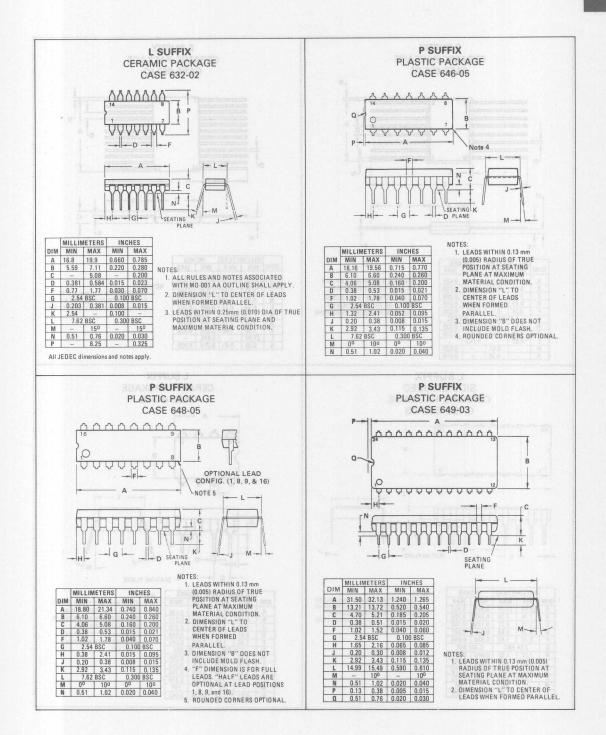
Maximum Non-Transmission Line Length (No Damping Resistor)	4"	8"	1"	
Unused Inputs	Leave Open 3	Leave Open 3	Leave Open®	
PC Board \$50-050 32AO	Standard 2-Sided or Multilayer	Standard 2-Sided or Multilayer	Multilayer	
Cooling Requirements	500 Ifpm Air	500 Ifpm Air	500 Ifpm Air	
Bus Connection Capability	Yes (Wire-OR)	Yes (Wire-OR)	Yes (Wire-OR)	
MSI/LSI Parts	Yes	Yes	Yes (MSI)	
Maximum Twisted Pair Length (Differential Drive)	Limited By Cable Response Only, Usually >1000'	Limited by Cable Response Only, Usually >1000'	Limited by Cable Response Only, Usually >1000'	
The Ground Plane to Occupy Percent Area of Card	>75%	>50%	>75%	
Wire Wrap may be used	Yes	Yes	Not Recommended	
Compatible with MECL 10,000	Yes		Yes	

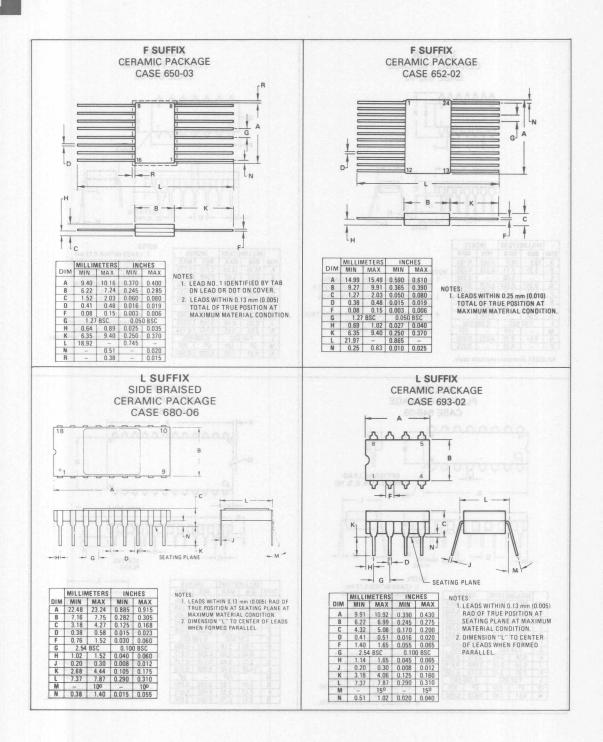
- \bigcirc All dc and ac parameters guaranteed for VEE = -5.2 V \pm 5%.
- 2 At the devices (functional only).
- 3 Except special functions without input pull-down resistors.

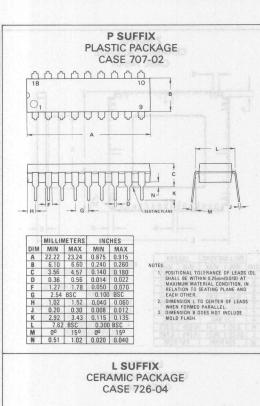
PACKAGE OUTLINE DIMENSIONS

A letter suffix to the MECL logic function part number is used to specify the package style (see drawings below). See appropriate selector guide for specific packaging available for a given device type.



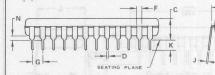






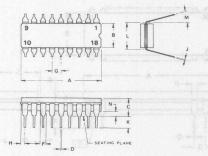
P SUFFIX PLASTIC PACKAGE CASE 724-02





	MILLIN	METERS	INC	HES		
DIM	MIN	MAX	MIN	MAX		
A	31.24	32.13	1.230	1.265		
В	6.35	6.86	0.250	0.270		
C	4.06	4.57	0.160	0.180		
D	0.38	0.51	0.015	0.020		
F	1.02	1.52	0.040	0.060		
G	2.54	2.54 BSC		0.100 BSC		
Н	1.60	2.11	0.063	0.083		
J	0.18	0.30	0.007	0.012		
K	2.92	3.43	0.115	0.135		
L	7.37	7.87	0.290	0.310		
M	-	100	N SIA	100		
N	0.51	1.02	0.020	0.040		

NOTE:
1. LEADS, TRUE POSITIONED WITHIN
0.25 mm (0.010) DIA AT SEATING
PLANE AT MAXIMUM MATERIAL
CONDITION (DIM D).



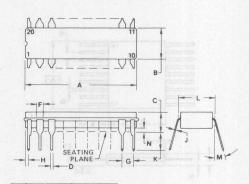
	DIM	MIN	MAX	MIN	MAX
	Α	22.35	23.11	0.880	0.910
	В	6.10	7.49	0.240	0.295
	C	-	5.08	-	0.200
	D	0.38	0.53	0.015	0.021
	F	1.40	1.78	0.055	0.070
j	G	2.54	BSC	0.100	BSC
	Н	0.51	1.14	0.020	0.045
1	J	0.20	0.30	0.008	0.012
1	K	3.16	4.32	0.125	0.170
1	L	7.62	BSC	0.300	BSC
١	M	00	150	00	150
i	N	0.51	1.02	0.020	0.040

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NOTES:

- 1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA. AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
- 2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
- 3. DIM "A" & "B" INCLUDES MENISCUS.

L SUFFIX CERAMIC PACKAGE CASE 732-03

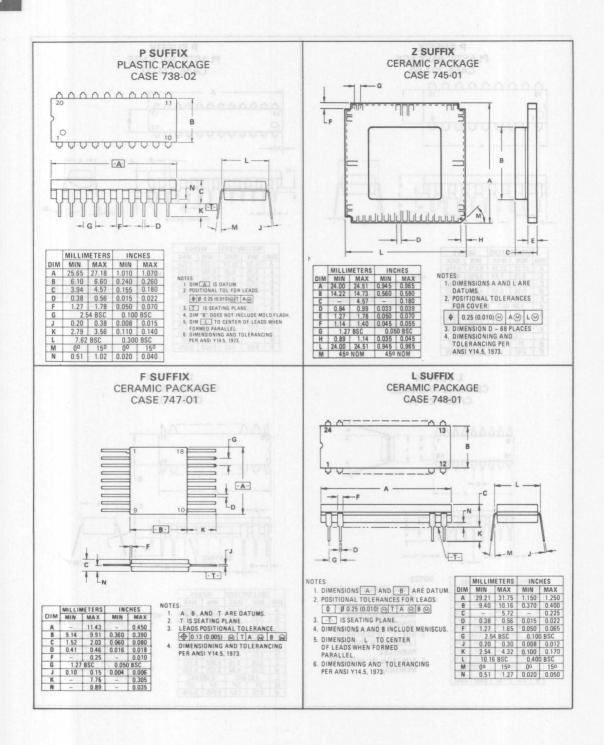


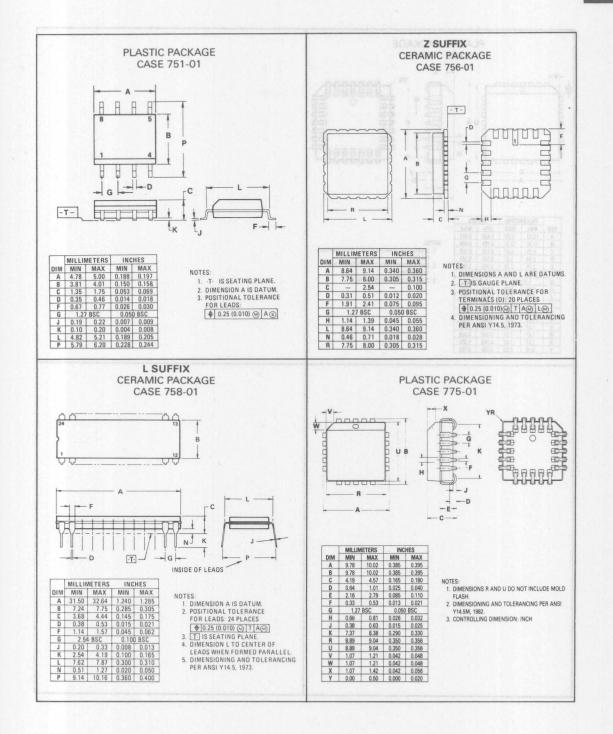
	MILLIN	TERS	INCHES			
MID	MIN	MAX	MIN	MAX		
Α	23.88	25.15	0.940	0.990		
В	6.60	7.49	0.260	0.295		
C	3.81	5.08	0.150	0.200		
D	0.38	0.56	0.015	0.022		
F	1.40	1.65	0.055	0.065		
G	2.54	BSC	0.100 BSC			
Н	0.51	1.27	0.020	0.050		
J	0.20	0.30	0.008	0.012		
K	3.18	4.06	0.125	0.160		
L	7.62	BSC	0.300	BSC		
M	00	150	00	150		
N	0.25	1.02	0.010	0.040		

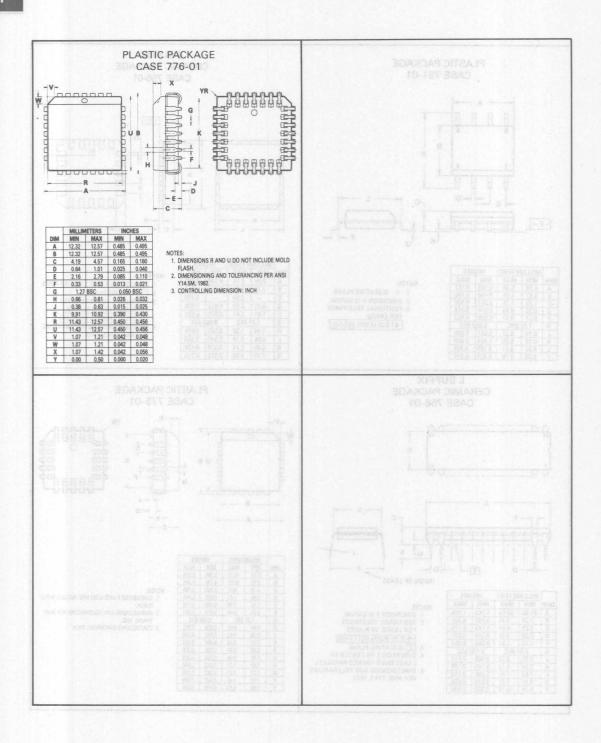
NOTES:

- 1. LEADS WITHIN 0.25 mm (0.010) DIA , TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
 2. DIM L TO CENTER OF LEADS
- WHEN FORMED PARALLEL.

 3. DIM A AND B INCLUDES
 MENISCUS.







- "Improve Fast-Logic Designs, by Bill Blood, Electronic Design, May 10, 1973.
- "Interface TTL Systems with ECL Circuits," by George Adams, EDN, September 5, 1973.
- "Increasing Minicomputer Speed with Emitter-Coupled Logic," by Jon De Laune, Computer Design, February 1974.
- "An Engineering Comparison Study MECL 10,000 and Schottky TTL," Motorola Inc., 1974.
- "ECL Circuits Drive Light-Emitting Diodes," by Bill Blood, EDN, January 20, 1974.
- "Four-Digit BCD Programmability Featured in Variable Modulus 60 MHz Counter," by Tom Balph and Bill Blood, Electronic Design, March 15, 1974.

- Electronic Design, August 16, 1974.
- "A CAD Program for High Speed Logic Element Interconnections," by Thomas Balph, William Blood, and Jerry Prioste, Computer Design, May 1975.
- "Build a Clock Bias Circuit for ECL Flip-Flops," by T. Balph and H. Gnauden, EDN, May 5, 1975.
- "Get the Best Processor Performance by Building It From ECL Bit Slices," By Tom Balph and Bill Blood, Electronic Design, June 7, 1977.
- "MECL System Design Handbook," by Bill Blood, Motorola Inc.

APPLICATION NOTES

Copies of these Application Notes and Engineering Bulletins can be obtained from your Motorola representative or authorized distributor, or from Technical Information Center, Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix, Arizona 85036.

- AN-270 Nanosecond Pulse Handling Techniques
- AN-504 The MC1600 Series MECL III Gates
- AN-535 Phase-Locked Loop Design Fundamentals
- AN-553 A New Generation of Integrated Avionic Synthesizers
- AN-556 Interconnection Techniques for Motorola's MECL 10K Series Emitter Coupled Logic
- AN-565 Using Shift Registers as Pulse Delay Networks
- AN-567 MECL Positive and Negative Logic
- AN-579 Testing MECL 10K Integrated Logic Circuits
- AN-581 An MSI 500 MHz Frequency Counter Using MECL and TTL
- AN-586 Measure Frequency and Propagation Delay with High Speed MECL Circuits
- AN-592 AC Noise Immunity of MECL 10K Integrated
- AN-700 Simulate MECL System Interconnections with a Computer Program

- AN-701 Understanding MECL 10K DC and AC Data Sheet Specifications
- AN-709 MECL 10k Arithmetic Elements, MC10179, MC10180, MC10181
- AN-720 Interfacing with MECL 10K Integrated Circuits
- AN-726 Bussing with MECL 10K Integrated Circuits
- AN-730 A High-Speed FIFO Memory Using the MECL MCM10143 Register File
- AN-742 A 200 MHz Autroranging MECL-McMOS Frequency Counter
- AN-774 A Simple High Speed Bipolar Microprocessor Illustrates System Design and Microprogram Techniques
- AN-827 Technique of Direct Programming Using Two-Modulus Prescaler
- EB-47 Event Counter and Storage Latches for High Frequency, High Resolution Counters
- EB-48 A Time Base and Control Logic Subsystem for High Frequency, High Resolution Counters

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- 1 'Improve Fest-Logic Designs," by 810 Blood, filectronic Design, May 10, 1973.
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- 'Build a Low Cost ECL Logic Proba: "by Tom Earth
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- A CAS Program for High Speed Logic Element Interconnections," by Thomas Balph, William Blood and Jerry Princis Computer Design, May 1875.
- 'Build a Clock Stas Circuit for ECL Flip-Flops,' by T Salph and H. Gnauden, EDN, May 5, 1975.
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APPRICATION NOTES

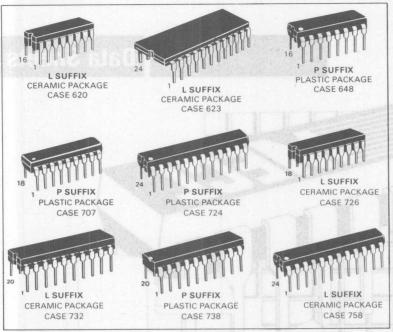
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- EB-47 Event Counter and Storage Latenes for High Fre-
- Bulb A Time Base and Control Logic Subsystem for

Data Sheets

Standard Packages



Special Packages



Function Selection—(0 to +75°C)

Function	Device	Case
NOR Gate		
Quad-2-Input with Strobe	MC10H100	620, 648
Quad-2-Input	MC10H102	620, 648
Triple 4-3-3 Input	MC10H106	620, 648
Dual 3-Input 3-Output	MC10H211	620, 648
OR Gate		
Quad 2-Input	MC10H103	620, 648
Dual 3-Input 3-Output	MC10H210	620, 648
AND Gates		
Quad AND	MC10H104	620, 648
Complex Gates		
Quad OR/NOR	MC10H101	620, 648
Triple 2-3-2 Input OR/NOR	MC10H105	620, 648
Triple Exclusive OR/NOR	MC10H107	620, 648
Dual 4-5 Input OR/NOR	MC10H109	620, 648
Quad Exclusive OR	MC10H113	620, 648
Dual 2-Wide OR-AND/OR-AND INVERT	MC10H117	620, 648
Dual 2-Wide 3-Input OR/AND	MC10H118	620, 648
4-Wide 4-3-3-3 Input OR-AND	MC10H119	620, 648
4-Wide OR-AND/OR-AND INVERT	MC10H121	620, 648
Hex Buffer w/Enable	MC10H188	620, 648
Hex Inverter w/Enable	MC10H189	620, 648

Function	Device	Case
Translators		
Quad TTL to MECL	MC10H124	620, 648
Quad MECL TO TTL	MC10H125	620, 648
Quad MECL-to-TTL Translator, Single Power Supply (-5.2 V or		
+5.0 V)	MC10H350	620, 648
Quad TTL to MECL, ECL Strobe	MC10H424	620, 648
Receivers		
Quad Line Receiver	MC10H115	620, 648
Triple Line Receiver	MC10H116	620, 648
Flip-Flop Latches		
Dual D Master Slave Flip-Flop	MC10H131	620, 648
Dual J-K Master Slave Flip-Flop	MC10H135	620, 648
Hex D Flip-Flop	MC10H176	620, 648
Dual D Latch	MC10H130	620, 648
Quint Latch	MC10H175	620, 648
Hex D Flip-Flop	MC10H186	620, 648
w/Common Reset		
Parity Checker		
12-Bit Parity Generator-Checker	MC10H160	620, 648

Binary to 1-8 (High)	MC10H162	620, 648
Dual Binary to 1-4 (Low)	MC10H171	620, 648
Dual Binary to 1-4 (High)	MC10H172	620, 648
3-Input Priority Encoder	MC10H165	620, 648
Data Selector Multiplexer	rocciones a chic	
Quad Bus Driver/Receiver with		
2-to-1 Output Multiplexers	MC10H330	758, 724
Dual Bus Driver/Receiver with	VEGGGGGG	
4-to-1 Output Multiplexers	MC10H332	732, 738
Quad 2-Input Multiplexers	a comentous be	word in th
(Noninverting)	MC10H158	620, 648
Quad 2-Input Multiplexers	will rither pools	_intelsi m
(Inverting)	MC10H159	620, 648
8-Line Multiplexer	MC10H164	620, 648
Quad 2-Input Multiplexer Latch	MC10H173	620, 648
Dual 4-1 Multiplexer	MC10H174	620, 648
Counters		
Universal Hexadecimal	MC10H136	620, 648
Binary Counter	MC10H016	620, 648
Arithmetic Functions	darren 1 St	
Look Ahead Carry Block Dual High Speed Adder/	MC10H179	620, 648
Subtractor	MC10H180	620, 648
4-Bit ALU	MC10H181	623, 649
Ly 261 201 0		724, 758
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Figure 2 illustrates the relative size difference however, the junction isolated translator of MCCL 10K, and the junction isolated translator of MCCL 10KM. This suggests that parton sacre could be improved awoloid at lower power perfect that illustration is the gate level, the power pitch output translator cannot be reduced without searificing output demicrated sides because of the 50 ohm trive requirements of MECL. In more complex functions, where part of the delay is associated with internal gates. MECL 10KH devices use less power than the aquivalent MECL 10KH devices and previde an even more significant improvement.

THERE I. -- TYPICAL PAMILY CHARACTERISTICS FOR THE AND 182H CHICUITS

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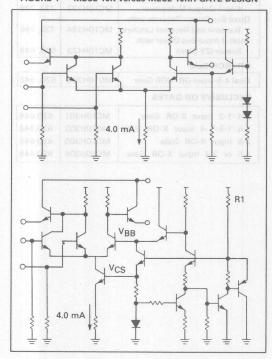
Quad Bus Driver/Receiver with	MC10H166	620, 648 620, 648
Transmit and Receiver Latches	MC10H334	732, 738
Memories	nemen menter esamble rang	ang zawa 5% nanwe
16 × 4 Bit Register File 8 × 2 Bit Content Addressable	MC10H145	620, 648
Memory	MC10H155	707, 726
Bus Driver (25 ohm outputs)	aya gmitaixa	enhance
Triple 4-3-3 Input Bus Driver (25 Ohms)	MC10H123	620, 648
Quad Bus Driver/Receiver with 2-to-1 Output Multiplexers Dual Bus Driver/Receiver with	MC10H330	724, 758
4-to-1 Output Multiplexers Quad Bus Driver/Receiver with	MC10H332	732, 738
Transmit and Receiver Latches Triple 3-Input Bus Driver with	MC10H334	732, 738
Enable (25 Ohm)	MC10H423	620, 648
OR/NOR Gate	9 4	-
Dual 4-5-Input OR/NOR Gate	MC10H209	620, 648
EXCLUSIVE OR GATES		
2-4/1-2 Input X-OR Gate	MC10H301	620,648
2-4/1-6/1-4 Input X-OR Gate	MC10H302	620,648
2-5 Input X-OR Gate	MC10H303	620,648
1-5 or 2-4 Input X-OR Gate	MC10H304	620,648

The schematics in Figure 1 compare the basic gate structure of the MECL 10KH to that of MECL 10K devices. The gate switch current is established with a function source in the MECL 10KH family as compared to a resistor source in MECL 10KH family as compared to a resistor to the MECL 10KH series. The advantages of these design devices has been replaced with a vottage regulator in the resistors that yield correspondingly bean related collector desistors that yield correspondingly bean related developed the power supply changes and matched output vacking refus with supply changes and matched output vacking refus with state as the gate level however, the sided performance more than corresponding.

MECL 10KH INTRODUCTION

Motorola's new MECL 10KH family features 100% improvement in propagation delay and clock speeds while maintaining power supply current equal to MECL 10K. This new MECL family is voltage compensated which allows guaranteed dc and switching parameters over a $\pm 5\%$ power supply range. Noise margins of MECL 10KH are 75% better than the MECL 10K series over the $\pm 5\%$ power supply range. MECL 10KH is compatible with MECL 10K and MECL III, a key element in allowing users to enhance existing systems by increasing the speed in critical timing areas. Also, many MECL 10KH devices are pinout/functional duplications of the MECL 10K series devices.

FIGURE 1 — MECL 10K versus MECL 10KH GATE DESIGN



The schematics in Figure 1 compare the basic gate structure of the MECL 10KH to that of MECL 10K devices. The gate switch current is established with a current source in the MECL 10KH family as compared to a resistor source in MECL 10K. The bias generator in the MECL 10K device has been replaced with a voltage regulator in the MECL 10KH series. The advantages of these design changes are: current-sources permit-matched collector resistors that yield correspondingly better matched delays, less variation in the output-voltage level with power supply changes, and matched output-tracking rates with temperature. These circuit changes increase complexity at the gate level; however, the added performance more than compensates.

The MECL 10KH family is being fabricated using Motorola's MOSAIC I (Motorola Oxide Self Aligned Implanted Circuits). The switching transistor's geometries obtained in the MOSAIC I process show a two-fold improvement in fτ, a reduction of more than 50% in parasitic capacitance and a decrease in device area of almost 76%.

FIGURE 2 — MOSAIC versus MECL 10K SWITCHING TRANSISTOR GEOMETRY

With improved geometry, the MECL 10KH switching transistors (left) are one-seventh the size of the older MECL 10K transistors (right). Along with the smaller area comes an improved f_T and reduced parasitic capacitances.

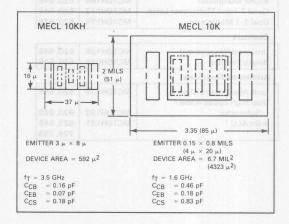


Figure 2 illustrates the relative size difference between the junction isolated transistor of MECL 10K and the MOSAIC I transistor of MECL 10KH. This suggests that performance could be improved twofold at lower power levels. However, at the gate level, the power of the output transistor cannot be reduced without sacrificing output characteristics because of the 50 ohm drive requirements of MECL. In more complex functions, where part of the delay is associated with internal gates, MECL 10KH devices use less power than the equivalent MECL 10K devices and provide an even more significant improvement in ac performance.

Table 1. — TYPICAL FAMILY CHARACTERISTICS FOR 10K AND 10KH CIRCUITS

	10K	10KH
Propagation delay (ns)	2.0	1.0
Power (mW)	25	25
Power-speed product (pJ)	50	25
Rise/fall times (ns) (20-80%)	2.0	1.5
Temperature range (°C)	-30 to +85	0 to +75
Voltage regulated	No	Yes
Technology	Junction	Oxide
	isolated	isolated
$V_{EE} = -5.2 \text{ V}$		

Supply & Temperature Variation

MECL 10KH temperature and voltage compensation is designed to guarantee compatibility with MECL 10K, MECL III, MECL Memories and the MC10900 and Macrocell Array products. Table 1 summarizes some performance characteristics of the MECL 10K and 10KH logic families in a 16-pin DIP. The MECL 10KH devices offer typical propagation delays of 1.0 ns at 25 mW per gate when operated from a $V_{\mbox{\footnotesize{EE}}}$ of -5.2 V. The resulting speed-power product of 25 picojoules is the best of any ECL logic family available today.

The operating temperature range is changed from -30°C to $+85^{\circ}\text{C}$ of the MECL 10K family to the narrower range of 0°C to 75°C for MECL 10KH. This change matches the constraints established by the memory and array products. Operation at -30°C would require compromises in performance and power. With few exceptions, commercial applications are satisfied by 0°C min.

Table 2. — MECL 10KH AC SPECIFICATIONS AND TRACKING

Parameter	Min	0°C Typ	Max	D. P. L.	25°C Typ			75°C Typ	Max	Units
tPD	0.7	1.1	1.6	0.7	1.0	1.5	0.7	1.1	1.7	ns
	Mii	n I	Vlax	Mii	1	Vlax	Mir	1	Max	
t _R (20-80%)	0.8	3	2.2	0.7		2.0	0.8		2.2	ns
t _F (20-80%)	0.8	3	2.2	0.7	-	2.0	0.8		2.2	ns

Delay variation Propagation Delay variation Parameter delay (ns)* vs temp (ps/°C) vs supply (ps/V) Тур Max Тур Max Тур Max 2.0 2.9 2.0 7.0 80 10K tPD 10KH 1.0 0.5 4.0 0 0

*V_{EE} = -5.2 V, Temp = 25°C

AC specifications of MECL 10KH products appear in Table 2. In the MECL 10KH family, all ac specifications have guaranteed minimums and maximums for extremes of both temperature and supply — a first in ECL logic. In addition, flip flops, latches and counters will have guaranteed limits for setup time, hold time, and clock pulse width. The limits in Table 2 are guaranteed for a power supply variation of $\pm 5\%$. MECL 10K typically has a propagation delay (tpD) variation of 80 ps/V with no guaranteed maximum. The typical variation in tpD for MECL 10KH circuits is only 38 ps typically over the entire specified temperature range and power-supply tolerance, and is guaranteed not to exceed 300 ps.

The improved performance in temperature over MECL 10K are a result of the internal voltage regulator. The primary difference being the flatter tracking rate of the output "0" level voltage (V_{OL}). This difference does not affect the compatibility with existing MECL families.

Changes in output "1" level voltages (V_{OH}) with supply variations are 10 mV/V less for the MECL 10KH family. V_{OH} varies with the supply, primarily because of changes in chip temperature caused by the changes in power dissipation. However, the current in the MECL 10KH circuits remains almost constant with supply changes, since the circuits are voltage compensated and use current sources for all internal emitter followers. Threshold voltage (V_{BB})

Table 3. — LOGIC LEVEL DC TRACKING RATE FOR 10K AND 10KH CIRCUITS

		Min	Тур	Max
ΔVOH/ΔΤ	10KH	1.2	1.3	1.5
(mV/°C)	10K	1.2	1.3	1.5
ΔV _{BB} /ΔΤ	10KH	0.8	1.0	1.2
(mV/°C)	10K	0.8	1.0	1.2
ΔV _{OL} /ΔΤ	10KH	0	0.4	0.6
(mV/°C)	10K	0.35	0.5	0.75
		0.75	1.0	1.55
ΔVOH/ΔVFF	10KH	-20	bloow r	0
(mV/V)	10K	-30	noise m	erric 0
ΔV _{BB} /ΔV _{FF}	10KH	0	10	25
(mV/V)	10K	110	150	190
ΔVΟΙ/ΔVFF	10KH	08 W 0 18	20	50
(mV/V)	10K	200	250	320

and output "0" level voltage (V_{OL}) variations are shown with respect to MECL 10K in Table 3. In both cases voltage compensation has reduced the variations significantly.

Noise Margin Considerations

Specification of input voltage levels (V_{IHA}, V_{ILA}) are changed from those of MECL 10K resulting in improved noise margins for MECL 10KH.

The MECL 10K circuits have two sets of output voltage specifications (V_{OH}, V_{OHA} and V_{OL}, V_{OLA}). The first output voltage specification in each set (V_{OH} and V_{OL}) are guaranteed maximum and minimum output levels for typical input levels. The second specification in each set (V_{OHA} and V_{OLA}) is the guaranteed worst-case output level for input threshold voltages. System analysis for worst-case noise margin considers V_{OHA} and V_{OLA} only. The MECL 10KH family has only one set of output voltages (V_{OH} and V_{OL}) with minimum and maximum values specified. The minimum value of V_{OH} and the maximum value for V_{OL} of the MECL 10KH family is synonomous with the V_{OHA} and V_{OLA} specifications of MECL 10K family.

The V_{OH} values for the MECL 10KH circuits are equal to or better than the MECL 10K levels at all temperatures. Input threshold voltages (V_{IHA} and V_{ILA}, which are synonymous with V_{IH} min and V_{IL} max for 10KH) are also improved and guaranteed V_{IHA} has been decreased by 25 mV over the entire operating temperature range, resulting in a "1" level noise margin of 150 mV (compared to

Table 4. — NOISE MARGIN versus POWER-SUPPLY CONDITIONS

Parameter		V _{EE} -10%		V _{EE} -5%		VEE		V _{EE} +5%	
		Тур	Min	Тур	Min	Тур	Min	Тур	Min
Noise Margin High	10KH	224	150	227	150	230	150	233	150
V _{NH} (mV)	10K	127	47	166	86	205	125	241	164
Noise Margin Low	10KH	264	150	267	150	270	150	273	150
V _{NL} (mV)	10K	223	103	249	129	275	155	301	181

*Temp = 0 to 75°C

125 mV for the MECL 10K circuits). V_{ILA} has been decreased by 5.0 mV, providing a "0" level noise margin equal to the "1" level noise margin. The V_{OL} minimum of the MECL 10KH is more negative than for MECL 10K (~1950 mV) instead of ~1850 mV). The V_{OL} level for the MECL 10K family was selected to ensure that the gate would not saturate at high temperatures and high supply voltages. The reduction in operating temperature range for the MECL 10KH family and the improvement in tracking rate allow the lower V_{OL} level. The change in this level does not affect system noise margins. Although some of the interface levels change with temperature, the changes in voltage levels are well within the tolerance ranges that would keep the families compatible. Table 4 lists some noise margins for V_{EE} supply variations.

The compatibility of MECL 10KH with MECL 10K may be demonstrated by applying the tracking rates in Table 3 to the dc specifications. The method for determining compatibility is to show acceptable noise margins for MECL 10KH, MECL 10K and mixed MECL 10K/MECL 10KH systems. The asssumption is that the families are compatible if the noise margin for a mixed system is equal to or better than the same system using only the MECL 10K series.

Using an all MECL 10K system as a reference, three possible logic mixes must be considered: MECL 10K driving MECL 10KH; MECL 10KH driving MECL 10KH arving MECL 10KH. The system noise margin for the three configurations can now be calculated for the following cases (See Figure 3):

In Case 1, the system uses multiple power supplies, each independently voltage regulated to some percentage tolerance. Worst-case is where one device is at the plus extreme and the other device is at the minus extreme of the supply tolerance.

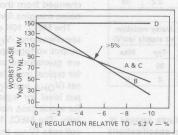
In Case 2, a system operates on a single supply or several supplies slaved to a master supply. The entire system can drift, but all devices are at the same supply voltage.

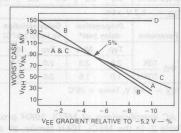
In Case 3, a system has excessive supply drops throughout. Supply gradients are due to resistive drops in V_{FF} bus.

The analysis indicates that the noise margins for a MECL 10K/10KH system equal or exceed the margins for an all 10K system for supply tolerance up to $\pm 5\%$. The results of the analysis are shown in Figure 3.

FIGURE 3 — NOISE MARGIN versus POWER-SUPPLY VARIATION

Case 2





Case 3

A. MECL 10K DRIVING MECL 10K B. MECL 10K DRIVING MECL 10KH C. MECL 10KH DRIVING MECL 10K D. MECL 10KH DRIVING MECL10KH

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Advance Information

MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

The MC10H016 is a member of Motorola's new MECL family. The MC10H016 is a high-speed synchronous, presettable, cascadable 4-bit binary counter. It is useful for a large number of conversion, counting and digital integration applications.

- Counting Frequency, 200 MHz Minimum
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V _{CC} = 0)	VEE	-8.0 to 0	Vdc
Input Voltage (V _{CC} = 0)	VI	0 to VEE	Vdc
Output Current — Continuous — Surge	lout	50 100	mA
Operating Temperature Range	TA	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T _{stg}	-55 to +150 -55 to +165	°C

ELECTRICAL CHARACTERISTICS (VEE = -5.2 V ± 5%) (See Note)

Characteristic	Combal	()0	2	5°	75°		Hain
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	IE.	-	126	-	115	-	126	mA
Input Current High All Except MR Pin 12 MR	linH	-	450 1190	_ _	265 700	-	265 700	μА
Input Current Low	linL	0.5	1	0.5	-	0.3	5-1	μΑ
High Output Voltage	Vон	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	VOL	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	VIH	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	VIL	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

AC PARAMETERS

Propagation Delay	t pd		974					ns
Clock to Q		0.7	3.5	0.7	3.2	0.7	3.5	St.
Clock to TC		0.7	3.5	0.7	3.2	0.7	3.5	1
MR to Q		0.7	3.5	0.7	3.0	0.7	3.5	
Set-up Time	tset					1		ns
Pn to Clock		2.0	-	2.0	1	2.0	-	
CE or PE to Clock		2.5	-	2.5	-	2.5	-	
Hold Time	thold							ns
Clock to Pn		1.0	-	1.0	-	1.0	-	
Clock to CE or PE		0.5	_	0.5	-	0.5		
Counting Frequency	fcount	200	_	200	-	200	-	MHz
Rise Time	tr	0.7	2.3	0.7	2.1	0.7	2.3	ns
Fall Time	tf	0.7	2.3	0.7	2.1	0.7	2.3	ns

NOTE

Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

This document contains information on a new product. Specifications and information herein are subject to change without notice. 2-7



4-BIT BINARY COUNTER



L SUFFIX CERAMIC PACKAGE CASE 620

P SUFFIX PLASTIC PACKAGE CASE 648



PIN ASSIGNMENT

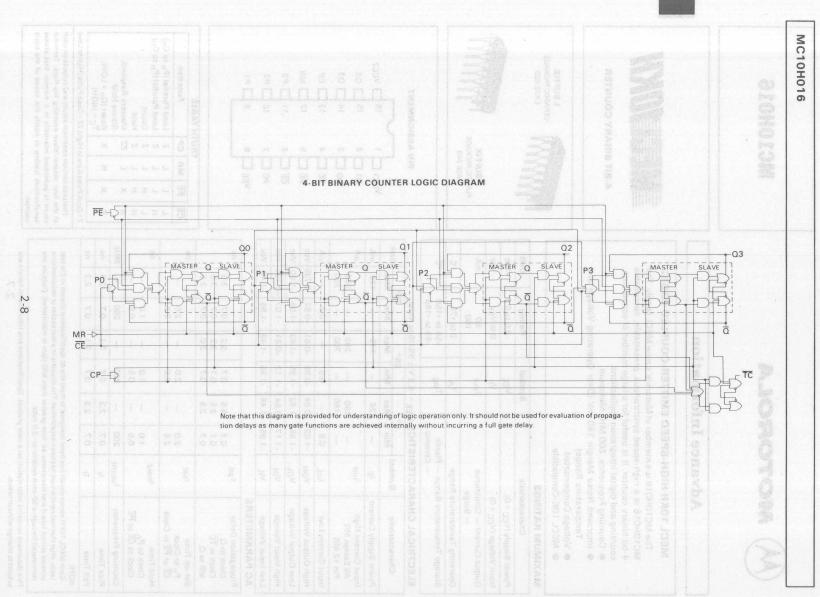


TRUTH TABLE

CE	PE	MR	СР	Function
L	L	L	Z	Load Parallel (Pn to Qn)
Н	L	L	Z	Load Parallel (Pn to Qn)
L	Н	L	Z	Count
Н	Н	L	Z	Hold
X	X	L	ZZ	Masters Respond; Slaves Hold
X	X	Н	Х	Reset ($Q_n = LOW$, $\overline{T}_C = HIGH$)

Z = Clock Pulse (Low to High); ZZ = Clock Pulse (High to Low)

Features include assertion inputs and outputs on each of the four master/slave counting flip-flops. Terminal count is generated internally in a manner that allows synchronous loading at nearly the speed of the basic counter.





Advance Information

MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

The MC10H100 is a member of Motorola's new MECL family. This MECL 10KH part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increases in power supply current.

- Propagation Delay, 1.0 ns Typical
- 25 mW Typ/Gate (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K—Compatible

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V _{CC} = 0)	VEE	-8.0 to 0	Vdc
Input Voltage (V _{CC} = 0)	VI	0 to VEE	Vdc
Output Current — Continuous — Surge	lout	50 100	mA
Operating Temperature Range	TA	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T _{stg}	-55 to +150 -55 to +165	°C

ELECTRICAL CHARACTERISTICS (VEE = -5.2 V ± 5%) (See Note)

0.2	HOTOM:	0	0	25°		75°		Unit
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	IE .	404	29	-	26	-	29	mA
Input Current High Pin 9 All Other Inputs	linH		900 500	_	560 310	8 + -	560 310	μА
Input Current Low	linL	0.5	-	0.5	uv Tau	0.3	-187	μА
High Output Voltage	VOH	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	VOL	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	VIH	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	VIL	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

AC PARAMETERS

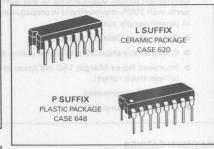
Propagation Delay	Hereta	0.5	1.5	0.5	1.5	0.5	1.7	ns
Rise Time	tr	0.5	1.9	0.5	2.0	0.5	2.3	ns
Fall Time	tf	0.5	1.7	0.5	2.0	0.5	2.0	ns

NOTE

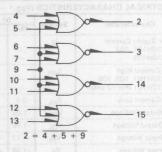
Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

This document contains information on a new product. Specifications and information herein are subject to change without notice. MECL, MECL III, MECL 10K and MECL 10KH are trademarks of Motorola Inc.









V_{CC1} = Pin 1 V_{CC2} = Pin 16 V_{EE} = Pin 8

The MC10H100 is a quad NOR gate. Each gate has 3 inputs, two of which are independent and one of which is tied common to all four gates.



MC10H101 MC10H102 MC10H105

Advance Information

MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

The MC10H101, MC10H102 and MC10H105 are members of Motorola's new MECL family. These MECL 10KH parts are functional/pinout duplications of the standard MECL 10K family parts, with 100% improvement in propagation delay, and no increases in power-supply current.

- Propagation Delay, 1 ns typical
- Power Dissipation 25 mW/Gate (same as MECL 10K)
- Improved Noise Margin 150 mV (over operating voltage and temperature range)
- Voltage Compensated
- MECL 10K-Compatible

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V _{CC} = 0)	VEE	-8.0 to 0	Vdc
Input Voltage (V _{CC} = 0)	VI	O to VEE	Vdc
Output Current — Continuous — Surge	lout	50 100	mA
Operating Temperature Range	TA	0-75	°C
Storage Temperature Range — Plastic — Ceramic	T _{stg}	-55 to 150 -55 to 165	°C

ELECTRICAL CHARACTERISTICS (VEE = -5.2 V ±5%)

OL - Control of the Control	0 1	(0	2	5°	75°		Hala
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current MC10H101, 102 MC10H105	lE.	0	29 23		26 21	1 10	29 23	mA
Input Current High MC10H101, 102, 105 MC10H101 (Pin 12 only)	linH		425 850	E	265 535	_	265 535	μА
Input Current Low	linL	0.5	_	0.5		0.3		μА
High Output Voltage	Vон	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	VOL	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	VIH	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	VIL	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

AC PARAMETERS

Propagation Delay	tpd	0.5	1.6	0.5	1.5	0.5	1.7	ns
Rise Time	tr	0.5	2.2	0.5	2.0	0.5	2.2	ns
Fall Time	t _f	0.5	2.2	0.5	2.0	0.5	2.2	ns

Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater then 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

This document contains information on a new product. Specifications and information herein are subject to change without notice

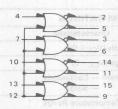




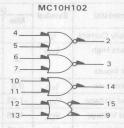
CERAMIC PACKAGE **CASE 620**





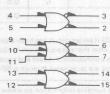


Quad OR/NOR Gate

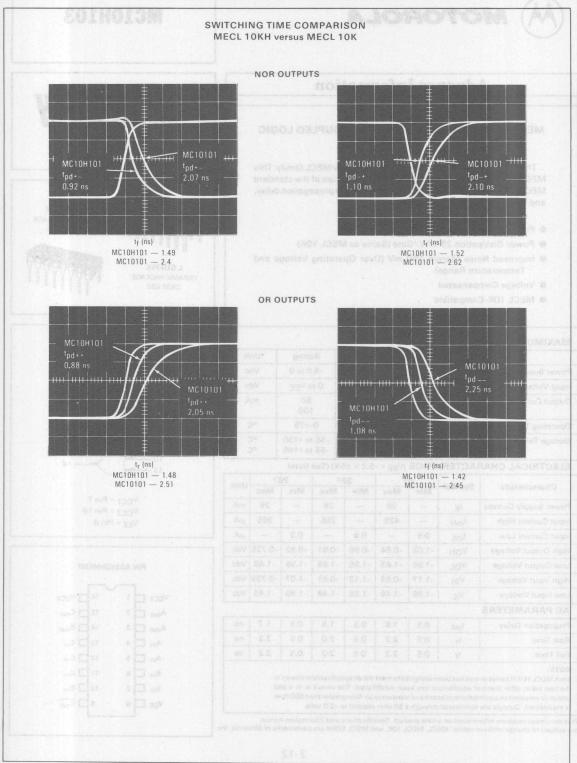


Quad 2-Input NOR Gate





Triple 2-3-2 Input OR/NOR Gate



2

Advance Information

MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

The MC10H103 is a member of Motorola's new MECL family. This MECL 10KH part is a functional/pinout duplication of the standard MECL 10K family part with 100% improvement in propagation delay, and no increases in power-supply current.

- Propagation Delay, 1.0 ns Typical
- Power Dissipation 25 mW/Gate (Same as MECL 10K)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V _{CC} = 0)	VEE	-8.0 to 0	Vdc
Input Voltage (V _{CC} = 0)	VI	0 to VEE	Vdc
Output Current — Continuous — Surge	lout	50 100	mA
Operating Temperature Range	TA	0-+75	°C
Storage Temperature Range — Plastic — Ceramic	T _{stg}	-55 to +150 -55 to +165	°C

ELECTRICAL CHARACTERISTICS (VEE = -5.2 V ±5%) (See Note)

Characteristic	0		0°		25°		75°	
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	I _E	-	29	-	26	-	29	mA
Input Current High	linH	-	425	-	265	-	265	μΑ
Input Current Low	linL	0.5	-	0.5	-	0.3	-	μΑ
High Output Voltage	Voн	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	VOL	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	VIH	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	VIL	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

AC PARAMETERS

Propagation Delay	tpd	0.5	1.6	0.5	1.5	0.5	1.7	ns
Rise Time	tr	0.5	2.2	0.5	2.0	0.5	2.2	ns
Fall Time	tf	0.5	2.2	0.5	2.0	0.5	2.2	ns

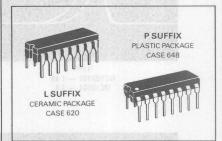
NOTE

Each MECL 10 KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50 ohm resistor to -2.0 volts.

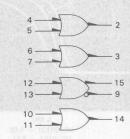
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QUAD 2-INPUT OR GATE

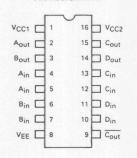






V_{CC1} = Pin 1 V_{CC2} = Pin 16 V_{EE} = Pin 8

PIN ASSIGNMENT





Advance Information

MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

The MC10H104, MC10H107 and MC10H109 are members of Motorola's new MECL family. These MECL 10KH parts are functional/pinout duplications of the standard MECL 10K family parts, with 100% improvement in propagation delay, and no increase in power-supply current.

- Propagation Delay, 1 ns Typical
- Power Dissipation 35 mW/Gate Typical (same as MECL 10K)
- Improved Noise Margin 150 mV (over operating voltage and temperature range)
- Voltage Compensated
- MECL 10K-Compatible

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V _{CC} = 0)	VEE	-8.0 to 0	Vdc
Input Voltage (V _{CC} = 0)	VI	0 to VEE	Vdc
Output Current — Continuous — Surge	lout	50 100	mA
Operating Temperature Range	TA	0-75	°C
Storage Temperature Range — Plastic — Ceramic	T _{stg}	-55 to 150 -55 to 165	°C

ELECTRICAL CHARACTERISTICS (VEE = 5.2 V ±5%) (See Note)

Characteristic	Symbol	()°	2	5°	75°		Unit
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	le le							mA
MC10H104		-	39	_	35	-	39	
MC10H107		_	31	-	28	-	31	
MC10H109	THE PERSON NAMED IN		15	1112	14	-	15	
Input Current High	linH	-	425	-	265	-	265	μΑ
Input Current Low	linL	0.5	-	0.5	=	0.3	-	μА
High Output Voltage	- VOH	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	VOL	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	VIH	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	VIL	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

AC PARAMETERS

Propagation Delay	tpd			8 7 13		PAT THE	E 1119	ns
MC10H104		0.5	2.0	0.5	1.8	0.5	2.0	
MC10H107		0.5	2.0	0.5	1.9	0.5	2.0	
MC10H109		0.5	1.6	0.5	1.5	0.5	1.7	
Rise Time	tr	0.5	2.2	0.5	2.0	0.5	2.2	ns
Fall Time	tf	0.5	2.2	0.5	2.0	0.5	2.2	ns

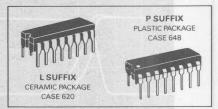
NOTE

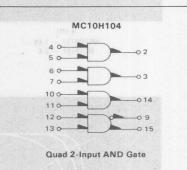
Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater then 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

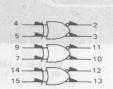
This document contains information on a new product. Specifications and information herein are subject to change without notice.

MC10H104 MC10H107 MC10H109



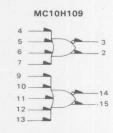






MC10H107

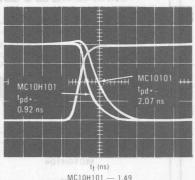
Triple 2-Input Exclusive OR/NOR Gate



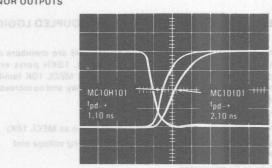
Dual 4-5 Input OR/NOR Gate

SWITCHING TIME COMPARISON MECL 10KH versus MECL 10K

NOR OUTPUTS

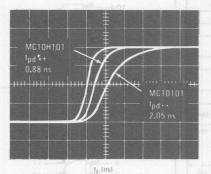


MC10H101 - 1.49 MC10101 - 2.4

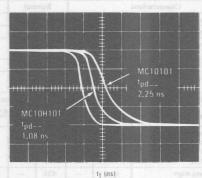


MC10H101 - 1.52 3 201 133M & MC10101 - 2.62

OR OUTPUTS



MC10H101 - 1.48 MC10101 - 2.51



MC10H101 - 1.42 MC10101 - 2.45









Advance Information

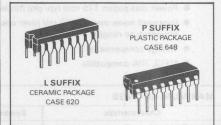
MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

The MC10H106 is a member of Motorola's new MECL family. This device is a triple 4-3-3 input NOR gate. This 10KH part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay and no increase in power-supply current.

- Propagation Delay, 1.0 ns Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible



TRIPLE 4-3-3 INPUT NOR GATE



MAXIMUM RATINGS

Symbol	Rating	Unit		
VEE	-8.0 to 0	Vdc		
VI	0 to VEE	Vdc		
lout	50 100	mA		
TA	0 - +75	°C		
T _{stg}	-55 to +150 -55 to +165	℃ ℃		
	V _{EE} V _I lout T _A	VEE -8.0 to 0 VI 0 to VEE Jout 50 100 TA 0 - +75 Tstg -55 to +150		

ELECTRICAL CHARACTERISTICS (VEE = -5.2 V ±5%) (See Note)

Symbol	0°		25°		75°		
	Min	Max	Min	Max	Min	Max	Unit
I _E	-	23	-	21	8 1 -	23	mA
linH	-	500		310	-	310	μΑ
linL	0.5	ost <u>-0</u>	0.5		0.3	-	μΑ
VOH	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
VOL	- 1.95	- 1.63	- 1.95	-1.63	- 1.95	-1.60	Vdc
VIH	-1.17	-0.84	-1.13	-0.81	- 1.07	-0.735	Vdc
VIL	-1.95	- 1.48	- 1.95	-1.48	- 1.95	- 1.45	Vdc
	IE InH InL VOH VOL VIH	Symbol Min IE	Min Max IE - 23 InH - 500	Min Max Min IE — 23 — InH — 500 — InL 0.5 — 0.5 VOH -1.02 -0.84 -0.98 VOL -1.95 -1.63 -1.95 VIH -1.17 -0.84 -1.13	Symbol Min Max Min Max IE — 23 — 21 InH — 500 — 310 InL 0.5 — 0.5 — VOH -1.02 -0.84 -0.98 -0.81 VOL -1.95 -1.63 -1.95 -1.63 VIH -1.17 -0.84 -1.13 -0.81	Min Max Min Max Min IE — 23 — 21 — InH — 500 — 310 — InL 0.5 — 0.5 — 0.3 VOH -1.02 -0.84 -0.98 -0.81 -0.92 VOL -1.95 -1.63 -1.95 -1.63 -1.95 VIH -1.17 -0.84 -1.13 -0.81 -1.07	Symbol Min Max Min Max Min Max I _E — 23 — 21 — 23 I _{InH} — 500 — 310 — 310 I _{InL} 0.5 — 0.5 — 0.3 — V _{OH} -1.02 -0.84 -0.98 -0.81 -0.92 -0.735 V _{OL} -1.95 -1.63 -1.95 -1.63 -1.95 -1.60 V _{IH} -1.17 -0.84 -1.13 -0.81 -1.07 -0.735

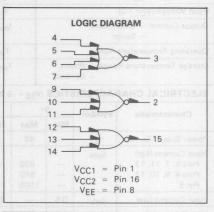
AC PARAMETERS

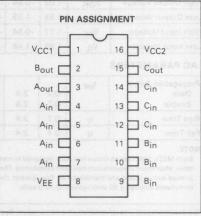
Propagation Delay	tpd	0.7	1.6	0.7	1.5	0.7	1.7	ns
Rise Time	tr	0.7	2.2	0.7	2.0	0.7	2.2	ns
Fall Time	tf	0.7	2.2	0.7	2.0	0.7	2.2	ns

NOTE

Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater through a 50-ohm resistor to -2.0 volts.

This document contains information on a new product. Specifications and information herein are subject to change without notice.









2

Advance Information

QUAD EXCLUSIVE OR GATE

The MC10H113 is a member of Motorola's new MECL family. The MC10H113 is a Quad Exclusive OR Gate with an enable common to all four gates. The outputs may be wire-ORed together to perform a 4-bit comparison function (A=B). The enable is active LOW.

- Propagation delay 1.3 ns typ.
- Power dissipation 175 mw typ/pkg (no load)
- Improved noise margin 150 mV (over operating voltage and temperature range)
- Voltage compensated
- MECL 10K-compatible

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V _{CC} = 0)	VEE	-8.0 to 0	Vdc
Input Voltage (V _{CC} = 0)	VI	0 to VEE	Vdc
Output Current — Continuous — Surge	lout	50 100	mA
Operating Temperature Range	TA	0 to +75	or 0°C
Storage Temperature Range — Plastic — Ceramic	T _{stg}	-55 to +150 -55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (VEE = -5.2 V ±5%) (See Note)

Characteristic	Symbol	C)0	2	25°		75°	
Characteriotic		Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	IE.	81	46	-	42	[8]	46	mĄ
Input Current High Pins 5, 7, 11, 13 Pins 4, 6, 10, 12 Pin 9	inH = 199	AF	430 510 1100		270 320 740		270 320 740	μА
Input Current Low	linL	0.5	_	0.5	1 100	0.3	+ "	μА
High Output Voltage	VOH	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	VOL	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	VIH	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	VIL	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

AC PARAMETERS

Propagation Delay Data Enable	tpd g	0.7	2.5	0.7	2.3	0.7	2.5	ns
Rise Time	tr	0.7	2.4	0.7	2.2	0.7	2.4	ns
Fall Time	tf	0.7	2.4	0.7	2.2	0.7	2.4	ns

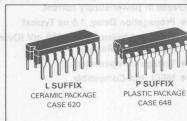
NOTE

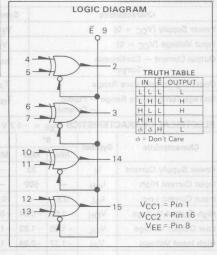
Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50 ohm resistor to –2 0 volts.

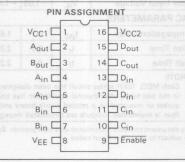
This document contains information on a new product-Specifications and information herein are subject to change without notice.



QUAD EXCLUSIVE OR GATE









QUAD LINE RECEIVER

Advance Information

MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

The MC10H115 is a member of Motorola's new MECL family. The MC10H115 is a quad differential amplifier designed for use in sensing differential signals over long lines. This MECL 10KH part is a functional/pinout duplication of the standard MECL 10K family part. with 100% improvement in counting frequency and no increase in power-supply current.

The base bias supply (VBB) is made available at Pin 9 to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necessary. Active current sources provide the MC10H115 with excellent common mode rejection. If any amplifier in a package is not used, one input of that amplifier must be connected to VBB (Pin 9) to prevent upsetting the current source bias network.

- Propagation Delay, 1.0 ns Typical
- Voltage Compensated
- Power Dissipation 110 mW Typ/Pkg (No Load) MECL 10K-Compatible
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)

- CERAMIC PACKAGE

L SUFFIX CASE 620

PLASTIC PACKAGE

CASE 648

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V _{CC} = 0)	VEE	-8.0 to 0	Vdc
Input Voltage (V _{CC} = 0)	VI	0 to VEE	Vdc
Output Current — Continuous — Surge	lout	50 100	mA
Operating Temperature Range	TA	0-+75	°C
Storage Temperature Range — Plastic — Ceramic	T _{stg}	-55 to +150 -55 to +165	°C

ELECTRICAL CHARACTERISTICS (VEE = -5.2 V ±5%) (See Note)

Characteristic	180 pt 61	00		25°		75°		
	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	E	Divide Si	29	1	26	P _ 15	29	mA
Input Current	linH	applica	150	14-	95	0/ 50	95	μА
	Ісво	HALLES BY	1.5	1-	1.0	1 - 20	1.0	μΑ
High Output Voltage	VOH	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	VOL	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	VIH	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	VIL	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc
Reference Voltage	V _{BB}	-1.38	-1.27	-1.37	-1.25	-1.31	-1.19	Vdc

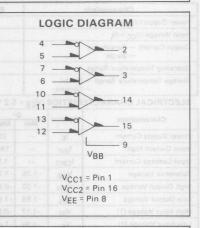
AC PARAMETERS

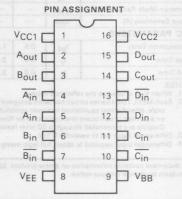
Propagation Delay	tpd	0.7	1.6	0.7	1.5	0.7	1.7	ns
Rise Time	tras	0.7	2.2	0.7	2.0	0.7	2.2	ns
Fall Time	t _f	0.7	2.2	0.7	2.0	0.7	2.2	ns

NOTE:

Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 Ifpm is maintained. Outputs are terminated through a 50 ohm resistor to -2.0 volts.

This document contains information on a new product. Specifications and information herein are subject to change without notice. 2-17





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Advance Information

MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

The MC10H116 is a member of Motorola's new MECL family. It is a functional/pinout duplication of the MC10116, with 100% improvement in propagation delay and no increase in power-supply current.

- Propagation Delay, 1 ns typical
- Power Dissipation 85 mW typ/pkg (same as MECL 10K)
- Improved Noise Margin 150 mV (over operating voltage and temperature range) (1)
- Voltage Compensated
- MECL 10K Compatible.

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (VCC = 0)	VEE	-8.0 to 0	Vdc
Input Voltage (V _{CC} = 0)	V _I	0 to VEE	Vdc
Output Current — Continuous — Surge	lout	50 100	mA MA
Operating Temperature Range	TA	0-75	°C
Storage Temperature Range — Plastic — Ceramic	T _{stg}	-55 to 150 -55 to 165	°C °C

ELECTRICAL CHARACTERISTICS (VEE = 5.2 V ±5%) (2)

Characteristic	Combal	0	0°		25°		75°	
	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	1E	-	23	-	21	29.8	23	mA
Input Current High	linH		150	-	95	-ta	95	μА
Input Leakage Current	Ісво	-	1.5	1 =	1.0	0.00	1.0	μА
Reference Voltage	VBB	-1.38	-1.27	-1.37	-1.25	-1.31	-1.19	Vdc
High Output Voltage	VOH	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	VOL	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage (1)	VIH	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage (1)	VIL	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc
Common Mode Range (3)	VCMR	-	-	-2.85 t	o -0.8	0-756	4-11	Vdc
Input Sensitivity (4)	Vpp	-	-	150) typ	10	1-18	mVpp

AC PARAMETERS

Propagation Delay	tpd	0.5	1.6	0.5	1.5	0.5	1.7	ns
Rise Time	t _r	0.5	2.2	0.5	2.0	0.5	2.2	ns
Fall Time	tf	0.5	2.2	0.5	2.0	0.5	2.2	ns

NOTES

- When VBB is used as the reference voltage
 Each MECL TOKH series circuit has been designed to meet the specifications shown in the test stable, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained.
- Outputs are terminated through a 50-ohm resistor to -2.0 volts.

 3. Differential input not to exceed 1.0 Vdc
- 4. Differential input required to obtain full logic swing on output.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

TRIPLE LINE RECEIVER



P SUFFIX
PLASTIC PACKAGE
CASE 648

MC10H116



Triple Line Receiver

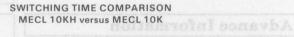
The MC10H116 is designed to be used in sensing differential signals over long lines. The bias supply (VgB) is made available to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necessary.

Active current sources provide these receivers with excellent common-mode noise rejection. If any amplifier in a package is not used, one input of that amplifier must be connected to VBB to prevent unbalancing the current-source bias network.

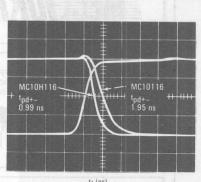
The MC10H116 does not have internal-input pull-down resistors. This provides high impedance to the amplifier input and facilitates differential connections.

Applications:

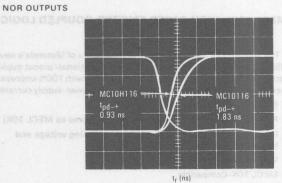
- Low Level Receiver
- Schmitt Trigger
- Voltage Level Interface



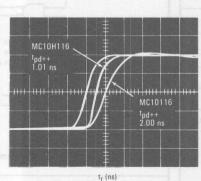
OR OUTPUTS



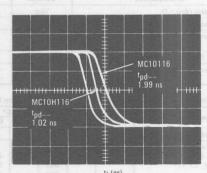
t_f (ns) MC10H116 — 1.08 MC10116 — 1.74



MC10H116 — 1.12 MC10116 — 1.86



t_r (ns) MC10H116 — 1.23 MC10116 — 1.98



t_f (ns)

MC10H116 — 1.21

MC10116 — 1.84

MC10116 — 1.84

MC10H117 MC10H118

2

Advance Information

MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

The MC10H117 and MC10H118 are members of Motorola's new MECL family. These MECL 10KH parts are functional/pinout duplications of the standard MECL 10K family parts, with 100% improvement in propagation delay, and no increase in power-supply current.

- Propagation Delay, 1 ns Typical
- Power Dissipation 100 mW/Gate Typical (same as MECL 10K)
- Improved Noise Margin 150 mV (over operating voltage and temperature range)
- Voltage Compensated
- MECL 10K-Compatible.

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit	
Power Supply (V _{CC} = 0)	VEE	-8.0 to 0	Vdc	
Input Voltage (V _{CC} = 0)	VI	0 to VEE	Vdc	
Output Current — Continuous — Surge	lout	50 100	mA	
Operating Temperature Range	TA	0-75	°C	
Storage Temperature Range — Plastic — Ceramic	T _{stg}	-55 to 150 = -55 to 165	°C	

ELECTRICAL CHARACTERISTICS (VFF = 5.2 V ±5%) (See Note)

Characteristic		()°	2	5°	7	5°	
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	1 _E		29		26		29 🤿	mA
Input Current High Pins 3*, 4, 5, 12, 13, 14* Pins 6, 7, 10, 11 Pin 9	linH		465 545 710		275 320 415		275 320 415	μΑ
Input Current Low	linL	0.5	-	0.5	-	0.3	-	μΑ
High Output Voltage	VOH	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	VOL	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	VIH	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	VIL	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

AC PARAMETERS

Propagation Delay	tpd	0.5	2.0	0.5	1.8	0.5	1.9	ns
Rise Time	tr	0.5	2.0	0.5	2.0	0.5	2.2	ns
Fall Time	tf	0.5	2.0	0.5	2.0	0.5	2.2	ns

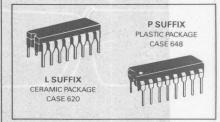
*MC10H118 only

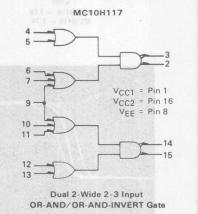
NOTE

Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater then 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

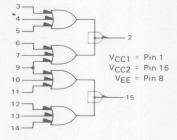
This document contains information on a new product. Specifications and information herein are subject to change without notice.











Dual 2-Wide 3-Input OR-AND Gate



MC10H119 MC10H121

Advance Information

MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

The MC10H119 and MC10H121 are members of Motorola's new MECL family. These MECL 10KH parts are functional/pinout duplications of the standard MECL 10K family parts, with 100% improvement in propagation delay, and no increase in power-supply current.

- Propagation Delay, 1 ns Typical
- Power Dissipation 100 mW/Gate Typical (same as MECL 10K)
- Improved Noise Margin 150 mV (over operating voltage and temperature range)
- Voltage Compensated
- MECL 10K-Compatible.

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit	
Power Supply (V _{CC} = 0)	VEE	-8.0 to 0		
Input Voltage (V _{CC} = 0)	V _I	0 to VEE	Vdc	
Output Current — Continuous — Surge	lout	50 100	mA	
Operating Temperature Range	TA	0-75	°C	
Storage Temperature Range — Plastic — Ceramic	T _{stg}	-55 to 150 -55 to 165	°C	

ELECTRICAL CHARACTERISTICS (VFF = 5.2 V ±5%) (See Note)

Characteristic	Combat	0)°	2	5°	7	5°	
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	1E		29		26	1001	29	mA
Input Current High Pins 3*, 4, 5, 6, 7, 9,	linH					1 681	- 01 66	μΑ
11, 12, 13, 14, 15 Pin 10	1	-	500 610		295 360	755	295 360	49
Input Current Low	linL	0.5	81-	0.5	-001	0.3	W1 + 20	μА
High Output Voltage	VOH	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	VOL	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	VIH	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	VIL	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

AC PARAMETERS

Propagation Delay	t _{pd}	0.5	2.0	0.5	2.0	0.7	1.9	ns
Rise Time	tr	0.5	2.0	0.5	2.0	0.7	2.3	ns
Fall Time	t _f	0.5	2.0	0.5	2.0	0.7	2.3	ns

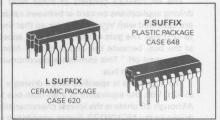
*MC10H119 only

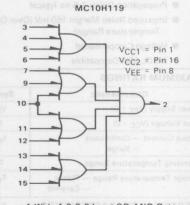
NOTE

Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater then 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

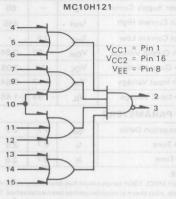
This document contains information on a new product. Specifications and information herein are subject to change without notice.







4-Wide 4-3-3-3 Input OR-AND Gate



4-Wide OR-AND/OR-AND-INVERT Gate

Advance Information

TRIPLE 4-3-3 INPUT BUS DRIVER

The MC10H123 is a member of Motorola's new MECL family. The device is a triple 4-3-3 Input Bus Driver.

The MC10H123 consists of three NOR gates designed for bus driving applications on card or between cards. Output low logic levels are specified with $V_{OL} \le -2.0$ Vdc so that the bus may be terminated to -2.0 Vdc. The gate output, when low, appears as a high impedance to the bus, because the output emitter-followers of the MC10H123 are "turned-off." This eliminates discontinuities in the characteristic impedance of the bus.

The VOH level is specified when driving a 25-ohm load terminated to -2.0 Vdc, the equivalent of a 50-ohm bus terminated at both ends. Although 25 ohms is the lowest characteristic impedance that can be driven by the MC10H123, higher impedance values may be used with this part. A typical 50-ohm bus is shown in Figure 1.

- Propagation Delay, 1.5 ns Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit	
Power Supply (V _{CC} = 0)	VEE	-8.0 to 0	Vdc	
Input Voltage (V _{CC} = 0)	VI	O to VEE	Vdc	
Output Current — Continuous — Surge	lout	50 100	mA	
Operating Temperature Range	TA	0 to +75	°C	
Storage Temperature Range — Plastic — Ceramic	T _{stg}	-55 to +150 -55 to +165	°C °C	

ELECTRICAL CHARACTERISTICS (VFF = -5.2 V ±5%) (See Note)

01		0)°	2	5°	7	5°	Unit
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	HOLENA	-	60		56	0-1-84	60	mA
Input Current High	linH -	Landing	495		310	1 1 000	310	μА
Input Current Low	linL	0.5		0.5	611	0.3	30	μА
High Output Voltage	VOH	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	VOL	-2.1	-2.03	-2.1	-2.03	-2.1	-2.03	Vdc
High Input Voltage	VIH	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	VIL	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

AC PARAMETERS

Propagation Delay	tpd	0.7	2.3	0.7	2.3	0.7	2.3	ns
Rise Time	t _r	0.7	2.5	0.7	2.5	0.7	2.5	ns
Fall Time	tf	0.7	2.5	0.7	2.5	0.7	2.5	ns

Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50 ohm resistor to -2.0 volts.

This document contains information on a new product. Specifications and information herein are subject to change without notice. 2-22



TRIPLE 4-3-3 INPUT **BUS DRIVER**

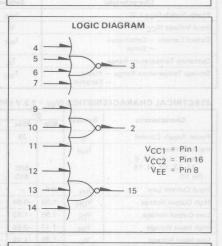


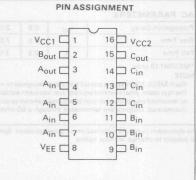
CASE 620

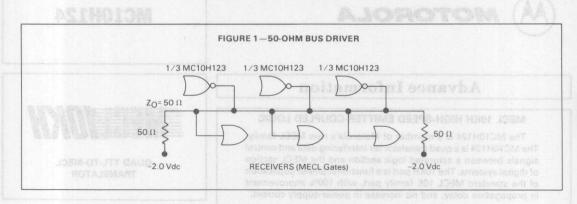




PLASTIC PACKAGE CASE 648









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Advance Information

MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

The MC10H124 is a member of Motorola's new MECL family. The MC10H124 is a quad translator for interfacing data and control signals between a saturated logic section and the MECL section of digital systems. The 10KH part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increase in power-supply current.

- Propagation Delay, 1.5 ns Typical
- Propagation Delay, 1.5 ns Typical
 Voltage Compensated
- Improved Noise Margin 150 mV
- MECL 10K-Compatible

(Over Operating Voltage and Temperature Range)

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V _{CC} = 5.0 V)	VEE	-8.0 to 0	Vdc
Power Supply (VEE = -5.2 V)	Vcc	0 to +7.0	Vdc
Input Voltage (V _{CC} = 5.0 V) TTL	VI	0 to V _{CC}	Vdc
Output Current — Continuous — Surge	lout	50 100	mA
Operating Temperature Range	TA	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T _{stg}	- 55 to + 150 - 55 to + 165	°C

ELECTRICAL CHARACTERISTICS ($V_{FF} = -5.2 \text{ V} \pm 5\%$, $V_{CC} = 5.0 \text{ V} \pm 5.0 \%$)

01			0	10	2!	5°	75	°C	
Characteristic		Symbol	Min	Max	Min	Max	Min	Max	Unit
Negative Power S Drain Current	Supply	ΙE	-	72		66	-	72	mAdd
Positive Power St	upply	Іссн	_	16	_	16	_	18	mAdd
Drain Current		ICCL	_	25	_	25		25	mAdd
Reverse Current	Pin 6 Pin 7	IR	_	200 50	=	200 50		200 50	μAdc
Forward Current	Pin 6 Pin 7	lF	=	- 12.8 - 3.2	=	- 12.8 - 3.2	_	- 12.8 - 3.2	mAdd
Input Breakdown	Voltage	V _{(BR)in}	5.5	_	5.5	-	5.5	-	Vdc
Input Clamp Volta	age	VI	_	- 1.5	-	- 1.5	1-	- 1.5	Vdc
High Output Volta	age	VOH	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Volta	ige	VOL	- 1.95	- 1.63	- 1.95	-1.63	- 1.95	-1.60	Vdc
High Input Voltag	je	VIH	2.0	_	2.0	_	2.0	_	Vdc
Low Input Voltage	е	VIL	_	0.8	_	0.8	_	0.8	Vdc

AC PARAMETERS

Propagation Delay	tpd	0.7	2.5	0.7	2.2	0.7	2.5	ns
Rise Time	tr	0.5	1.5	0.5	1.5	0.5	1.7	ns
Fall Time	tf	0.5	1.5	0.5	1.5	0.5	1.7	ns

NOTE

Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

This document contains information on a new product. Specifications and information herein are subject to change without notice. $\begin{tabular}{ll} \hline & 2-24 \\ \hline \end{tabular}$



QUAD TTL-TO-MECL TRANSLATOR

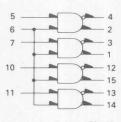


P SUFFIX PLASTIC PACKAGE CASE 648

L SUFFIX CERAMIC PACKAGE CASE 620

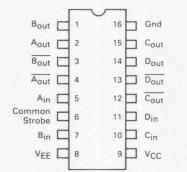


QUAD TTL-TO-ECL TRANSLATOR



 $\begin{array}{rcl} & \text{Gnd} & = & \text{Pin 16} \\ \text{V}_{CC} \ (+5.0 \ \text{Vdc}) & = & \text{Pin 9} \\ \text{V}_{EE} \ (-5.2 \ \text{Vdc}) & = & \text{Pin 8} \\ \end{array}$

PIN ASSIGNMENT

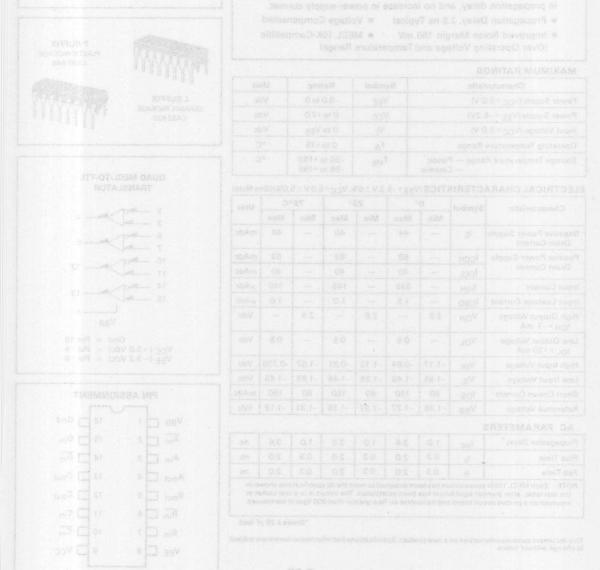


2

APPLICATIONS INFORMATION

The MC10H124 has TTL-compatible inputs and MECL complementary open-emitter outputs that allow use as an inverting/non-inverting translator or as a differential line driver. When the common strobe input is at the low-logic level, it forces all true outputs to a MECL low-logic state and all inverting outputs to a MECL high-logic state.

An advantage of this device is that TTL-level information can be transmitted differentially, via balanced twisted pair lines, to MECL equipment, where the signal can be received by the MC10H115 or MC10H116 differential line receivers. The power supply requirements are ground, +5.0 volts, and -5.2 volts.





Advance Information

MECL 10KH HIGH-SPEED EMITTER - COUPLED LOGIC

The MC10H125 is a member of Motorola's new MECL family. The MC10H125 is a quad translator for interfacing data and control signals between the MECL section and saturated logic section of digital systems. The 10KH part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increase in power-supply current.

- Propagation Delay, 2.5 ns Typical
- Voltage Compensated
- Improved Noise Margin 150 mV
 MECL 10k
 (Over Operating Voltage and Temperature Range)
- MECL 10K-Compatible

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V _{CC} = 5.0 V)	VEE	-8.0 to 0	Vdc
Power Supply (VEE = -5.2V)	Vcc	0 to +7.0	Vdc
Input Voltage (V _{CC} = 5.0 V)	VI	0 to VEE	Vdc
Operating Temperature Range	TA	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T _{stg}	-55 to +150 -55 to +165	°C

ELECTRICAL CHARACTERISTICS ($V_{EE} = -5.2 \text{ V} \pm 5\%$, $V_{CC} = 5.0 \text{ V} \pm 5.0\%$) (See Note)

Characteristic	Symbol	C	0	2	5°	75	°C	Unit
	O y moor	Min	Max	Min	Max	Min	Max	01
Negative Power Supply Drain Current	ΙE	-	44	-	40	-	44	mAdc
Positive Power Supply	Іссн	_	63	-	63	_	63	mAdc
Drain Current	ICCL	_	40	-	40	-	40	mAdc
Input Current	linH	_	225	-	145	-	145	μAdc
Input Leakage Current	Ісво	-	1.5	-	1.0	-	1.0	μAdc
High Output Voltage I _{OH} = -1 mA	Vон	2.5	-	2.5	_	2.5	-	Vdc
Low Output Voltage IOL = +20 mA	VOL	-	0.5	-	0.5	-	0.5	Vdc
High Input Voltage	VIH	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	VIL	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc
Short Circuit Current	los	60	150	60	150	60	150	mAdc
Reference Voltage	V _{BB}	-1.38	-1.27	-1.37	-1.25	-1.31	-1.19	Vdc

AC PARAMETERS

Propagation Delay*	tpd	1.0	3.6	1.0	3.6	1.0	3.6	ns
Rise Time	tr	0.3	2.0	0.3	2.0	0.3	2.0	ns
Fall Time	te	0.3	2.0	0.3	2.0	0.3	2.0	ns

NOTE: Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 ffpm is maintained.

*Drives a 25 pF load.

This document contains information on a new product. Specifications and information herein are subject to change without notice.



QUAD MECL-TO-TTL TRANSLATOR

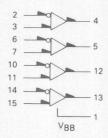


P SUFFIX PLASTIC PACKAGE CASE 648

L SUFFIX CERAMIC PACKAGE CASE 620

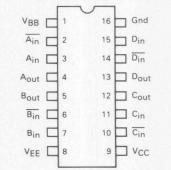


QUAD MECL-TO-TTL TRANSLATOR



 $\begin{array}{rcl} & \text{Gnd} & = & \text{Pin 16} \\ \text{V}_{CC} \ (+5.0 \ \text{Vdc}) & = & \text{Pin 9} \\ \text{V}_{EE} \ (-5.2 \ \text{Vdc}) & = & \text{Pin 8} \\ \end{array}$

PIN ASSIGNMENT



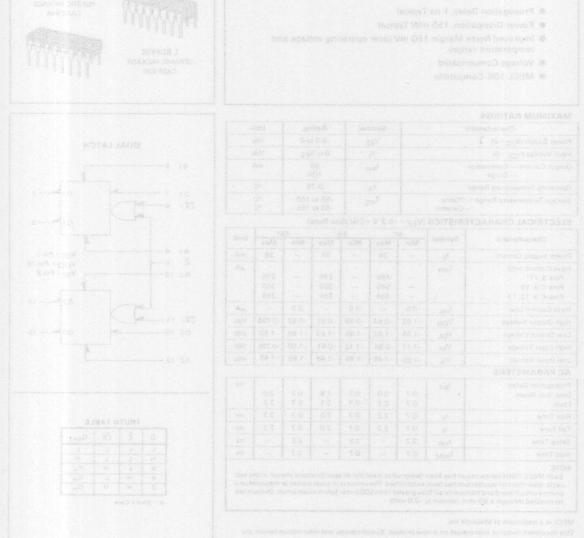
2

APPLICATION INFORMATION

The MC10H125 incorporates differential inputs and Schottky TTL "totem pole" outputs. Differential inputs allow for use as an inverting/non-inverting translator or as a differential line receiver. The VBB reference voltage is available on Pin 1 for use in single-ended input biasing. The outputs of the MC10H125 go to a low-logic

level whenever the inputs are left floating.

An advantage of this device is that MECL-level information can be received, via balanced twisted pair lines, in the TTL equipment. This isolates the MECL-logic from the noisy TTL environment. Power supply requirements are ground, +5.0 volts and -5.2 volts.



Advance Information

MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

The MC10H130 is a member of Motorola's new MECL family. This MECL 10KH part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in clock speed and propagation delay and no increase in power-supply current.

- Propagation Delay, 1 ns Typical
- Power Dissipation, 155 mW Typical
- Improved Noise Margin 150 mV (over operating voltage and temperature range)
- Voltage Compensated
- MECL 10K-Compatible



CASE 620

L SUFFIX
CERAMIC PACKAGE



P SUFFIX PLASTIC PACKAGE

CASE 648

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V _{CC} = 0)	VEE	-8.0 to 0	Vdc
Input Voltage (V _{CC} = 0)	V _I	0 to VEE	Vdc
Output Current — Continuous — Surge	lout	50 100	mA
Operating Temperature Range	TA	0-75	°C
Storage Temperature Range — Plastic — Ceramic	T _{stg}	-55 to 150 -55 to 165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2 V ±5%) (See Note)

0		0	25°		75°		Unit
Symbol	Min	Max	Min	Max	Min	Max	Unit
IE	-	38	-	35	-	38	mA
linH		468		275	_	275	μΑ
	=	545 434	_	320 255	N.T.	320 255	
linL	0.5	-	0.5	-	0.3	_	μА
VOH	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
VOL	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
VIH	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
VIL	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc
	I _{inL} VOH VOL VIH	Symbol Min IE	I _E - 38 I _{InH} - 468 - 545 - 434 I _{InL} 0.5 - VOH -1.02 -0.84 VOL -1.95 -1.63 VIH -1.17 -0.84	Symbol Min Max Min IE - 38 - InH - 468 - - 545 - - 434 - InL 0.5 - 0.5 VOH -1.02 -0.84 -0.98 VOL -1.95 -1.63 -1.95 VIH -1.17 -0.84 -1.13	Symbol Min Max Min Max I _E — 38 — 35 I _{InH} — 468 — 275 — 545 — 320 — 434 — 255 I _{InL} 0.5 — 0.5 — VOH -1.02 -0.84 -0.98 -0.81 VOL -1.95 -1.63 -1.95 -1.63 VIH -1.17 -0.84 -1.13 -0.81	Symbol Min Max Min Max Min I _E — 38 — 35 — I _{InH} — 468 — 275 — — 545 — 320 — — 434 — 255 — I _{InL} 0.5 — 0.5 — 0.3 V _{OH} -1.02 -0.84 -0.98 -0.81 -0.92 V _{OL} -1.95 -1.63 -1.95 -1.63 -1.95 V _{IH} -1.17 -0.84 -1.13 -0.81 -1.07	Symbol Min Max Min Max Min Max I _E — 38 — 35 — 38 I _{inH} — 468 — 275 — 275 — 545 — 320 — 320 — 434 — 255 — 255 I _{inL} 0.5 — 0.5 — 0.3 — VOH -1.02 -0.84 -0.98 -0.81 -0.92 -0.735 VOL -1.95 -1.63 -1.95 -1.63 -1.95 -1.60 VIH -1.17 -0.84 -1.13 -0.81 -1.07 -0.735

AC PARAMETERS

Propagation Delay	tpd							ns
Data, Set, Reset		0.7	2.0	0.7	1.8	0.7	2.0	
Clock		0.7	2.2	0.7	2.1	0.7	2.2	
Rise Time	t _r	0.7	2.2	0.7	2.0	0.7	2.2	ns
Fall Time	tf	0.7	2.2	0.7	2.0	0.7	2.2	ns
Setup Time	tset	2.2	-	2.2	-	2.2	-	ns
Hold Time	thold	0.7	-	0.7	-	0.7	-	ns

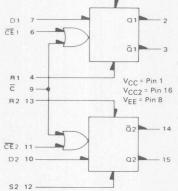
NOTE

Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater then 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

MECL is a trademark of Motorola Inc.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

DUAL LATCH



TRUTH TABLE

D	Ē	СE	Q _{n+1}
L	L	L	L
н	L	L	н
Φ	L	н	an
Φ	н	L	Qn
0	Н	Н	an

φ · Don't Care

2

APPLICATION INFORMATION

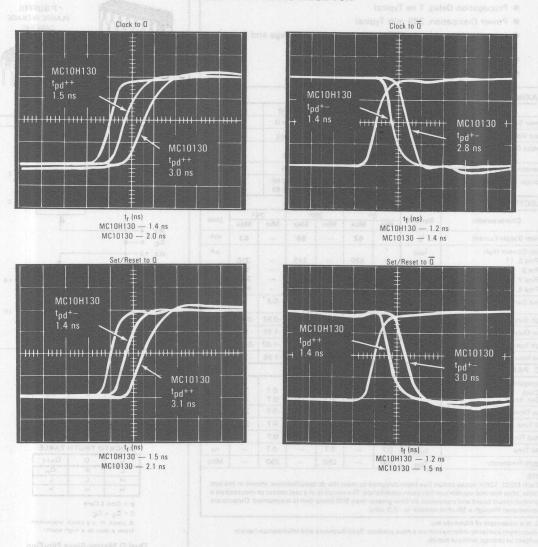
The MC10H130 is a clocked dual D type latch. Each latch may be clocked separately by holding the common clock in the low state, and using the clock enable inputs for the clocking function. If the common clock is to be used to clock the latch, the clock enable $\overline{(CE)}$ inputs must be in the low state. In this mode, the enable inputs perform the function of controlling the common clock $\overline{(C)}$.

Any change at the D input will be reflected at the output

while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information.

The set and reset inputs do not override the clock and D inputs. They are effective only when either \overline{C} or \overline{CE} or both are high.

SWITCHING TIME COMPARISON MECL 10KH versus MECL 10K



2

Advance Information

MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

The MC10H131 is a member of Motorola's new MECL family. This MECL 10KH part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in clock speed and propagation delay and no increase in power-supply current.

- Propagation Delay, 1 ns Typical
- Power Dissipation, 235 mW Typical
- Improved Noise Margin 150 mV (over operating voltage and temperature range)
- Voltage Compensated
- MECL 10K-Compatible

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V _{CC} = 0)	VEE	-8.0 to 0	Vdc
Input Voltage (V _{CC} = 0)	VI	0 to VEE	Vdc
Output Current — Continuous — Surge	lout	50 100	mA
Operating Temperature Range	TA	0-75	°C
Storage Temperature Range — Plastic — Ceramic	T _{stg}	-55 to 150 -55 to 165	°C °C

ELECTRICAL CHARACTERISTICS (VEE = -5.2 V ±5%) (See Note)

Characteristic	C	()°	2	5°	75°		Unit
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	THE ME	7174	62	-	56	-	62	mA
Input Current High Pins 6, 11	linH	lu-	530	_	310		310	μΑ
Pin 9			660	STEELS.	390	-	390	
Pins 7, 10 Pins 4, 5, 12, 13		=	485 790	_	285 465	=	285 465	
Input Current Low	linL	0.5	M-	0.5	-	0.3	700	μА
High Output Voltage	VOH	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	VOL	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	VIH	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	VIL	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

AC PARAMETERS

Propagation Delay Clock Set, Reset	t _{pd}	0.7 0.7	2.0	0.7	2.0 2.0	0.7 0.7	2.1	ns
Rise Time	t _r	0.7	2.3	0.7	2.3	0.7	2.5	ns
Fall Time	tf	0.7	2.3	0.7	2.3	0.7	2.5	ns
Setup Time	tset	0.7	_	0.7		0.7	- 46	ns
Hold Time	thold	0.7	_	0.7	-	0.7	-	ns
Toggle Frequency	f _{tog}	250	-	250	-	250	-	MHz

NOTE

Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater then 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to –2.0 volts.

MECL is a trademark of Motorola Inc.

This document contains information on a new product. Specifications and information herein are subject to change without notice.



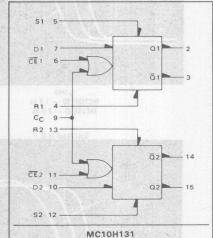
DUAL TYPE D MASTER-SLAVE FLIP FLOP



P SUFFIX PLASTIC PACKAGE CASE 648

L SUFFIX CERAMIC PACKAGE CASE 620





MCTUHTST

RS TRUTH TABLE

R	S	Qn+1
L	L	an
L	н	Н
Н	L	L
н	Н.	N.D.

CLOCKED TRUTH TABL

CLUCKE	DINUI	HIMBLE
С	D	Q _{n+1}
L	Φ	Qn
Н	L	L
Н	Н	Н

φ = Don't Care

C = CE + CC

A clock H is a clock transition from a low to a high state.

Dual D Master-Slave Flip-Flop

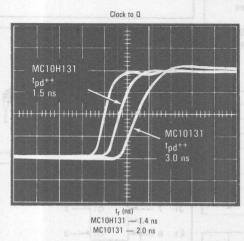
APPLICATION INFORMATION

The MC10H131 is a dual master-slave type D flip-flop. Asynchronous Set (S) and Reset (R) override Clock (C_C) and Clock Enable (CE) inputs. Each flip-flop may be clocked separately by holding the common clock in the new low state and using the enable inputs for the clocking function. If the common clock is to be used to clock the flip-flop, the Clock Enable inputs must be in the low state.

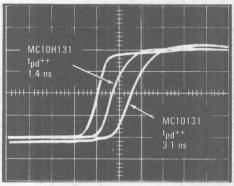
In this case, the enable inputs perform the function of controlling the common clock.

The output states of the flip-flop change on the positive transition of the clock. A change in the information present at the data (D) input will not affect the output information at any other time due to master slave construction.

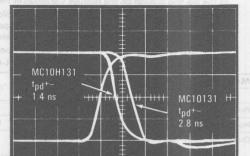
SWITCHING TIME COMPARISON MECL 10KH versus MECL 10K



Set/Reset to Q



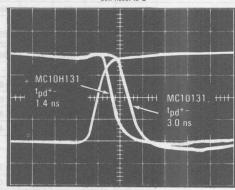
 $t_{\rm f}$ (ns) MC10H131 — 1.5 ns MC10131 — 2.1 ns



Clock to Q

t_r (ns) MC10H131 — 1.2 ns MC10131 — 1.4 ns

Set/Reset to Q



 $t_{\rm f}$ (ns) MC10H131 — 1.2 ns MC10131 — 1.5 ns



Advance Information

DUAL J-K MASTER SLAVE FLIP-FLOP

The MC10H135 is a member of Motorola's new MECL family. The MC10H135 is a dual J-K master slave flip-flop. The device is provided with an asynchronous set(s) and reset(R). These set and reset inputs overide the clock.

A common clock is provided with separate J-K inputs. When the clock is static, the \overline{JK} inputs do not effect the output. The output states of the flip flop change on the positive transition of the clock.

- Power Dissipation, 280 mW Typical/Pkg. (No Load)
- ftog 250 MHz Max
- Propagation Delay, 1.5 ns Typical
 Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
 - Voltage Compensated
 - MECL 10K-Compatible

MAN VIRALINA DATINICO

Characteristic	Symbol	Rating	Unit
Power Supply (V _{CC} = 0)	VEE	-8.0 to 0	Vdc
Input Voltage (V _{CC} = 0)	VI	O to VEE	Vdc
Output Current — Continuous — Surge	lout	50 100	mA
Operating Temperature Range	TA	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T _{stg}	-55 to +150 -55 to +165	°C

ELECTRICAL CHARACTERISTICS (VEE = -5.2 V ±5%) (See Note)

Characteristic	Symbol	()°	25°		75°		Unit
	Total teast	Min	Max	Min	Max	Min	Max	0
Power Supply Current	ΙE	1 - 11	75	i - 10	68	_	75	mA
Input Current High Pins 6, 7, 10, 11 Pins 4, 5, 12, 13 Pin 9	linH	_ 	460 800 675	- - -	285 500 420		285 500 420	μА
Input Current Low	linL	0.5	-	0.5	11-	0.3	- 60	μА
High Output Voltage	Vон	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	VOL	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	VIH	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	VIL	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

AC PARAMETERS

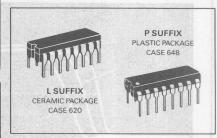
Propagation Delay	tpd							ns
Set, Reset, Clock		0.7	2.6	0.7	2.3	0.7	2.6	1000
Rise Time	t _r	0.7	2.2	0.7	2.0	0.7	2.2	ns
Fall Time	tf	0.7	2.2	0.7	2.0	0.7	2.2	ns
Set-up Time	t _{set}	1.5	- 4	1.5	_	1.5	_	ns
Hold Time	thold	1.0		1.0	_	1.0	_	ns
Toggle Frequency	f _{toq}		250		250		250	MHz

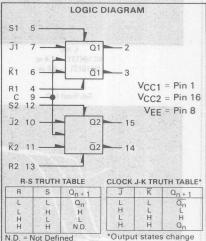
Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50 ohm resistor to -2.0 volts.

This document contains information on a new product. Specifications and information herein are subject to change without notice. 2-32

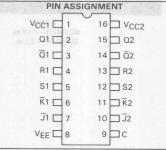


DUAL J-K MASTER SLAVE FLIP-FLOP





on positive transition of clock for J-K input condition present.





Advance Information

MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

The MC10H136 is a member of Motorola's new MECL family. The MC10H136 is a high speed synchronous hexadecimal counter. This 10KH part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in counting frequency and no increase in power-supply current.

- Counting frequency, 250 MHz minimum
- Voltage Compensated
- Power Dissipation, 625 mW Typical
- MECL 10K-Compatible
- Improved Noise Margin 150 mV (over operating voltage and temperature range)

MAXIMUM BATINGS

MAXIMOM HATHEO								
Characteristic	Symbol	Rating	Unit					
Power Supply (V _{CC} = 0)	VEE	-8.0 to 0	Vdc					
Input Voltage (V _{CC} = 0)	V _I	0 to VEE	Vdc					
Output Current — Continuous — Surge	lout	50 100	mA					
Operating Temperature Range	TA	0-75	°C					
Storage Temperature Range — Plastic — Ceramic	T _{stg}	-55 to 150 -55 to 165	°C °C					

ELECTRICAL CHARACTERISTICS (VFF = -5.2 V ±5%) (See Note)

01		0	0	25°		75°		194.
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	I _E	-	165	TOTAL	150	LIMO	165	mA
Input Current High Pins 5, 6, 11, 12, 13 Pin 9 Pin 7	1000	8-101q	430 670 535	54 <u>7</u> ,18 at <u>nu</u> d	275 420 335	-	275 420 335	μΑ
Pin 10 Ped to Auditamiol	ni odi di		380	I ban	240	-	240	blo
Input Current Low	linL	0.5	A 4	0.5	BID_BIT	0.3	16700	μА
High Output Voltage	VOH	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	VOL	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	VIH	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	VIL	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

AC PARAMETERS

Propagation Delay	tpd				STORY IS			ns
Clock to Q		0.7	3.5	0.7	3.2	0.7	3.5	
Clock to Carry Out		0.7	7.7	0.7	7.0	0.7	7.7	
Carry in to Carry Out		0.7	3.5	0.7	3.0	0.7	3.5	100
Set-up Time	tset							ns
Data (DO to C)		2.0	-	2.0	-	2.0	-	
Select (S to C)		3.5	_	3.5	-	3.5	_	1
Carry In (Cin to C)		2.0	_	2.0	_	2.0	_	
(C to Cin)		0	-	0	-	0	-	
Hold Time	thold						No. of The	ns
Data (C to DO)	1.0.0	0	- 3	0	-	0	_	
Select (C to S)		-0.5	_	-0.5	-	-0.5	- 1	
Carry In (C to Cin)		0	-	0	-	0	_	
(Cin to C)		2.2	-	2.2	-	2.2	-	
Counting Frequency	fcount	250	-	250	-	250	-	MHz
Rise Time	t _r	0.7	2.3	0.7	2.1	0.7	2.3	ns
Fall Time	tf	0.7	2.3	0.7	2.1	0.7	2.3	ns

Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater then 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.



UNIVERSAL HEXADECIMAL COUNTER



P SUFFIX PLASTIC PACKAGE CASE 648

LSUFFIX CERAMIC PACKAGE CASE 620



FUNCTION SELECT TABLE

CIN	S1	S2	Operating Mode
φ	L	L	Preset (Program)
L	L.	Н	Increment (Count Up)
Н	L	Н	Hold Count
L	Н	L	Decrement (Count Down)
Н	Н	L	Hold Count
φ	н	H	Hold (Stop Count)

SEQUENTIAL TRUTH TABLE*

_	INPUTS							OUTPUTS					
S1	52	DO	D1	D2	D3	Carry	Clock	00	01	02	Q3	Carry	
L	L	L	L	н	н	Φ	н	L	L	н	н	L	
L	н	0	0	0	0	L	н	н	L	н	н	н	
L	H	0	0	0	Φ	L	н	L	н	н	н	н	
L	н	0	0	0	0	L	н	н	н	н	н	L	
L	н	0	0	0	0	н	L	н	н	н	н	н	
L	н	0	0	0	0	н	н	н	н	н	н	н	
H	H	0	0	0	0	Φ	н	н	н	н	н	н	
L	L	н	н	L	L	0	н	н	н	L	L	L	
н	L	Φ	0	0	Φ	L	н	L	н	L	L	н	
H	L	Φ	0	Φ	Φ	L	H	H	L	L	L	н	
H	L	0	0	0	Φ	L	H	L	L	L	L	L	
H	L	0	0	0	0	L	H	н	н	H	н	H	

- O = Don't care

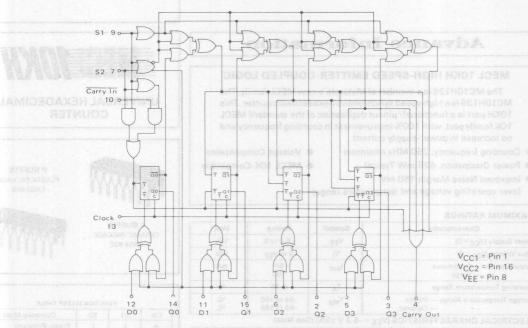
 * Truth table shows logic states assuming inputs vary in sequence shown from top to bottom.

 * A clock H is defined as a clock input transition from a low to a high logic level.

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This document contains information on a new product. Specifications and information herein are subject to change without notice.

HEXADECIMAL COUNTER



NOTE: FLIP FLOPS WILL TOGGLE WHEN ALL TINPUTS ARE LOW.

APPLICATION INFORMATION

The MC10H136 is a high speed synchronous counter that operates at 250 MHz. Counter operating modes include count up, count down, pre-set and hold count. This device allows the designer to use one basic counter for many applications.

The S1, S2, control lines determine the operating modes of the counter. In the pre-set mode, a clock pulse is necessary to load the counter with the information present on the data inputs (D0, D1, D2, and D3). Carry out goes low on the terminal count or when the counter is being pre-set.



Advance Information

MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

The MC10H141 is a four-bit universal shift register. This device is a functional/pinout duplication of the standard MECL 10K part with 100% improvement in propagation delay and operation frequency and no increase in power supply current.

- Shift frequency, 250 MHz Min
- Power Dissipation, 425 mW Typical
- Improved Noise Margin 150 mV (over operating voltage and temperature range)
- Voltage Compensated
- MECL 10K-Compatible

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V _{CC} = 0)	VEE	-8.0 to 0	Vdc
Input Voltage (VCC = 0)	VI	0 to VEE	Vdc
Output Current — Continuous — Surge	lout	50 100	mA
Operating Temperature Range	TA	0-75	°C
Storage Temperature Range — Plastic — Ceramic	T _{stg}	-55 to 150 -55 to 165	℃ ℃

ELECTRICAL CHARACTERISTICS (VEE = -5.2 V ± 5%)

		0)°	2	5°	7		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	IE.		112	P3478	102	DUNE.	112	mA
Input Current High Pins 5, 6, 9, 11, 12, 13 Pin 7,10 Pin 4	linH te ere ere T este to y	ip m sti st <u>en</u> tr	405 416 510	k: *Ne nt. <u>8</u> nd	255 260 320	12 — 12 —	255 260 320	μА
Input Current Low	linL	0.5	THE RES	0.5	THE PERSON	0.3	-25	μΑ
High Output Voltage	VOH	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	VOL	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	VIH	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	VIL	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

AC PARAMETERS

Propagation Delay	tpd	1.1	2.0	1.0	1.9	1.1	2.1	ns
Hold Time	thold	1.0	-	1.0	_	1.0	-	ns
Set up Time Data Select	t _{set}	1.5 3.0	=	1.5 3.0	=	1.5 3.0	_	ns
Rise Time Fall Time	t _r	0.7 0.7	2.4 2.3	0.7 0.7	2.2	0.7 0.7	2.4 2.4	ns
Shift Frequency	fshift	250	-	250	_	250	_	MH

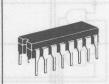
NOTE

Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

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MC10H141

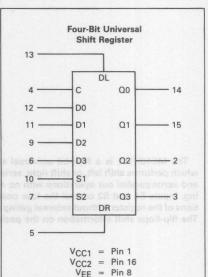




P SUFFIX PLASTIC CASE CASE 648



L SUFFIX CERAMIC CASE CASE 620

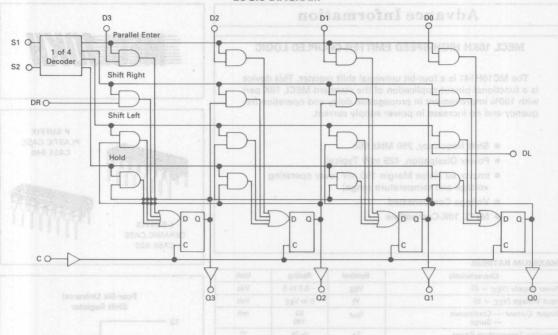


TRUTH TABLE

SEL	ECT	OPERATING	OUTI	PUTS		
S1	S2		Q0 _{n+1}	Q1 _{n+1}	Q2 _{n+1}	Q3 _{n+1}
L	L	Parallel Entry	D0	D1	D2	D3
L	Н	Shift Right*	Q1 _n	Q2 _n	Q3 _n	DR
Н	L	Shift Left*	DL	Q0 _n	Q1 _n	Q2 _n
Н	Н	Stop Shift	Q0 _n	Q1 _n	Q2 _n	Q3 _n

 Outputs as exist after pulse appears at "C" input with input conditions as shown (Pulse Positive transition of clock input).

LOGIC DIAGRAM



APPLICATION INFORMATION

The MC10H141 is a four-bit universal shift register which performs shift left, or shift right, serial/parallel in, and serial/parallel out operations with no external gating. Inputs S1 and S2 control the four possible operations of the register without external gating of the clock. The flip-flops shift information on the positive edge of

the clock. The four operations are stop shift, shift left, shift right, and parallel entry of data. The other six inputs are all data type inputs; four for parallel entry data, and one for shifting in from the left (DL) and one for shifting in from the right (DR).



Advance Information

MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

The MC10H145 is a member of Motorola's new MECL family. The MC10H145 is a 16×4 bit register file. The active-low chip select allows easy expansion.

The operating mode of the register file is controlled by the \overline{WE} input. When \overline{WE} is "low" the device is in the write mode, the outputs are "low" and the data present at D_n input is stored at the selected address, when \overline{WE} is "high", the device is in the read mode — the data state at the selected location is present at the Q_n outputs.

- Address Access Time, 3.5 ns Typical
- Power Dissipation, 700 mW Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V _{CC} = 0)	VEE	-8.0 to 0	Vdc
Input Voltage (V _{CC} = 0)	VI	0 to VEE	Vdc
Output Current — Continuous — Surge	lout	50 100	mA
Operating Temperature Range	TA	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T _{stg}	-55 to +150 -55 to +165	°C

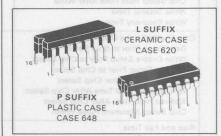
ELECTRICAL CHARACTERISTICS (VEE = -5.2 V ± 5%) (See Note)

Characteristic	0 1 1	0°		25°		7	Hais	
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	IE.	-	165	X-	150	-	165	mA
Input Current High	linH	-	375	-	220	-	220	μΑ
Input Current Low	linL	0.5		0.5		0.3		μΑ
High Output Voltage	VOH	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	VOL	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	VIH	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	VIL	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

NOTE

Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.









TRUTH TABLE

MODE	15.5	INPUT		OUTPUT
- 85	CS	WE	Dn	Qn
Write "0"	L	L	L	L
Write "1"	L	L	Н	L
Read	L	Н	φ	Q
Disabled	Н	φ	φ	L

 ϕ = Don't Care

Q-State of Addressed Cell

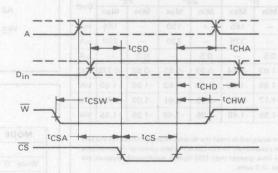
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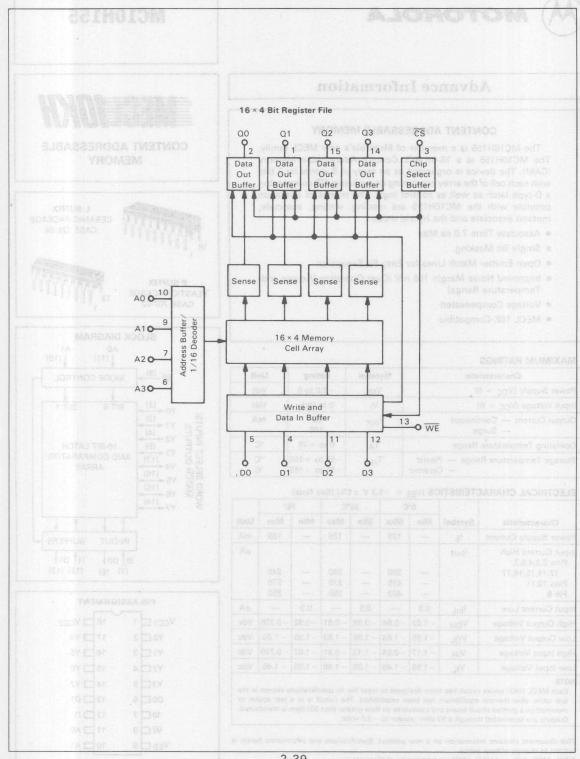
	MC10H145 T _A = 0 to +75°C, V _{EE} = -5.2 Vdc ±5%				
Characteristics	Symbol	Min	Max	Unit	Conditions
Read Mode Chip Select Access Time Chip Select Recovery Time Address Access Time	tACS tRCS tAA	1.0 1.0 2.0	3.0 3.0 5.0	ns	Measured from 50% of input to 50% of output. See Note 2.
Write Mode Write Pulse Width Data Setup Time Prior to Write Data Hold Time After Write Address Setup Time Prior to Write Address Hold Time After Write Chip Select Setup Time Prior to Write Chip Select Hold Time After Write Write Disable Time Write Recovery Time	tW tWSD tWHD tWSA tWHA tWSCS tWHCS tWS tWR	3.5 0.5 0 1.5 1.0	4.0	er file. I sere file sere in i Og ingli device i	tWSA = 3.5 ns Measured at 50% of input to 50% of output. tW = 4.0 ns.
Chip Enable Strobe Mode Data Setup Prior to Chip Select Write Enable Setup Prior to Chip Select Address Setup Prior to Chip Select Data Hold Time After Chip Select Write Enable Hold Time After Chip Select Address Hold Time After Chip Select Chip Select Minimum Pulse Width	tCSD tCSW tCSA tCHD tCHW tCHA tCS	0 0 0 1.0 0 2.0	y ent to and	ns leavey heate	Guaranteed but not tested on standard product. See Figure 1.
Rise and Fall Time Address to Output CS to Output	t _r , t _f	0.6 0.6	2.5 2.5	ns	Measured between 20% and 80% points.
Capacitance Input Capacitance Output Capacitance	C _{in} C _{out}	Rusing	6.0	pF	Measured with a pulse technique.

NOTES: 1. Test circuit characteristics: $R_T = 50 \,\Omega$, MC10H145. $C_L \le 5.0 \,\text{pF}$ (including jig and Stray Capacitance). Delay should be derated 30 ps/pF for capacitive loads up to 50 pF.

- 2. The maximum Address Access Time is guaranteed to be the worst-case bit in the memory.
- 3. For proper use of MECL in a system environment, consult MECL System Design Handbook.

FIGURE 1 — CHIP ENABLE STROBE MODE





2

Advance Information

CONTENT ADDRESSABLE MEMORY

The MC10H155 is a member of Motorola's new MECL family. The MC10H155 is a 16-bit ECL Content Addressable Memory (CAM). The device is organized as an array of 8 words by 2 bits with each cell of the array containing an exclusive-OR comparator, a D-type latch as well as control logic. The modes of operation possible with the MC10H155 are reading, writing, associate, masked associate and the hybrid mode.

- Associate Time 7.0 ns Max
- Single Bit Masking
- Open Emitter Match Lines for Easy Bit Expansion
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

MAXIMUM RATINGS

MAXIMOM HATHEGO			
Characteristic	Symbol	Rating	Unit
Power Supply (V _{CC} = 0)	VEE	- 8.0 to 0	Vdc
Input Voltage (V _{CC} = 0)	VI	0 to VEE	Vdc
Output Current — Continuous — Surge	lout	50 100	mA
Operating Temperature Range	TA	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T _{stg}	- 55 to + 150 - 55 to + 165	°C

ELECTRICAL CHARACTERISTICS (VFF = -5.2 V ±5%) (See Note)

		0	°C	25°C		75°			
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit	
Power Supply Current	ΙE	_	135	-	125	_	135	mA	
Input Current High Pins 2,3,4,5,7, 12,14,15,16,17 Pins 10,11 Pin 8	linH	_	380 435 400	_ _ _	240 270 250		240 270 250	μΑ	
Input Current Low	linL	0.5	_	0.5	_	0.3	_	μΑ	
High Output Voltage	VOH	- 1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc	
Low Output Voltage	VOL	- 1.95	-1.63	- 1.95	- 1.63	- 1.95	-1.60	Vdc	
High Input Voltage	V _{IH}	-1.17	- 0.84	- 1.13	-0.81	- 1.07	-0.735	Vdc	
Low Input Voltage	VIL	- 1.95	- 1.48	- 1.95	- 1.48	- 1.95	- 1.45	Vdc	

NOTE:

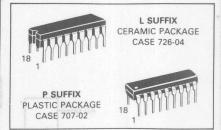
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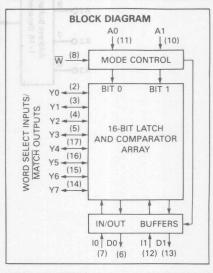
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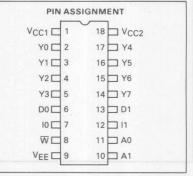
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CONTENT ADDRESSABLE MEMORY







AC PARAMETERS

			(ollat si	25°		75°C		The MC	
Characteristic		esb to	Min	Max	Min	Max	Min	Max	Unit	
Associate Time	(I to Y) (A to Y)	TA1 TA2	= 3	6.0 6.0	isb <u>orn</u> s	6.0 6.0	ent ni to	7.0 7.0	ns	
Disable Time	(A to D)	TD1 TD2 TD3	=	6.0 4.0 6.5		6.0 4.0 6.5		7.0 5.0 7.0	. ns	
Setup Time pro-11 -Ol edi te massiq etali	$(Y \text{ to } \overline{W})$	TS2 TS3 TS4	_ :	8.0 3.0 4.0	Dearling	8.0 3.0 4.0	its (Unit), u state s has V.lis	9.0 4.0 5.0	ns	
Write Pulse Width Write Access Time TS4 ≥ TW TS4 ≥ TW	(W to D)	TW TA3 TA4	- h	8.0 8.0 6.0	ia r im ios PHOTON	8.0 8.0 6.0	entiter s gmyly	9.0 9.0 7.0	ns	
Hold Time	(W/to A) (W/to Y) (W/to I)	7.4. 1. 10 Carlot at 1	= ,	1.0 3.0 3.0		1.0 3.0 3.0	dt vilke i	1.5 4.0 4.0	ns	
Read Access Time TS4 ≥ TW TS4 ≥ TW	(Y to D) (A to D)	territoria.	— 1 — 0	5.0 4.0	ono q an diy d ba	5.0 4.0	ligr ii) d y sid lig rist	6.0 5.0	ns	
Cycle Time, CP Rate	ent eA .w	ol og	40	_	40	- W <u>ee</u> 1 61	35	-OA_path	MHz	

TOUTH TABLE

Mode	A0	A1	10	11	W	D0	D1	Qn0	Qn1	of auguso lie Yn luoires on T
Associate ¹	1	1	1/0	1/0	X	0	0	Qn0	Qn1	Qn0 ⊕ I0 + Qn1 ⊕ I1
Associate ^{1,2} (Masked)	1	0	1/0	Х	1	0	D1	Qn0	Qn1	Qn0 ⊕ 10
Associate ^{1,2} (Masked)	0	.1	X	1/0	OHV.	D0	0	Qn0	Qn1	Qn1 ⊕ I1
Read ^{2,3}	0	0	X	X	1	D0	D1	Qn0	Qn1	0 (Selected Address)
Write ^{3,4}	0	0	1/0	1/0	0	10	11	10	11	0 (Selected Address)
Hybrid ⁵	1	0	1/0	1/0	0	0	- 11	Qn0	I1∙₹n	Qn0 ⊕ 10
Hybrid ⁵	0	1	1/0	1/0	0	10	0	I0∙Ÿn	Qn1	Qn1 ⊕ I1

X = Don't Care

Qn0 = Contents of Address n, Bit 0 (n = 0 to 7)

Qn1 = Contents of Address n, Bit 1

NOTES:

- 1. 1 (High) = Mismatch of Qn \oplus I, 0 (Low) = Match of Qn \oplus I 2. D0 = Q00 \cdot \overrightarrow{Y} 0 + Q10 \cdot \overrightarrow{Y} 1 + \cdot \cdot + Q70 \cdot \overrightarrow{Y} 7 D1 = Q01 \cdot \overrightarrow{Y} 0 + Q11 \cdot \overrightarrow{Y} 1 + \cdot \cdot + Q71 \cdot \overrightarrow{Y} 7
- 3. Under normal operation, only one Y address is selected for read or write.
- 4. The write is transparent.
- 5. At all "matched" addresses there exists a simultaneous Associate and Write.

The MC10H155 can be operated in any of the following modes: Read, Write, Associate, Masked Associate and Hybrid. Lines Y0-Y7 can be used as either inputs (a linear word select in the read/write mode) or as outputs (indicating match/mismatch in the associate mode).

Associate

Data present on the I0 and I1 inputs are compared with the latch outputs (Qn0, Qn1) of each cell. If the data input is at the same state as the latch output of a particular Y location, that Y-line goes low. Because these Y outputs are open emitters, expansion in multiples of 2 bits is obtained by tying additional MC10H155's to the Y-bus lines.

Masked Associate

This mode allows only the comparison of a single bit which is selected by bringing the corresponding A0- or A1-line high. The other bit is inhibited by holding the corresponding A0- or A1-line low.

Read

The particular cell output to be read is selected by bringing the associated Y-input low. Under normal op-

eration only one cell is selected to be read, all Y-inputs of deselected cells must be held high. The state of the selected cell appears on outputs D0 and D1. In the case where more than one cell is selected, the outputs of these cells are OR-ed together and appear on the D0-, D1-outputs.

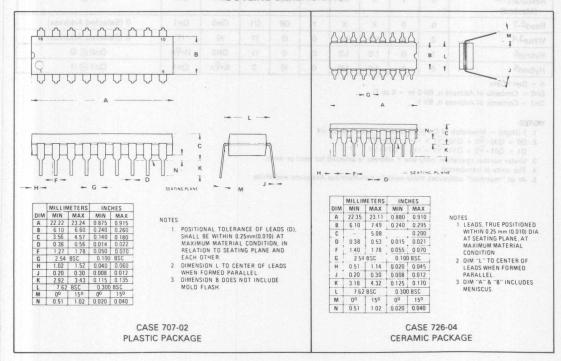
Write

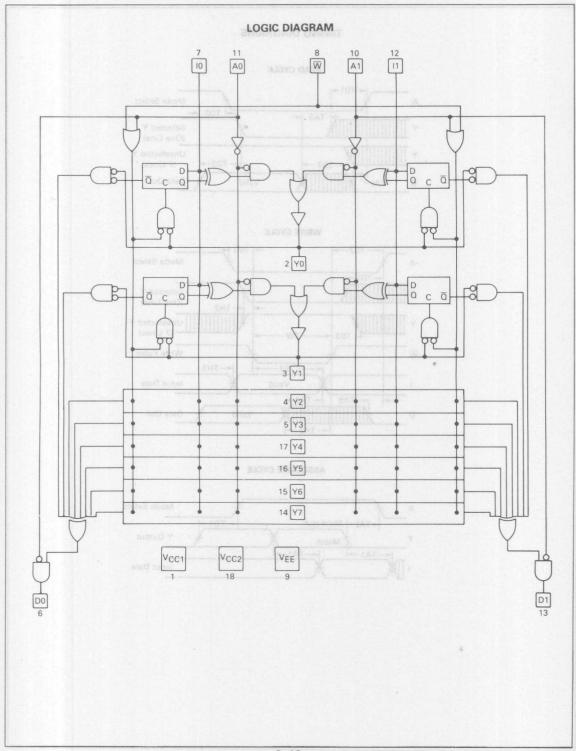
In this mode data present at the I0-, I1-inputs is transferred to the latch outputs. Since the D0-, D1-outputs are transparent, they follow the state of these I0-, I1-inputs. The particular cells to be written into are selected by taking their respective Y-inputs low. All deselected cells, Y-inputs must be held high.

Hybrid

In this mode, only one of the I0- or I1-data inputs are associated with their respective latch outputs, Qn0 or Qn1. If a match exists, the corresponding Yn-line(s) will go low. As the Y-line goes low, this will address the other half of the memory for writing new data. Thus, when I0 matches Qn0, it is possible to write I1 in Qn1 or vice versa.

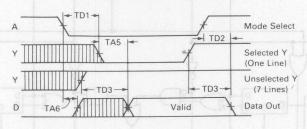
OUTLINE DIMENSIONS



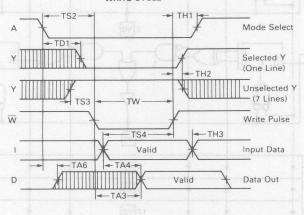


TIMING DIAGRAMS

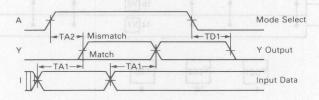




WRITE CYCLE



ASSOCIATE CYCLE





Advance Information

MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

The MC10H158 is a member of Motorola's new MECL family. The MC10H158 is a quad two channel multiplexer with common input select. A "high" level select enables input D00, D10, D20 and D30 and a "low" level select enables input D01, D11, D21 and D31. This MECL 10KH part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay and no increase in power-supply current.

- Propagation Delay, 1.5 ns Typical
- Power Dissipation, 197 mW Typical
- Improved Noise Margin 150 mV (over operating voltage and temperature range)
- Voltage Compensated
- MECL 10K-Compatible

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V _{CC} = 0)	VEE	-8.0 to 0	Vdc
Input Voltage (V _{CC} = 0)	ros VI	O to VEE	Vdc
Output Current — Continuous — Surge	lout	50 100	mA
Operating Temperature Range	TA	0-75	°C
Storage Temperature Range — Plastic — Ceramic	T _{stg}	-55 to 150 -55 to 165	°C °C

ELECTRICAL CHARACTERISTICS (VEE = -5.2 V ±5%)

Characteristic	Symbol	() •	2	5°	7	5°	
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	ΙE		53	II-A	48		53	mA
Input Current High Pin 9 Pins 3-6 and 10-13	linH		475 515	-	295 320	-	295 320	μΑ
Input Current Low	linL	0.5	036	0.5		0.3		μΑ
High Output Voltage	Voн	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	VOL	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	VIH	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	VIL	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

AC PARAMETERS

Propagation Delay Data Select	B mid :	pd [†] pd	1.0	1.9	1.0	1.8	1.0	2.0	ns
Rise Time		tr	0.7	2.2	0.7	2.0	0.7	2.2	ns
Fall Time	SAY HA	tf	0.7	2.2	0.7	2.0	0.7	2.2	ns

NOTE

Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater then 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

This document contains information on a new product. Specifications and information herein are subject to change without notice.



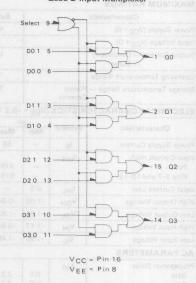


P SUFFIX PLASTIC PACKAGE CASE 648

L SUFFIX CERAMIC PACKAGE CASE 620



Quad 2-Input Multiplexer



TRUTH TABLE

Select	DO	D1	Q
L	φ	L	L
L	φ	Н	Н
н	L	φ	L
H	H	Φ	н

φ = Don't care

2

Advance Information

MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

The MC10H159 is a member of Motorola's new MECL family. The MC10H159 is a quad 2-input multiplexer with enable. This MECL 10KH part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay and no increase in power-supply current.

- Propagation Delay, 1.5 ns Typical
- Power Dissipation, 218 mW Typical
- Improved Noise Margin 150 mV (over operating voltage and temperature range)
- Voltage Compensated
- MECL 10K-Compatible





P SUFFIX PLASTIC PACKAGE CASE 648

L SUFFIX CERAMIC PACKAGE CASE 620



MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V _{CC} = 0)	VEE	-8.0 to 0	Vdc
Input Voltage (V _{CC} = 0)	VI	0 to VEE	Vdc
Output Current — Continuous — Surge	lout	50 100	mA
Operating Temperature Range	TA	0-75	°C
Storage Temperature Range — Plastic — Ceramic	T _{stg}	-55 to 150 -55 to 165	°C

ELECTRICAL CHARACTERISTICS (VFF = -5.2 V ±5%) (See Note)

01	Combat	0)°	2	5°	7	5°	11.3
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	ΙE		58	-10	53	T 1	58	mA
Input Current High Pin 9 Pins 3-7 and 10-13	linH	- 1	475 515		295 320	Ī	295 320	μА
Input Current Low	linL	0.5	-	0.5	-2	0.3	1	μА
High Output Voltage	VOH	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	VOL	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	VIH	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	VIL	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

AC PARAMETERS

Propagation Delay	tpd			13 2 40		- 30		ns
Data	100	0.5	2.2	0.5	2.0	0.5	2.2	
Select		1.0	3.2	1.0	3.0	1.0	3.2	-
Enable	-	1.0	3.2	1.0	3.0	1.0	3.2	
Rise Time	t _r	0.7	2.2	0.7	2.0	0.7	2.2	ns
Fall Time	t _f	0.7	2.2	0.7	2.0	0.7	2.2	ns

NOTE

Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater then 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

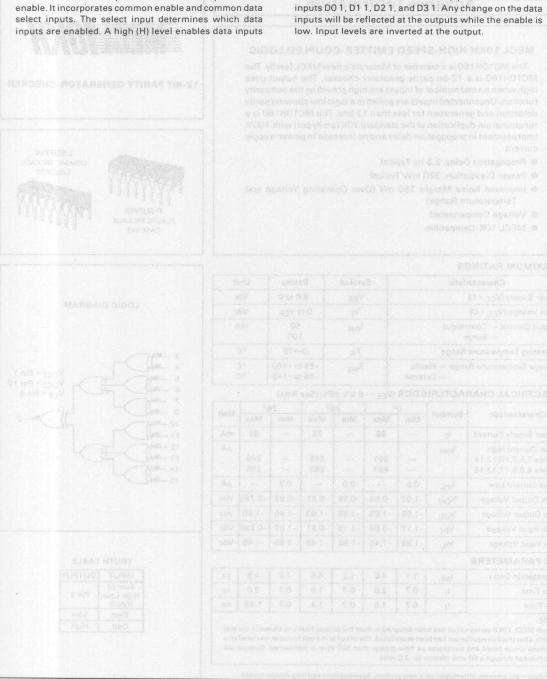
QUAD 2-INPUT MULTIPLEXER Select 9 D01 5 D00 6 D11 3 D10 4 Enable 7 D21 12 D2 0 13 Vcc Pin 16 VEE Pin 8

Enable	Select	DO	D1	0
L	L	Φ	L	Н
L	L	Ф	н	L
L	Н	L	Φ	Н
L	Н	H	Φ	L
Н	φ	Φ	Φ	L

APPLICATION INFORMATION

The MC10H159 is a quad two channel multiplexer with

DO 0, D1 0, D2 0, and D3 0. A low (L) level enables data



Advance Information

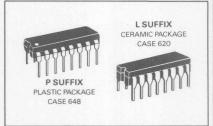
MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

The MC10H160 is a member of Motorola's new MECL family. The MC10H160 is a 12-bit parity generator-checker. The output goes high when an odd number of inputs are high providing the odd parity function. Unconnected inputs are pulled to a logic low allowing parity detection and generation for less than 12 bits. The MC10H160 is a functional pin duplication of the standard 10K family part with 100% improvement in propagation delay and no increase in power-supply current.

- Propagation Delay, 2.5 ns Typical
- Power Dissipation, 320 mW Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible



12-BIT PARITY GENERATOR-CHECKER



MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V _{CC} = 0)	VEE	-8.0 to 0	Vdc
Input Voltage (V _{CC} = 0)	VI	0 to VEE	Vdc
Output Current — Continuous — Surge	lout	50 100	mA
Operating Temperature Range	TA	0-+75	°C
Storage Temperature Range — Plastic — Ceramic	T _{stg}	-55 to +150 -55 to +165	°C

ELECTRICAL CHARACTERISTICS (VEE = -5.2 V ±5%) (See Note)

	0 1 1	()°	2	25°		75°	
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	1E	-	88	-	78	-	86	mA
Input Current High Pins 3,5,7,10,12,14 Pins 4,6,9,11,13,15	linH	_	391 457	_	246 285	_	246 285	μΑ
Input Current Low	linL	0.5	-	0.5	_	0.3	_	μΑ
High Output Voltage	VOH	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	VOL	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	VIH	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	VIL	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

AC PARAMETERS

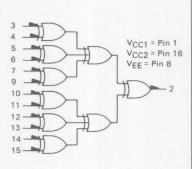
Propagation Delay	tpd	1.1	4.8	1.2	4.5	1.2	4.8	ns
Rise Time	tr	0.7	2.0	0.7	1.9	0.7	2.0	ns
Fall Time	tf	0.7	1.5	0.7	1.4	0.7	1.45	ns

NOTE:

Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50 ohm resistor to -2.0 volts.

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LOGIC DIAGRAM



TRUTH TABLE

INPUT	OUTPUT
Sum of High Level Inputs	Pin 2
Even	Low
Odd	High



Advance Information

MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

The MC10H161 is a member of Motorola's new MECL family. This part provides parallel decoding of a three bit binary word to one of eight lines. The MC10H161 is useful in high-speed multiplexer/demultiplexer applications.

- Propagation Delay, 1 ns Typical
- Power Dissipation 315 mW Typical (same as MECL 10K)
- Improved Noise Margin 150 mV (over operating voltage and temperature range)
- Voltage Compensated
- MECL 10K-Compatible.

MAXIMUM RATINGS

		200	
Characteristic	Symbol	Rating	Unit
Power Supply (V _{CC} = 0)	VEE	-8.0 to 0	Vdc
Input Voltage (V _{CC} = 0)	VI	0 to VEE	Vdc
Output Current — Continuous — Surge	lout	50 100	mA ****
Operating Temperature Range	TA	0-75	°C
Storage Temperature Range — Plastic — Ceramic	T _{stg}	-55 to 150 -55 to 165	°C °C

ELECTRICAL CHARACTERISTICS (VFF = -5.2 V ±5%) (See Note)

Chamadadia	Combal	0	0	2	5°	7	5°	Unit
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	1E	-	84		76	-	84	mA
Input Current High	linH	-	465		275	-	275	μΑ
Input Current Low	linL	0.5	-	0.5	-	0.3	-	μА
High Output Voltage	VOH	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	VOL	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	VIH	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	VIL	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

AC PARAMETERS

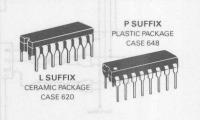
Propagation Delay	t _{pd}	0.5	3.1	0.5	3.0	0.5	3.2	ns
Rise Time	· t _r	0.5	2.2	0.5	2.0	0.5	2.2	ns
Fall Time	`t _f	0.5	2.2	0.5	2.0	0.5	2.2	ns

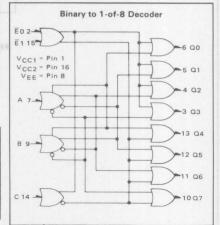
NOTE

Each MECL 10KH series circuit has been designed to meet the do specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater then 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

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	BLE		PU	TS	OUTPUTS							
Ē1	ĒΟ	С	В	Α	00	Q1	02	Q3	Q4	Q5	Q6	07
L	L	L	L	L	L	н	н	н	н	н	н	Н
L	L	L	L	H	H	L	H	H	н	н	н	н
L	L	L	н	L	· H	H	L	н	н	н	н	н
L	L	L	H	н	н	н	н	L	н	н	н	н
L	L	H	L	L	H	н	н	H	L	H	н	н
L	L	н	L	н	н	н	н	H	н	L	н	н
L	L	H	н	L	н	H	H	н	н	н	L	н
L	L	н	н	н	н	н	н	н	н	н	н	L
н	Φ	0	Φ	0	н	н	н	H	н	н	н	н
0	н	Φ	0	Φ	н	н	H	н	н	н	н	Н

The MC10H161 is designed to decode a three bit input word to one of eight output lines. The MC10H161 output will be low when selected while all other output are high. The enable inputs, when either or both are high, force all outputs high.

The MC10H161 is a true parallel decoder. This eliminates unequal parallel path delay times found in other decoder designs. These devices are ideally suited for multiplexer/demultiplexer applications.

FIGURE 1 — HIGH SPEED 16-BIT MULTIPLEXER/DEMULTIPLEXER

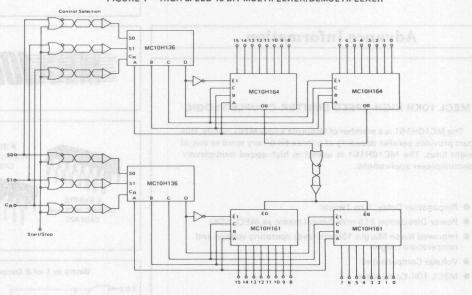
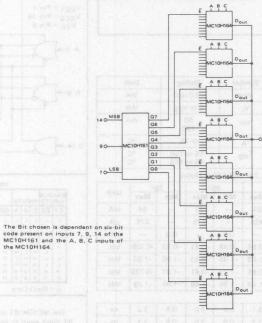


FIGURE 2 - 1-OF-64 LINE MULTIPLEXER



the MC10H164.



Advance Information

MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

The MC10H162 is a member of Motorola's new MECL family. This part provides parallel decoding of a three bit binary word to one of eight lines. The MC10H162 is useful in high-speed multiplexer/demultiplexer applications.

- Propagation Delay, 1 ns Typical
- Power Dissipation 315 mW Typical (same as MECL 10K)
- Improved Noise Margin 150 mV (over operating voltage and temperature range)
- Voltage Compensated
- MECL 10K-Compatible.

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V _{CC} = 0)	VEE	-8.0 to 0	Vdc
Input Voltage (V _{CC} = 0)	VI	0 to VEE	Vdc
Output Current — Continuous — Surge	lout	50 100	mA
Operating Temperature Range	TA	0-75	°C
Storage Temperature Range — Plastic — Ceramic	T _{stg}	-55 to 150 -55 to 165	°C

ELECTRICAL CHARACTERISTICS (VEE = -5.2 V ±5%) (See Note)

01	0 11	C	0	2	5°	7	5°	Unit
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	I _E	-	84	1	76	-	84	mA
Input Current High	linH	-1	465	-	275		275	μΑ
Input Current Low	linL	0.5		0.5		0.3	_	μА
High Output Voltage	VOH	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	VOL	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	VIH	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	VIL	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

AC PARAMETERS

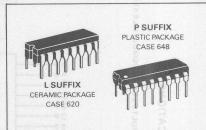
Propagation Delay	tpd	0.5	3.1	0.5	3.0	0.5	3.2	ns
Rise Time	tr	0.5	2.2	0.5	2.0	0.5	2.2	ns
Fall Time	tf	0.5	2.2	0.5	2.0	0.5	2.2	ns

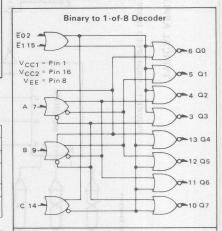
NOTE

Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater then 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

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	IN	PUT	rs			OUTPUTS								
EO	Ē1	C	В	A	00	Q1	Q2	Q3	Q4	Q5	Q6	07		
L	L	L	L	L	н	L	L	L	L	L	L	L		
L	L	L	L	н	L	н	L	L	L	L	L	L		
L	L	L	н	L	L	L	н	L	L	L	L	L		
L	L	L	н	н	L	L	L	н	L	L	L	L		
L	L	H	L	L	L	L	L	L	н	L	L	L		
L	·L	н	L	н	L	L	L	L	L	н	L	L		
L	L	н	н	L	L	L	L	L	L	L	H	L		
L	L	н	н	н	L	L	L	L	L	L	L	н		
H	0	Φ	Φ	0	L	L	L	L	L	L	L	L		
Φ	н	Φ	Φ	0	L	L	L	L	L	L	L	L		

The MC10H162 is designed to decode a three bit input word to one of eight output lines. The MC10H162 output will be high when selected while all other output are low. The enable inputs, when either or both are high, force all outputs low.

The MC10H162 is a true parallel decoder. This eliminates unequal parallel path delay times found in other decoder designs. These devices are ideally suited for multiplexer/demultiplexer applications.



Advance Information

PIGGRE 1 - HIGH SPEED 18-BIT MULTIPLEXER/DEMULTIPLEXER

MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

The MC10H164 is a member of Motorola's new MECL family. This MECL 10KH part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increase in power supply current.

- Propagation Delay, 1 ns Typical
- Power Dissipation 310 mW Typical (same as MECL 10K)
- Improved Noise Margin 150 mV (over operating voltage and temperature range)
- Voltage Compensated
- MECL 10K-Compatible.

MAXIMUM BATINGS

mir training in the training of			
Characteristic	Symbol	Rating	Unit
Power Supply (V _{CC} = 0)	VEE	-8.0 to 0	Vdc
Input Voltage (V _{CC} = 0)	VI	0 to V _{EE}	Vdc
Output Current — Continuous — Surge	lout	50 100	mA
Operating Temperature Range	TA	0-75	°C
Storage Temperature Range — Plastic — Ceramic	T _{stg}	-55 to 150 -55 to 165	°C °C

ELECTRICAL CHARACTERISTICS (VEE = -5.2 V ±5%) (See Note)

Characteristic	Combal	0	0°		25°		5°	Unit
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	1 _E	-	83	+14	75	11-	83	mA
Input Current High	linH	-	512	- Special	320	140	320	, µА
Input Current Low	linL	0.7	-	0.7	-	0.7	-	μА
High Output Voltage	Voн	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	VOL	-1.95	-1.63	-1.95	-1.63	-0.735	-1.60	Vdc
High Input Voltage	ViH	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	VIL	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

AC PARAMETERS

Propagation Delay	tpd				F			ns
X ₀ -X ₇		1.0	2.8	0.7	2.7	0.7	2.9	
A, B, C		1.0	3.8	0.7	3.6	0.7	3.9	
Enable		1.0	1.9	0.7	1.7	0.7	1.9	
Rise Time	tr	0.6	2.1	0.5	2.0	0.6	2.2	ns
Fall Time	tf	0.6	2.1	0.5	2.0	0.6	2.2	ns

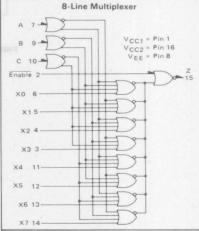
NOTE

Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater then 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

This document contains information on a new product. Specifications and information herein are subject to change without notice.







	ADD	PUTS				
ENABLE	С	В	А	Z		
L	L	L	L	XO		
L	L	L	н	X1		
Les este	L	н	L	X2		
L	L	Н	н	X3		
to Larver	3 H	L	L	X4		
La Se	H	L	н	X5		
L	н	н	L	X6		
L	н	н	н	X7		
н	ф	Φ	Φ	L		

The MC10H164 is designed to be used in data multiplexing and parallel to serial conversion applications. Full parallel gating provides equal delays through any data path. The MC10H164 incorporates an output buffer, eight inputs and an enable. A high on the enable forces the output low. The open emitter output allows the MC10H164 to be connected directly to a data bus. The enable line allows an easy means of expanding to more than 8 lines using additional MC10H164's.

FIGURE 1 - HIGH SPEED 16-BIT MULTIPLEXER/DEMULTIPLEXER

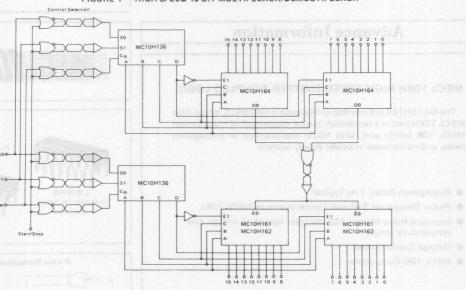
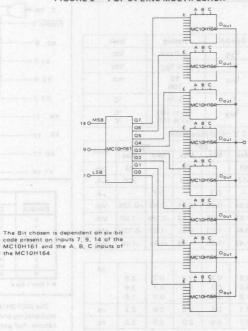


FIGURE 2 - 1-OF-64 LINE MULTIPLEXER





Advance Information

8-INPUT PRIORITY ENCODER

The MC10H165 is a member of Motorola's new MECL family. The MC10H165 is an 8-Input Priority Encoder. This 10KH part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increases in power supply current.

- Propagation Delay, Data-to-Output, 2.2 ns Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit			
Power Supply (V _{CC} = 0)	VEE	-8.0 to 0	Vdc			
Input Voltage (V _{CC} = 0)	VI	0 to VEE	Vdc			
Output Current — Continuous — Surge	lout	50 100	mA			
Operating Temperature Range	TA	0 to +75	°C			
Storage Temperature Range — Plastic — Ceramic	T _{stg}	-55 to +150 -55 to +165	°C			

ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2 V ±5.0%) (See Note)

	0°		25°		75°C		
Symbol	Min	Max	Min	Max	Min	Max	Unit
ΙE	-	144	_	131		144	mA
linH	3	510 600		320 370		320 370	μAdd
linL	0.5	_	0.5	-	0.3	_	μΑ
VOH	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
VOL	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
VIH	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
VIL	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc
	IE InH VOH VOL VIH	Symbol Min IE	Symbol Min Max IE — 144 InH — 510 — 600 IinL 0.5 — VOH -1.02 -0.84 VOL -1.95 -1.63 VIH -1.17 -0.84	Symbol Min Max Min IE 144 IinH 510 600 IinL 0.5 0.5 VOH -1.02 -0.84 -0.98 VOL -1.95 -1.63 -1.95 VIH -1.17 -0.84 -1.13	Symbol Min Max Min Max I _E 144 131 I _{inH} 510 320 600 370 I _{inL} 0.5 0.5 V _{OH} -1.02 -0.84 -0.98 -0.81 V _{OL} -1.95 -1.63 -1.95 -1.63 V _{IH} -1.17 -0.84 -1.13 -0.81	Symbol Min Max Min Max Min IE — 144 — 131 — InH — 510 — 320 — — 600 — 370 — InL 0.5 — 0.5 — 0.3 VOH -1.02 -0.84 -0.98 -0.81 -0.92 VOL -1.95 -1.63 -1.95 -1.63 -1.95 VIH -1.17 -0.84 -1.13 -0.81 -1.07	Symbol Min Max Min Max Min Max I _E — 144 — 131 — 144 I _{InH} — 510 — 320 — 320 — 600 — 370 — 370 I _{InL} 0.5 — 0.5 — 0.3 — V _{OH} –1.02 –0.84 –0.98 –0.81 –0.92 –0.735 V _{OL} –1.95 –1.63 –1.95 –1.63 –1.95 –1.60 V _{IH} –1.17 –0.84 –1.13 –0.81 –1.07 –0.735

AC PARAMETERS

Propagation Delay Data input → Output Clock Input → Output	t _{pd}	0.7	3.4	0.7	3.2	0.7 0.7	3.4 2.2	ns
Setup Time	t _{set}	3.0	_	3.0	_	3.0	_	ns
Hold Time	thold	0.5	-	0.5	-	0.5		ns
Rise Time	tr	0.5	2.2	0.5	2.0	0.5	2.2	ns
Fall Time	tf	0.5	2.2	0.5	2.0	0.5	2.2	ns

NOTE:

Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

This document contains information on a new product. Specifications and information herein are subject to change without notice.





L SUFFIX CERAMIC PACKAGE CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENT



TRUTH TABLE

DATA INPUTS						OUTPUTS					
D0	D1	D2	D3	D4	D5	D6	D7	03	Q2	Q1	QO
Н	φ	φ	φ	φ	φ	φ	φ	Н	L	L	L
L	Н	φ	φ	φ	φ	φ	φ	Н	L	L	Н
L	L	Н	φ	φ	φ	ф	ф	Н	L	Н	L
L	L	L	Н	φ	φ	φ	φ	H	L	Н	н
L	L	L	L	Н	φ	φ	φ	Н	Н	L	L
L	L	L	L	L	Н	φ	φ	H	Н	L	Н
L	L	L	L	L	L	Н	φ	Н	Н	Н	L
L	L	L	L	L	L	L	н	Н	н	н	Н
L	L	L	L	L	L	L	L	L	L	L	L

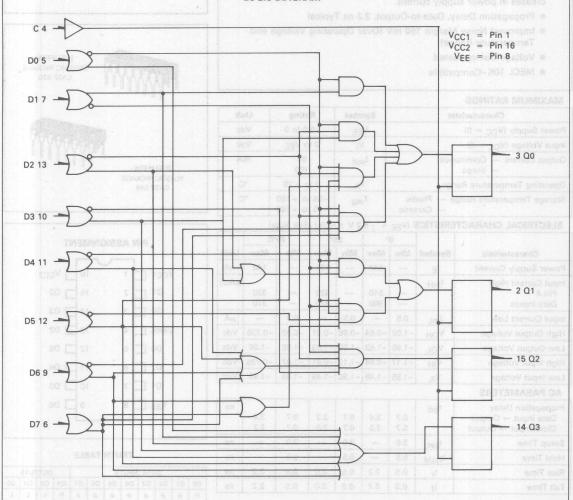
 $\phi = Don't Care$

8-INPUT PRIORITY ENCODER

The MC10H165 is a device designed to encode eight inputs to a binary coded output. The output code is that of the highest order input. Any input of lower priority is ignored. Each output incorporates a latch allowing synchronous operation. When the clock is low the outputs follow the inputs and latch when the clock goes high. This device is very useful for a variety of applications in checking system status in control processors, peripheral controllers, and testing systems.

The input is active when high, (e.g., the three binary outputs are low when input D0 is high). The Q3 output is high when any input is high. This allows direct extension into another priority encoder when more than eight inputs are necessary. The MC10H165 can also be used to develop binary codes from random logic inputs, for addressing ROMs, RAMs, or for multiplexing data.

LOGIC DIAGRAM



Numbers at ends of terminals denote pin numbers for L and P packages.

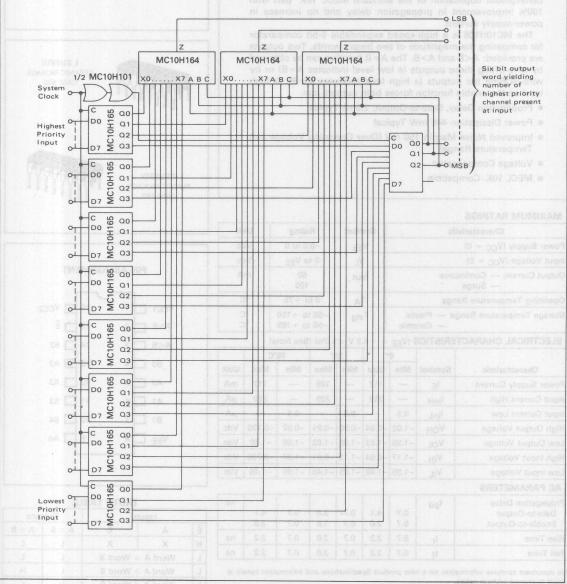
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APPLICATION INFORMATION

A typical application of the MC10H165 is the decoding of system status on a priority basis. A 64-line priority encoder is shown in the figure below. System status lines are connected to this encoder such that, when a given condition exists, the respective input will be at a logic high level. This scheme will select the one

of 64 different system conditions, as represented at the encoder inputs, which has priority in determining the next system operation to be performed. The binary code showing the address of the highest priority input present will appear at the encoder outputs to control other system logic functions.

64-LINE PRIORITY ENCODER



2

Advance Information

5-BIT MAGNITUDE COMPARATOR

The MC10H166 is a member of Motorola's new MECL family.

The MC10H166 is a 5-Bit Magnitude Comparator and is a functional/pinout duplication of the standard MECL 10K part with 100% improvement in propagation delay and no increase in power-supply current.

The MC10H166 is a high-speed expandable 5-bit comparator for comparing the magnitude of two binary words. Two outputs are provided: A<B and A>B. The A=B function can be obtained by wire-ORing these outputs (a low level indicates A=B) or by wire-NORing the outputs (a high level indicates A \neq B). A high level on the enable function forces both outputs low.

- Propagation Delay, Data-to-Output, 2.0 ns Typical
- Power Dissipation 440 mW Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V _{CC} = 0)	VEE	-8.0 to 0	Vdc
Input Voltage (V _{CC} = 0)	VI	0 to VEE	Vdc
Output Current — Continuous — Surge	lout	50 100	mA
Operating Temperature Range	TA	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T _{stg}	-55 to +150 -55 to +165	°C

ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2 V ±5.0%) (See Note)

		0°		25°		75°C		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	ΙE	_	117	_	106		117	mA
Input Current High	linH	_	350	-	220	_	220	μΑ
Input Current Low	linL	0.5		0.5		0.3		μΑ
High Output Voltage	VOH	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	VOL	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	VIH	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	VIL	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

AC PARAMETERS

Propagation Delay Data-to-Output Enable-to-Output	t _{pd}	0.7 0.7	4.1	0.7	3.8 1.8	0.7 0.7	4.1	ns
Rise Time	t _r	0.7	2.2	0.7	2.0	0.7	2.2	ns
Fall Time	tf	0.7	2.2	0.7	2.0	0.7	2.2	ns

This document contains information on a new product Specifications and information herein is subject to change without notice.



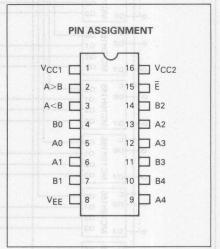
5-BIT MAGNITUDE COMPARATOR



L SUFFIX CERAMIC PACKAGE CASE 620

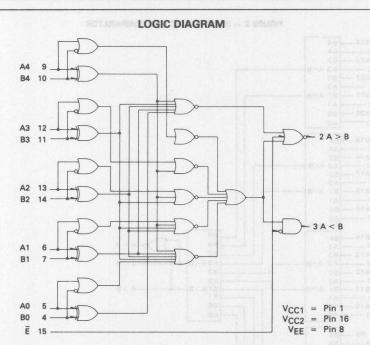
P SUFFIX
PLASTIC PACKAGE
CASE 648





TRUTH TABLE

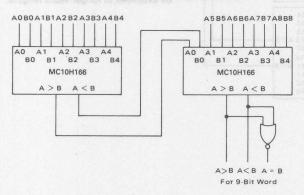
	Input	Outputs			
Ē	Α	В	A < B	A > B	
Н	X	X	L	L	
L	Word A =	Word B	L	L	
L	Word A >	Word B	L	Н	
L	Word A <	Word B	Н	L	



NOTE:

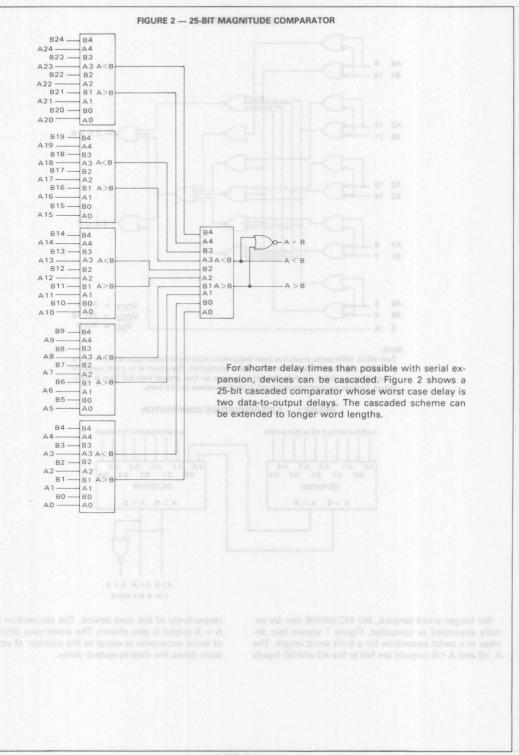
Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

FIGURE 1 — 9-BIT MAGNITUDE COMPARATOR



For longer word lengths, the MC10H166 can be serially expanded or cascaded. Figure 1 shows two devices in a serial expansion for a 9-bit word length. The A >B and A <B outputs are fed to the A0 and B0 inputs

respectively of the next device. The connection for an A=B output is also shown. The worst case delay time of serial expansion is equal to the number of comparators times the data-to-output delay.





MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

The MC10H173 is a quad 2-input multiplexer with latch. This device is a functional/pinout duplication of the standard MECL 10K part, with 100% improvement in propagation delay and no increase in power supply current.

- Data Propagation Delay, 1.5 ns Typical
- Voltage Compensated
- Power Dissipation, 275 mW Typical
- MECL 10K-Compatible
- Improved Noise Margin 150 mV (over operating voltage and temperature range)

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V _{CC} = 0)	VEE	-8.0 to 0	Vdc
Input Voltage (V _{CC} = 0)	VI	0 to VEE	Vdc
Output Current — Continuous — Surge	lout	50 100	mA
Operating Temperature Range	TA	0-75	°C
Storage Temperature Range — Plastic — Ceramic	T _{stg}	-55 to 150 -55 to 165	°C

ELECTRICAL CHARACTERISTICS (VFF = -5.2 V ± 5%) (See note)

)°	25°		75°C		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	ΙE		73		66		73	mAdc
Input Current High Pins 3-7 & 10-13 Pin 9	linH		510 475		320 300		320 300	μΑ
Input Current Low	linL	0.5	_	0.5	_	0.3	_	μА
High Output Voltage	Vон	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	VOL	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	VIH	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	VIL	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

AC PARAMETERS

Propagation Delay	tpd							ns
Data		0.7	2.3	0.7	2.1	0.7	2.3	11211
Clock		1.0	3.7	1.0	3.5	1.0	3.7	
Select		1.0	3.6	1.0	3.4	1.0	3.6	
Set Up Time	tset							ns
Data		0.7	_	0.7	_	0.7	_	
Select		1.0	-	1.0	_	1.0	-	
Hold Time	thold							ns
Data		0.7	_	0.7	_	0.7	_	
Select		1.0	-	1.0	_	1.0	_	
Rise Time	tr	0.7	2.4	0.7	2.1	0.7	2.4	ns
Fall Time	tf	0.7	2.4	0.7	2.1	0.7	2.4	ns

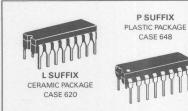
NOTE

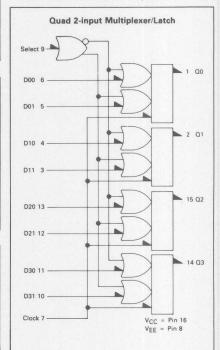
Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

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MC10H173







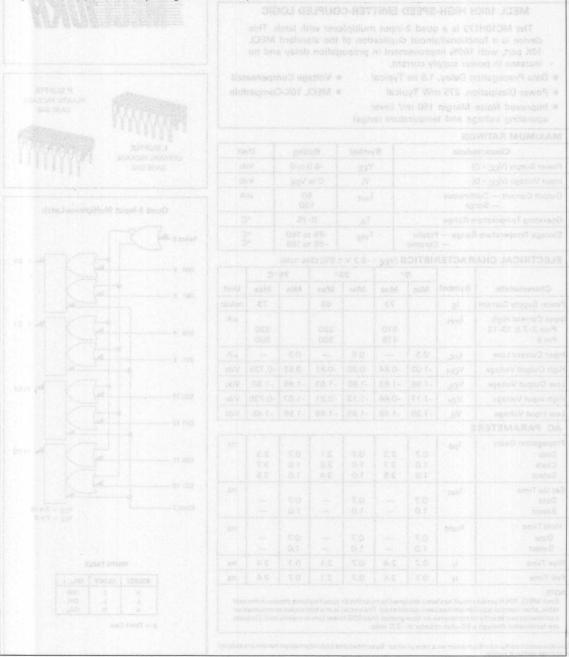
TRUTH TABLE

SELECT	CLOCK	Q0n+1
Н	L	D00
L	L	D01
ф	Н	Q0n

φ = Don't Care

The MC10173 is a quad two-channel multiplexer with latch. It incorporates common clock and common data select inputs. The select input determines which data input is enabled. A high (H) level enables data inputs D00, D10, D20, and D30 and a low (L) level enables data inputs D01, D11, D21, D31. Any change on the data input

will be reflected at the outputs while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information.





Advance Information

MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

The MC10H174 is a Dual 4-to-1 Multiplexer. This device is a functional/pinout duplication of the standard MECL 10K part, with 100% improvement in propagation delay and no increase in power supply current.

- Propagation Delay, 1.5 ns Typical
- Power Dissipation, 305 mW Typical
- Improved Noise Margin 150 mV (over operating voltage and temperature range)
- Voltage Compensated
- MECL 10K-Compatible

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V _{CC} = 0)	VEE	-8.0 to 0	Vdc
Input Voltage (V _{CC} = 0)	VI	0 to VEE	Vdc
Output Current — Continuous — Surge	lout	50 100	mA
Operating Temperature Range	TA	0-75	°C
Storage Temperature Range — Plastic — Ceramic	T _{stg}	- 55 to 150 - 55 to 165	°°°°°°°°°°°°°°°°°°°°°°°°°°°°°°°°°°°°°

ELECTRICAL CHARACTERISTICS (VFF = -5.2 V ± 5%) (See note)

		0°		25°		75°		Carpine .
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	IE		80		73	8	80	mAdo
Input Current High Pins 3–7 & 9–13 Pin 14	linH	è nc	475 670	0	300 420	0- 56	300 420	μAdc
Input Current Low	linL	0.5	-	0.5	W I Do	0.3	1-1-89	μА
High Output Voltage	VOH	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	VOL	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	VIH	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	VIL	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

AC PARAMETERS

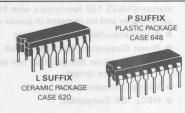
Propagation Delay Data Select (A, B) Enable	^t pd	1.0 1.0 1.0	2.9 3.8 1.9	0.7 0.7 0.7	2.7 3.6 1.7	0.7 0.7 0.7	2.9 3.8 1.9	ns
Rise Time	t _r	0.6	2.2	0.5	2.0	0.6	2.2	ns
Fall Time	tf	0.6	2.2	0.5	2.0	0.6	2.2	ns

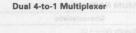
NOTE

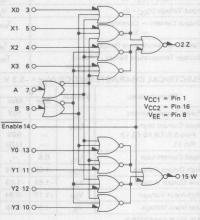
Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

This document contains information on a new product. Specifications and information herein are subject to change without notice.









TRUTH TABLE

	ENABLE	ADDRES	S INPUTS	OUTPUTS		
	Ε	В	A	Z	W	
	Н	ф	ф	L	L	
	L	L	L	XO	Y0 -	
I	le ldL as a	ed aLd m	н	X1	Y1	
	L	Н	L	X2	Y2	
1	L	н	Н	ХЗ	Y3	

φ = Don't Care



2

Advance Information

MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

The MC10H175 is a member of Motorola's new MECL family. The MC10H175 is a quint D type latch with common reset and clock lines. This MECL 10KH part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay and no increase in power-supply current.

- Propagation Delay, 1.2 ns Typical
- Power Dissipation, 400 mW Typical
- Improved Noise Margin 150 mV (over operating voltage and temperature range)
- Voltage Compensated
- MECL 10K-Compatible

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V _{CC} = 0)	VEE	-8.0 to 0	Vdc
Input Voltage (V _{CC} = 0)	V _I	0 to VEE	Vdc
Output Current — Continuous — Surge	lout	50 100	mA
Operating Temperature Range	TA	0-75	°C
Storage Temperature Range — Plastic — Ceramic	T _{stg}	-55 to 150 -55 to 165	°C °C

ELECTRICAL CHARACTERISTICS (VEE = -5.2 V ±5%) (See Note)

01	0	1	0	2	5°	7	5°	11-10
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	1E	1	107	1	97	-	107	mA
Input Current High Pins 5,6,7,9,10,12,13 Pin 11	linH	-	565 1120	18	335 660	0 <u>i</u> n	335 660	μА
Input Current Low	linL	0.5	-	0.5	41+	0.3	-	μА
High Output Voltage	VOH	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	VOL	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	VIH	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	VIL	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

AC PARAMETERS

Propagation Delay	.tpd			1	W 122	1 60	1 316	ns
Data		0.7	1.8	0.7	1.7	0.7	1.8	100
Clock		0.7	2.3	0.7	2.2	0.7	2.2	
Reset		0.7	2.1	0.7	2.0	0.7	2.1	
Set-up Time	tset	1.5	-	1.5	1	1.5	0 + 7	ns
Hold Time	thold	1.0	-	1.0	1 + 3	1.0	0 + 3	ns
Rise Time	t _r	0.7	1.8	0.7	1.8	0.7	1.9	ns
Fall Time	tf	0.7	1.8	0.7	1.8	0.7	1.9	ns

NOTE

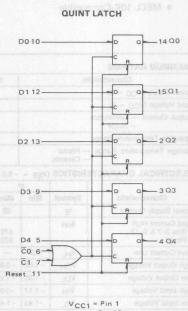
Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater then 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

This document contains information on a new product. Specifications and information herein are subject to change without notice.











TRUTH TABLE

D	CO	Č1	Reset	Q n+1
L	L	L	Φ	L
н	L	L	Φ	H
φ	H	0	L	Qn
φ	0	н	L	Qn
Φ	H	0	н	L
φ	0	н	н	L

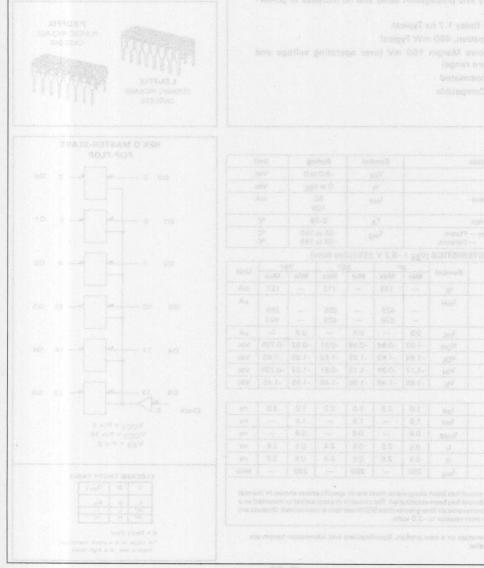
φ = don't care

APPLICATION INFORMATION

The MC10H175 is a high speed, low power quint latch. It features five D type latches with common reset and a common two-input clock. Data is transferred on the negative edge of the clock and latched on the positive edge. The two clock inputs are "OR"ed together.

Any change on the data input will be reflected at the

outputs while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information. The reset input is enabled only when the clock is in the high state.



2

Advance Information

MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

The MC10H176 is a member of Motorola's new MECL family. The MC10H176 contains six master slave type "D" flip-flops with a common clock. This MECL 10KH part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in clock frequency and propagation delay and no increase in power-supply current.

- Propagation Delay 1.7 ns Typical
- Power Dissipation, 460 mW Typical
- Improved Noise Margin 150 mV (over operating voltage and temperature range)
- Voltage Compensated
- MECL 10K-Compatible





L SUFFIX CERAMIC PACKAGE CASE 620



P SUFFIX

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V _{CC} = 0)	VEE	-8.0 to 0	Vdc
Input Voltage (V _{CC} = 0)	V _I	0 to VEE	Vdc
Output Current — Continuous — Surge	lout	50 100	mA
Operating Temperature Range	TA	0-75	°C
Storage Temperature Range — Plastic — Ceramic	T _{stg}	-55 to 150 -55 to 165	°C

ELECTRICAL CHARACTERISTICS (VFF = -5.2 V ±5%) (See Note)

Obti-di-	0	0)°	2	5°	75°		Unit
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	ΙE	-	123	-	112	-	123	mA
Input Current High Pins 5,6,7,10,11,12 Pin 9	linH	_	425 670	=	265 420	=	265 420	μА
Input Current Low	linL	0.5	-	0.5	-	0.3	-	μА
High Output Voltage	VOH	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	VOL	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	VIH	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	VIL	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

AC PARAMETERS

Propagation Delay	tpd	1.0	2.9	1.0	2.7	1.0	3.0	ns
Set-up Time	tset	1.5	-	1.5	-	1.5	-	ns
Hold Time	thold	0.8	-	0.8	_	0.8	-	ns
Rise Time	t _r	0.5	2.5	0.5	2.4	0.5	2.6	ns
Fall Time	tf	0.5	2.5	0.5	2.4	0.5	2.6	ns
Toggle Frequency	f _{tog}	250	_	250	-	250	-	MHz

NOTE

Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater then 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

HEX D MASTER-SLAVE FLIP-FLOP 00 DO 5 01 6 D2 02 D3 10 13 04 D4 11 D5 12 Clock V_{CC1} = Pin 1 V_{CC2} = Pin 16 V_{EE} = Pin 8

CLOCKED TRUTH TABLE

С	D	Q _{n+1}
L	Φ	an
н.	L	L
н.	н	H

φ = Don't Care

*A clock H is a clock transition from a low to a high state.

APPLICATION INFORMATION

The MC10H176 contains six high-speed, master slave type "D" flip-flops. Data is entered into the master when the clock is low. Master-to-slave data transfer takes place on the positive-going Clock transition. Thus, outputs may

change only on a positive-going Clock transition. A change in the information present at the data (D) input will not affect the output information any other time due to the master-slave construction of this device.

2

Advance Information

MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

The MC10H179 is a member of Motorola's new MECL family. It is a functional/pinout duplication of the standard MECL 10K part, with 100% improvement in propagation delay and no increase in power supply current.

- Power Dissipation, 300 mW Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V _{CC} = 0)	VEE	-8.0 to 0	Vdc
Input Voltage (V _{CC} = 0)	VI	0 to VEE	Vdc
Output Current — Continuous — Surge	l _{out}	50 100	mA
Operating Temperature Range	TA	0-+75	°C
Storage Temperature Range — Plastic — Ceramic	T _{stg}	-55 to +150 -55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2 V ± 5%) (See Note)

Characteristic	Combal	0)0	2	5°	7	75°	mA μA
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	
Power Supply Current	ΙE	-	79	-	72	-	79	mA
Input Current High Pins 5 and 9 Pins 4, 7 and 11 Pin 14 Pin 12 Pins 10 and 13	linH		465 545 705 790 870		275 320 415 465 510	=	275 320 415 465 510	μΑ
Input Current Low	linL	0.5	_	0.5	-	0.3	_	μΑ
High Output Voltage	VOH	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	VOL	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	VIH	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	VIL	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

AC PARAMETERS

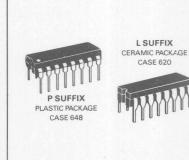
Propagation Delay Pins 5, 7, 9, 10, 11, 13 to 3 or 6	tpd	0.7	2.8	0.7	2.5	0.7	2.8	ns
G to GG		0.7	2.8	0.7	2.5	0.7	2.8	
P to PG		0.7	2.0	0.7	1.8	0.7	2.0	
P to G _G		0.7	2.8	0.7	2.5	0.7	2.8	
Rise Time	tr	0.5	2.4	0.5	2.2	0.5	2.4	ns
Fall Time	tf	0.5	2.4	0.5	2.2	0.5	2.4	ns

NOTE

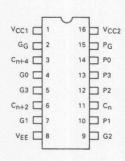
Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 flpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

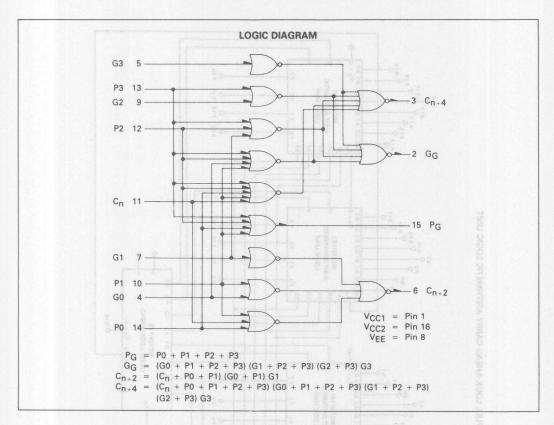


LOOK-AHEAD CARRY BLOCK



PIN ASSIGNMENT





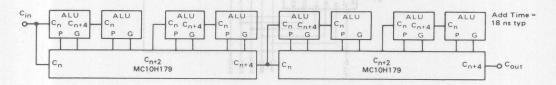
TYPICAL APPLICATIONS

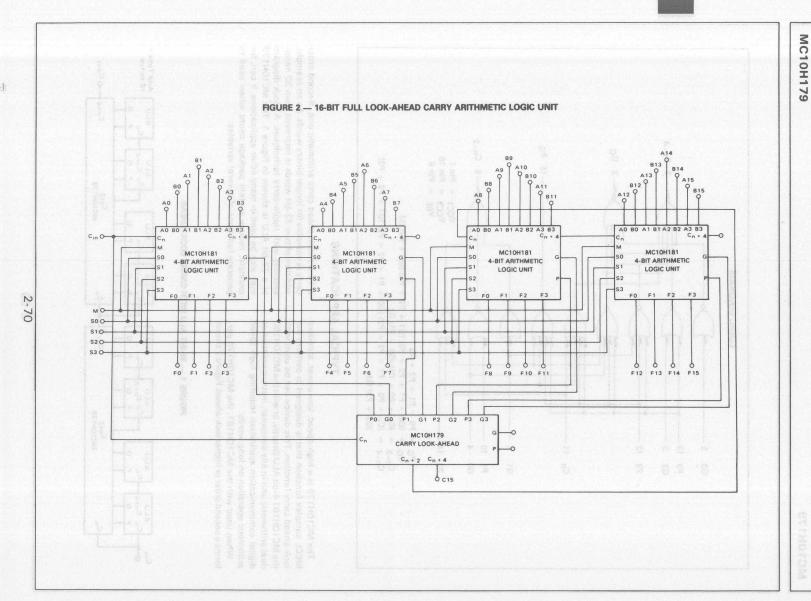
The MC10H179 is a high-speed, low-power, standard MECL complex function that is designed to perform the look-ahead carry function. This device can be used with the MC10H181 4-bit ALU directly, or with the MC10H180 dual arithmetic unit in any computer, instrumentation or digital communication application requiring high speed arithmetic operation on long words.

When used with the MC10H181, the MC10H179 performs a second order or higher look-ahead. Figure 2 shows

a 16-bit look-ahead carry arithmetic unit. Second order carry is valuable for longer binary words. As an example, addition of two 32-bit words is improved from 30 nanoseconds with ripple-carry techniques. A block diagram of a 32-bit ALU is shown in Figure 1. The MC10H179 may also be used in many other applications. It can, for example, reduce system package count when used to generate functions of several variables.

FIGURE 1 — 32-BIT ALU WITH CARRY LOOK-AHEAD







MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

The MC10H180 is a member of Motorola's new MECL family. It is a high-speed, low-power, general-purpose adder/subtractor. It is designed to be used in special purpose adders/subtractors or in high-speed multiplier arrays.

Inputs for each adder are Carry-in, Operand A, and Operand B; outputs are Sum, Sum and Carry-out. The common select inputs serve as a control line to Invert A for subtract, and a control line to Invert B.

- Propagation Delay, 1.8 ns Typical, Operand and Select to Output
- Power Dissipation, 360 mW Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit	
Power Supply (V _{CC} = 0)	VEE	-8.0 to 0	Vdc	
Input Voltage (V _{CC} = 0)	VI	0 to VEE	Vdc	
Output Current — Continuous — Surge	lout	50 100	mA	
Operating Temperature Range	TA	0-+75	°C	
Storage Temperature Range — Plastic — Ceramic	T _{stg}	-55 to +150 -55 to +165	°C °C	

ELECTRICAL CHARACTERISTICS (VEE = -5.2 V ± 5%) (See Note)

Characteristic	0 1 1	0	0	25°		7	5°		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit	
Power Supply Current	I _E	-	95	-	86	-	95	mA	
Input Current High Pins 4, 12 Pins 7, 9 Pin 5, 6, 10, 11	linH	=	665 515 410	_	417 320 255	Ξ	417 320 255	μΑ	
Input Current Low	linL	0.5	- 1	0.5	_	0.3	-	μΑ	
High Output Voltage	VOH	-1.020	-0.840	-0.980	-0.810	-0.920	-0.735	Vdc	
Low Output Voltage	VOL	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc	
High Input Voltage	VIH	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc	
Low Input Voltage	VIL	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc	

AC PARAMETERS

Propagation Delay Operand to Output Select to Output Carry-in to Output	^t pd	0.5 0.5 0.5	3.8 3.8 2.1	0.5 0.5 0.5	3.5 3.5 1.8	0.5 0.5 0.5	3.8 3.8 2.1	ns
Rise Time	t _r	0.5	2.2	0.5	2.0	0.5	2.2	ns
Fall Time	tf	0.5	2.2	0.5	2.0	0.5	2.2	ns

NOTE

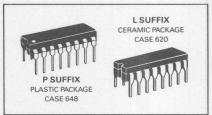
Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 ffpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

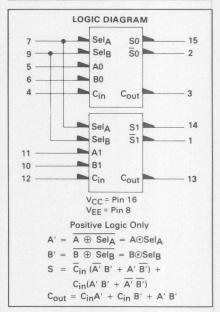
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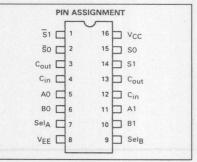
MC10H180



DUAL 2-BIT ADDER/SUBTRACTOR







FUNCTION SELECT TABLE

SelA	SelB	Function
Н	Н	S = A plus B
Н	L	S = A minus B
L	Н	S = B minus A
L	L	S = 0 minus A minus B

TRUTH TABLE

		INI	PUTS					
FUNCTION	SelA	Selg	A0	ВО	Cin	SO	S0	Cout
ADD	н	н	L	L	L	L	н	L
	н	н	L	L	Н	н	L	L
	Н	H	L	H	L	Н	L	L
	H	н	L	H	H	L	Н	H
	Н	н	H	L	L	н	L	L
	н	н	Н	L	Н	L	Н	Н
	н	H	Н	H	L	L	H	H
	Н	H	Н	Н	Н	Н	L	Н
SUBTRACT	Н	L	L	L	L	н	L	L
	H	L	L	L	H	L	H	H
	H	L	L	. н	L	L	н	L
	H	L	L	H-	H	Н	L	L
	H	L	H	L	L	L	H	н
	Н	L	н	L	Н	Н	L	Н
	н	L	н	н	L	н	L	L
	н	L	H	н	H	L	н	H

		IN	PUTS					
FUNCTION	SelA	SelB	A0	BO	Cin	SO	S0	Cout
REVERSE	L	н	L	L	L	н	L	L
SUBTRACT	L	Н	L	L	H	L	н	н
	L	н	L	Н	L	L	Н	н
	L	н	L	H	H	Н	L	H
	L	Н	н	L	L	L	Н	L
	L	Н	Н	L	Н	н	L	L
3 033	L	н	H	H	L	H	L	L
	L	Н	Н	Н	Н	L	Н	Н
	L	L	L	L	L	L	н	н
	o L	L	L	LO	H	H	L	Н
	L	L	L	Н	L	н	L	L
	F	L	L	H	H	L	н	н
	L	L	Н	L	L	H	L	L
27	L	L	Н	L	Н	L	H	H
	SC 18	30	н	H	L	O.	H	L
	L	L	H.	Н	Н	Н	L	L

	XAMUN SON SON SON SON SON SON SON SON SON SO	

			15

2-72



Advance Information

MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

The MC10H181 is a high-speed arithmetic logic unit capable of performing 16 logic operations and 16 arithmetic operations on two four-bit words. Full internal carry is incorporated for ripple through operation.

Arithmetic logic operations are selected by applying the appropriate binary word to the select inputs (S0 through S3) as indicated in the tables of arithmetic/logic functions. Group carry propagate (P_G) and carry generate (G_G) are provided to allow fast operations on very long words using a second order look-ahead. The internal carry is enabled by applying a low level voltage to the mode control input (M).

When used with the MC10H179, full-carry look-ahead, as a second order look-ahead block, the MC10H181 provides high-speed arithmetic operations on very long words.

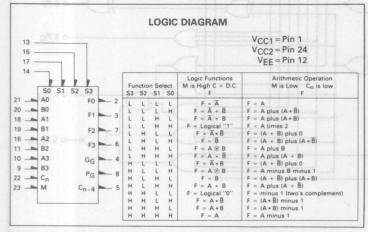
This 10KH part is a functional/pinout duplication of the standard MECL 10K family part with 100% improvement in propagation delay and no increase in power supply current.

- Improved Noise Margin, 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated

MECL 10K - Compatible

MAXIMUM RATINGS

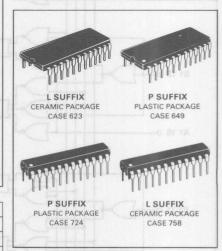
Characteristic	Symbol	Rating	Unit
Power Supply (V _{CC} = 0)	VEE	-8.0 to 0	Vdc
Input Voltage (V _{CC} = 0)	VI	0 to VEE	Vdc
Output Current — Continuous — Surge	lout	50 100	mA
Operating Temperature Range	TA	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T _{stg}	-55 to +150 -55 to +165	°C °C

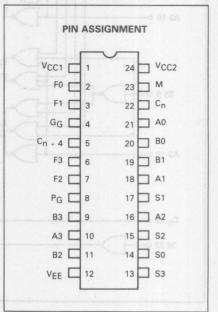


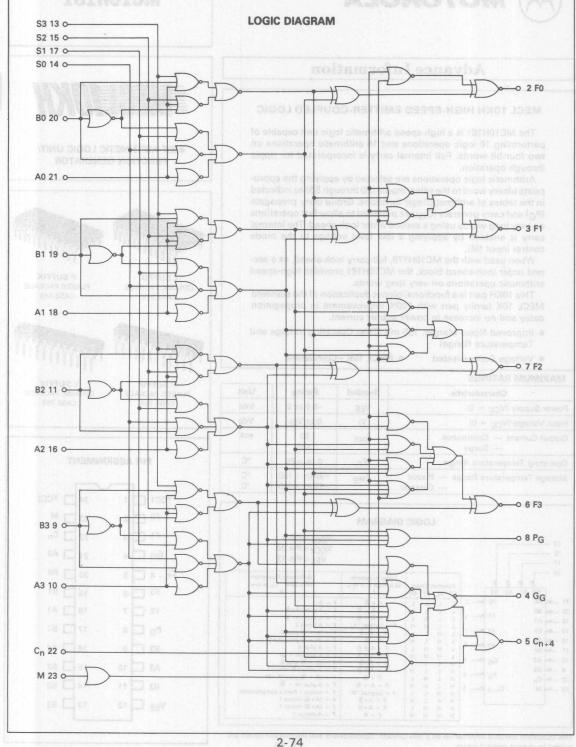
This document contains information on a new product. Specifications and information herein are subject to change without notice. 2-73



4-BIT ARITHMETIC LOGIC UNIT/ FUNCTION GENERATOR







ELECTRICAL CHARACTERISTICS (VEE = -5.2 V ±5.0%) (See Note)

		0	0	25°		75	°C ⊃°c	15	
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit	
Power Supply Current	IE	_	159	Contract of	145	B) The BY III	159	mA	
Input Current High Pin 22 Pins 14,23 Pins 13,15,17 Pins 10,16,18,21 Pins 9,11,19,20	linH	= =	720 405 515 475 465	isan E	450 255 320 300 275	= = = = = = = = = = = = = = = = = = = =	450 255 320 300 275	μΑ	
Input Current Low Pins 9–11, 13–22	linL	0.5		0.5	_	0.3	Tie	μΑ	
High Output Voltage	VOH	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc	
Low Output Voltage	VOL	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc	
High Input Voltage	VIH	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc	
Low Input Voltage	VIL	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc	

Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

AC PARAMETERS

	A CONTRACT		no even			AC S	witchi	ng Cha	racter	istics	1 20
			100		0	C	+2	5°C	+7	5°C	
Characteristic	Symbol	Input	Output	Conditions†	Min	Max	Min	Max	Min	Max	Unit
Propagation Delay Rise Time, Fall Time	t++,t t+,t-	C _n	C _{n+4} C _{n+4}	A0,A1,A2,A3 A0,A1,A2,A3	0.7 0.7	2.2 2.4	0.7	2.0	0.7 0.7	2.2	ns ns
Propagation Delay	t++,t+- t-+,t	C _n	F1 F1	Α0	0.7	3.8	0.7	3.5	0.7	3.8	ns
Rise Time, Fall Time	t+,t-	Cn	F1		0.7	2.2	0.7	2.0	0.7	2.2	11121
Propagation Delay Rise Time, Fall Time	t++,t+- t-+,t t+,t-	A1 A1 A1	F1 F1 F1		0.7 0.7 0.7	5.5 5.5 2.2	0.7 0.7 0.7	5.0 5.0 2.0	0.7 0.7 0.7	5.5 5.5 2.2	ns
Propagation Delay Rise Time, Fall Time	t++,t t+,t-	A1 A1	PG PG	S0,S3 S0,S3	0.7	3.8 2.4	0.7 0.7	3.5 2.2	0.7 0.7	3.8 2.4	ns ns
Propagation Delay Rise Time, Fall Time	t++,t t+,t-	A1 A1	G _G G _G	A0,A2,A3,C _n A0,A2,A3,C _n	0.7	5.0 2.4	0.7 0.7	4.5	0.7 0.7	5.0 2.4	ns ns
Propagation Delay Rise Time, Fall Time	t+-,t-+ t+,t-	A1 A1	C _{n+4}	A0,A2,A3,C _n A0,A2,A3,C _n	0.7	6.0 2.4	0.7	5.4 2.2	0.7	6.0	ns ns
Propagation Delay Rise Time, Fall Time	t++,t-+ t+,t-	B1 B1	F1 F1	S3,C _n S3,C _n	0.7	7.15 2.4	0.7	6.5	0.7	7.15 2.4	ns ns
Propagation Delay Rise Time, Fall Time	t++,t t+,t-	B1 B1	PG PG	S0,A1 S0,A1	0.7	3.8	0.7	3.5	0.7 0.7	3.8 2.4	ns ns
Propagation Delay Rise Time, Fall Time	t++,t t+,t-	B1 B1	G _G G _G	S3,C _n S3,C _n	0.7	5.0 2.4	0.7 0.7	4.5 2.2	0.7 0.7	5.0 2.4	ns ns
Propagation Delay Rise Time, Fall Time	t+-,t-+ t+,t-	B1 B1	C _{n+4}	S3,C _n	0.7 0.7	6.0 2.4	0.7	5.4	0.7 0.7	6.0 2.4	ns
Propagation Delay Rise Time, Fall Time	t++,t+- t+,t-	M	08 F1	8,1+ 80 ± 99.1+ 0,1- 10 ± 2,1.1-	0.7 0.7	3.9	0.7	3.5 2.0	0.7	3.9	ns
Propagation Delay Rise Time, Fall Time	t+-,t-+ t+,t-	S1 S1	F1 F1	A1,B1 A1,B1	0.7	5.5 2.2	0.7	5.0 2.0	0.7	5.5	ns
Propagation Delay Rise Time, Fall Time	t-+,t+- t+,t-	S1 S1	P _G	A3,B3 A3,B3	0.7	5.0 2.4	0.7 0.7	4.5	0.7 0.7	5.0	ns
Propagation Delay Rise Time, Fall Time	t+-,t-+ t+,t-	S1 S1	C _{n+4} C _{n+4}	A3,B3 A3,B3	0.7	6.0 2.4	0.7	5.4 2.2	0.7	6.0	ns
Propagation Delay Rise Time, Fall Time	t+-,t-+ t+,t-	S1 S1	G _G G _G	A3,B3 A3,B3	0.7	5.0 2.4	0.7	4.5 2.2	1.9 0.7	5.0 2.4	ns

†Logic high level (+1.11 Vdc) applied to pins listed. All other input pins are left floating or tied to +0.31 Vdc. $V_{CC1} = V_{CC2} = +2.0 \ \text{Vdc}, \ V_{EE} = -3.2 \ \text{Vdc}$

MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

The MC10H186 is a member of Motorola's new MECL family. The MC10H186 is a hex D type flip-flop with common reset and clock lines. This MECL 10KH part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in clock toggle frequency and propagation delay and no increase in power-supply current.

- Propagation Delay, 1.7 ns Typical
- Power Dissipation, 460 mW Typical
- Improved Noise Margin 150 mV (over operating voltage and temperature range)
- Voltage Compensated
- MECL 10K-Compatible



HEX-D FLIP FLOP



L SUFFIX CERAMIC PACKAGE CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648



MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit	
Power Supply (V _{CC} = 0)	VEE	-8.0 to 0	Vdc	
Input Voltage (V _{CC} = 0)	V _I	O to VEE	Vdc	1
Output Current — Continuous — Surge	lout	50 100	mA MA	
Operating Temperature Range	TA	0-75	°C	
Storage Temperature Range — Plastic — Ceramic	T _{stg}	-55 to 150 -55 to 165	°C °C	September 1

ELECTRICAL CHARACTERISTICS (VEE = -5.2 V ±5%) (See Note)

01	0 7.0	1) 0	2	25°		5°	Unit
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	I _E	Try	121	-	110		121	mA
Input Current High Pins 5,6,7,10,11,12	S linH 0	2.5	430	_	265		265	μА
Pin 9 0 0 5.0	0.7 45	□ a	670	-	420	-	420	
Pin 1 4 5 1 7 0	0.7 [.22	24	1250	-	765	-	765	μΑ
Input Current Low	I linL	0.5	(++0)	0.5	Sec.	0.3	100	μΑ
High Output Voltage	VOH	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	VOL	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	VIH	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	VIL	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

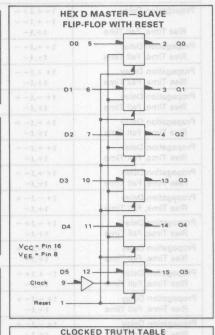
AC PARAMETERS

Propagation Delay	t _{pd}	0.7	3.0	0.7	2.7	0.7	3.0	ns
Set-up Time	tset	1.5	1.00	1.5	1424	1.5	24	ns
Hold Time	thold	1.0	90	1.0	68, 6 A	1.0	-	ns
Rise Time	tr	0.7	2.6	0.7	2.4	0.7	2.6	ns
Fall Time 0.8 8 1	t _f	0.7	2.6	0.7	2.4	0.7	2.6	ns
Toggle Frequency	ftog	250		250	DH LA	250	04	MHz
Reset Recovery Time (t ₁₋₉₊)	trr	3.0	_	3.0	_	3.0	_	ns

NOTE

Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater then 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

This document contains information on a new product. Specifications and information herein are subject to change without notice.



R C Q Qn+1 L L Ø Qn L H * L L L W L

Φ Don't Care
 *A clock H is a clock transition from a low to a high state.

APPLICATION INFORMATION

The MC10H186 contains six high-speed, master slave type "D" flip-flops. Data is entered into the master when the clock is low. Master-to-slave data transfer takes place on the positive-going Clock transition. Thus outputs may change only on a positive-going Clock transition. A change

in the information present at the data (D) input will not affect the output information any other time due to the master-slave construction of this device. A common Reset is included in this circuit. The Reset overrides the clock.

L SUFFIX
CERAMIC MCKAGE
CERAMIC MCKAGE
CAGERSO

MC10H188 is a high-speed Hex Buffer with a control Enable input. When Enable is in the high-state, all outputs are in the low-state. When Enable is in the low-state, the outputs take the same state as the inputs.

This MECL TOKH part is a functional/placed duplication of the

propagation below 1.3 hs Tuskel Data-to-Curbut

& Immoved Moles Margin 150 mV (Over Operation

6 Voltage Componested

WECL TOK-Compatible

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Each MECL 10XX series viscus free beautiful an accordance of specifical consistence shows in the rest policy, after the rest land to the second of the country of the second of the seco

MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

The MC10H188 is a member of Motorola's new MECL family. The MC10H188 is a high-speed Hex Buffer with a common Enable input. When Enable is in the high-state, all outputs are in the low-state. When Enable is in the low-state, the outputs take the same state as the inputs.

This MECL 10KH part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay and no increase in power-supply current.

- Propagation Delay, 1.3 ns Typical Data-to-Output
- Power Dissipation 180 mW Typ/Pkg (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit	
Power Supply (V _{CC} = 0)	VEE	-8.0 to 0		
Input Voltage (V _{CC} = 0)	VI	0 to VEE	Vdc	
Output Current — Continuous — Surge	lout	50 100	mA	
Operating Temperature Range	TA	0-+75	°C	
Storage Temperature Range — Plastic — Ceramic	T _{stg}	-55 to +150 -55 to +165	°C °C	

ELECTRICAL CHARACTERISTICS (VEE = -5.2 V ±5%) (See Note)

Symbol	Min —	Max	Min	Max	Min	Max	Unit
ΙE	_	40				WIGH	
	Land Company of the	46	-	42	-	46	mA
linH	-	495	-	310	-	310	μΑ
linL	0.5	_	0.5	-	0.3	-	μΑ
VOH	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
VOL	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
VIH	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
VIL	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc
	V _O H V _O L V _I H	V _{OH} -1.02 V _{OL} -1.95 V _{IH} -1.17	V _{OH} -1.02 -0.84 V _{OL} -1.95 -1.63 V _{IH} -1.17 -0.84	V _{OH} -1.02 -0.84 -0.98 V _{OL} -1.95 -1.63 -1.95 V _{IH} -1.17 -0.84 -1.13	V _{OH} -1.02 -0.84 -0.98 -0.81 V _{OL} -1.95 -1.63 -1.95 -1.63 V _{IH} -1.17 -0.84 -1.13 -0.81	V _{OH} -1.02 -0.84 -0.98 -0.81 -0.92 V _{OL} -1.95 -1.63 -1.95 -1.63 -1.95 V _{IH} -1.17 -0.84 -1.13 -0.81 -1.07	V _{OH} -1.02 -0.84 -0.98 -0.81 -0.92 -0.735 V _{OL} -1.95 -1.63 -1.95 -1.63 -1.95 -1.60 V _{IH} -1.17 -0.84 -1.13 -0.81 -1.07 -0.735

AC PARAMETERS

Propagation Delay Enable Data	^t pd	0.7 0.7	2.2	0.7	2.0	0.7 0.7	2.2	ns
Rise Time	t _r	0.7	2.4	0.7	2.2	0.7	2.4	ns
Fall Time	tf	0.7	2.4	0.7	2.2	0.7	2.4	ns

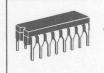
NOTE

Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50 ohm resistor to -2.0 volts.

This document contains information on a new product. Specifications and information herein are subject to change without notice.



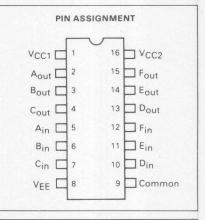
HEX BUFFER WITH ENABLE

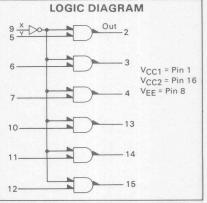


L SUFFIX CERAMIC PACKAGE CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648







TRUTH TABLE

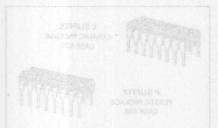
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- 8 Propagation Delay, 1.3 na Typical Data to Output
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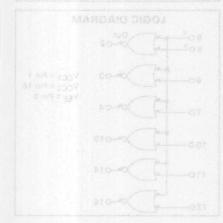
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-58 se +180 -85 to +185	

	0.0 T.0	2.1			
204					
					Fell Time











2

Advance Information

MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

The MC10H189 is a member of Motorola's new MECL family. The MC10H189 is a Hex Inverter with a common Enable input. The hex inverting function is provided when Enable is in the low-state. When Enable is in the high-state, all outputs are low.

This MECL 10KH part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay and no increase in power-supply current.

- Propagation Delay, 1.3 ns Typical Data-to-Output
- Power Dissipation 180 mW Typ/Pkg (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V _{CC} = 0)	VEE	-8.0 to 0	Vdc
Input Voltage (V _{CC} = 0)	VI	0 to VEE	Vdc
Output Current — Continuous — Surge	lout	50 100	mA
Operating Temperature Range	TA	0-+75	°C
Storage Temperature Range — Plastic — Ceramic	T _{stg}	-55 to +150 -55 to +165	°C

ELECTRICAL CHARACTERISTICS (VEE = -5.2 V ±5%) (See Note)

Characteristic	C	0	0°		25°		75°	
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	ΙE	-	46	_	42	-	46	mA
Input Current High	linH	-	495	-	310	-	310	μΑ
Input Current Low	linL	0.5	-	0.5	-	0.3	-	μΑ
High Output Voltage	Voн	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	VOL	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	VIH	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	VIL	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

AC PARAMETERS

Propagation Delay Enable Data	t _{pd}	0.7	2.2	0.7	2.1	0.7	2.3	ns
Rise Time	t _r	0.7	2.4	0.7	2.2	0.7	2.4	ns
Fall Time	tf	0.7	2.4	0.7	2.2	0.7	2.4	ns

NOTE:

Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50 ohm resistor to -2.0 volts.

This document contains information on a new product. Specifications and information herein are subject to change without notice.



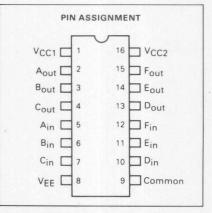
HEX INVERTER WITH ENABLE

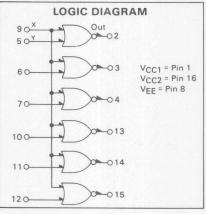


L SUFFIX CERAMIC PACKAGE CASE 620

P SUFFIX PLASTIC PACKAGE CASE 648





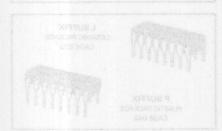




TRUTH TABLE

Inp	uts	Output
X	Υ	OUT
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L	Н	L
Н	L	L
Н	Н	L
	X L L	H L





				Rise Time

2-81

MECL 10KH HIGH-SPEED EMITTER—COUPLED LOGIC

The MC10H209 is a member of Motorola's new MECL family. It is a Dual 4–5-Input OR/NOR Gate. This MECL part is a functional/pinout duplication of the MECL III part MC1688.

- Propagation Delay Average, 0.75 ns Typical
- Power Dissipation 125 mW Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible





L SUFFIX CERAMIC PACKAGE CASE 620



P SUFFIX PLASTIC PACKAGE CASE 648

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V _{CC} = 0)	VEE	-8.0 to 0	Vdc
Input Voltage (V _{CC} = 0)	VI	0 to VEE	Vdc
Output Current — Continuous — Surge	lout	50 100	mA
Operating Temperature Range	TA	0-75	°C
Storage Temperature Range — Plastic — Ceramic	T _{stg}	-55 to +150 -55 to +165	°C

ELECTRICAL CHARACTERISTICS (VEE = -5.2 V ±5%) (See Note)

Characteristic	0	0)0	25°		75°		Unit
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	IE	_	-	-	30	-	_	mA
Input Current High	linH	-	640	-	400	-	400	μА
Input Current Low	linL	0.5	-	0.5	-	0.3	-	μА
High Output Voltage	VOH	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	VOL	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	VIH	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	VIL	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

AC PARAMETERS

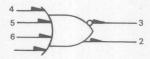
Propagation Delay	tpd	0.4	1.0	0.4	1.0	0.4	1,1	ns
Rise Time	tr	0.4	1.5	0.4	1.5	0.4	1.6	ns
Fall Time	tf	0.4	1.5	0.4	1.5	0.4	1.6	ns

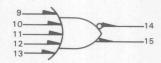
NOTE

Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained. Outputs are terminated through a 50 ohm resistor to -2.0 volts.

This document contains information on a new product. Specifications and information herein are subject to change without notice. MECL, MECL III, MECL 10K and MECL 10KH are trademarks of Motorola Inc.

Dual 4-5-Input OR/NOR Gate





V_{CC1} = Pin 1 V_{CC2} = Pin 16 V_{EE} = Pin 8



MC10H210 MC10H211

Advance Information

MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

The MC10H210 and MC10H211 are members of Motorola's new MECL family. These devices are dual 3-input, 3-output "OR" and "NOR" gates respectively. These MECL 10KH parts are functional/pinout duplications of the standard MECL 10K family parts, with 100% improvement in propagation delay and no increase in power-supply current.

- Propagation Delay, 1.0 ns Typical
- Power Dissipation, 160 mW Typical
- Improved Noise Margin 150 mV (over operating voltage and temperature range)
- Voltage Compensated
- MECL 10K-Compatible

MAXIMUM RATINGS

Symbol	Rating	Unit
VEE	-8.0 to 0	Vdc
VI	0 to VEE	Vdc
lout	50 100	mA
TA	0-75	°C
T _{stg}	-55 to 150 -55 to 165	°C °C
	VEE VI lout	VEE -8.0 to 0 VI 0 to VEE lout 50 100 TA 0-75 Tstg -55 to 150

ELECTRICAL CHARACTERISTICS (VFF = -5.2 V ±5%) (See Note)

Characteristic	0	0°		25°		7	Unit	
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	I _E	_	42	-	38	-	42	mA
Input Current High	linH	144-	720	-	450		450	μΑ
Input Current Low	linL	0.5	-	0.5	200	0.3		μА
High Output Voltage	VOH	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	VOL	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	VIH	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	VIL	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

AC PARAMETERS

Propagation Delay	tpd	0.7	1.6	0.7	1.5	0.7	1.7	ns
Rise Time	tr	0.7	2.2	0.7	2.0	0.7	2.2	ns
Fall Time	tf	0.7	2.2	0.7	2.0	0.7	2.2	ns

*Pin 1 and 15 internally connected.

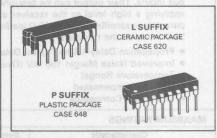
NOTE:

Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater then 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

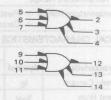
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Note: If crosstalk is present, double bypass capacitor to $0.2\mu F$.



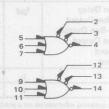


MC10H210 3-INPUT 3-OUTPUT "OR" GATE



V_{CC1} = Pin 1, 15* V_{CC2} = Pin 16 V_{EE} = Pin 8

MC10H211 3-INPUT 3-OUTPUT "NOR" GATE





Advance Information

QUAD BUS DRIVER/RECEIVER WITH 2-TO-1 OUTPUT MULTIPLEXERS

The MC10H330 is a member of Motorola's new MECL family. The MC10H330 is a Quad Bus Driver/Receiver with two-to-one output multiplexers. These multiplexers have a common select and output enable. When disabled, $(\overline{OE}=\text{high})$ the bus outputs go to -2.0 V. The receivers have 200 mV of hysteresis on their bus inputs. Their output can be brought to a low state (VOL) by applying a high level to the receiver enable $(\overline{RE}=\text{High}).$ The parameters specified are with 25 Ω loading on the bus drivers and 50 Ω loads on the receivers.

- Propagation Delay 1.5 ns Typical Data-to-Output
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V _{CC} = 0)	VEE	-8.0 to 0	Vdc
Input Voltage (V _{CC} = 0)	VI	0 to VEE	Vdc
Output Current — Continuous — Surge	lout	50 100	mA
Operating Temperature Range	TA	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T _{stg}	-55 to +150 -55 to +165	℃

ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2 V ±5.0%) (See Note)

	0	()°	25°		75°C		-
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	ΙE	_	157	_	143	1	157	mA
Input Current High Pins 5-8, 17-20 Pins 16, 21 Pin 9	linH	=	667 514 475		417 321 297	M <u>1</u> a0	417 321 297	μΑ
Input Current Low	linL	0.5	-	0.5	10	0.3	1084	μΑ
High Output Voltage	Vон	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	VOL	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	VIH	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	VIL	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

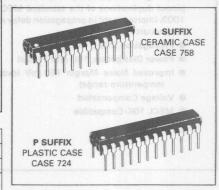
AC PARAMETERS

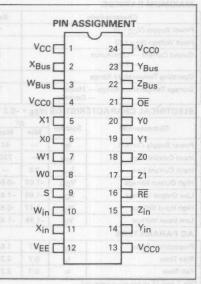
Propagation Delay	tpd			8	1 1 1		6.1	ns
Data-to-Bus Output	Pu	0.8	2.0	0.8	2.0	0.8	2.2	1 18
Select-to-Bus Output		1.0	3.2	1.0	3.2	1.0	3.4	1 5
OE-to-Bus Output		1.0	2.4	1.0	2.4	1.0	2.5	
Bus-to-Input	E	0.8	2.1	0.8	2.1	0.8	2.4	
RE-to-Input		0.8	2.2	0.8	2.2	0.8	2.5	ng chia
Rise Time	tr	0.8	2.0	0.8	2.0	0.8	2.0	ns
Fall Time	tf	0.8	2.0	0.8	2.0	0.8	2.0	ns

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QUAD BUS DRIVER/RECEIVER WITH 2-TO-1 OUTPUT MULTIPLEXERS

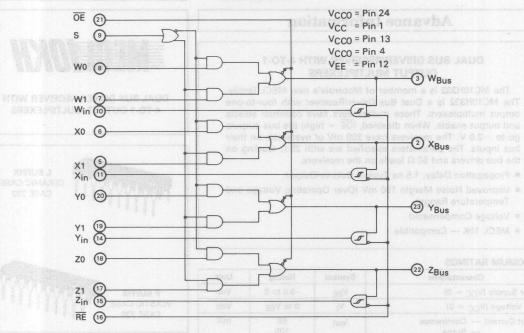




NOTE

Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

LOGIC DIAGRAM



MULTIPLEXER TRUTH TABLE

OE	S	W _{Bus}	X _{Bus}	YBus	Z _{Bus}		
Н	X	-2.0 V	-2.0 V	-2.0 V	-2.0 V		
L	L	WO	X0	Y0	Z0		
L	H	W1	X1	Y1	Z1		

RECEIVER TRUTH TABLE

RE	Win	Xin	Yin	Zin
H	L	Pajuni	□ L	. L
ooil) (de	W _{Bus}	X _{Bus}	YBus	Z _{Bus}

X — Don't care

DUAL BUS DRIVER/RECEIVER WITH 4-TO-1 OUTPUT MULTIPLEXERS

The MC10H332 is a member of Motorola's new MECL family. The MC10H332 is a Dual Bus Driver/Receiver with four-to-one output multiplexers. These multiplexers have common selects and output enable. When disabled, $(\overline{OE} = high)$ the bus outputs go to -2.0 V. The receivers have 200 mV of hysteresis on their bus inputs. The parameters specified are with 25 Ω loading on the bus drivers and 50 Ω loads on the receivers.

- Propagation Delay, 1.5 ns Typical Data-to-Output
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K Compatible

MAXIMUM RATINGS

MAXIMOM HATINGO		7 1-1			
Characteristic	Symbol	Rating	Unit		
Power Supply (V _{CC} = 0)	VEE	-8.0 to 0	Vdc		
Input Voltage (V _{CC} = 0)	VI	0 to VEE	Vdc		
Output Current — Continuous — Surge	lout	50 100	mA		
Operating Temperature Range	TA	0 to +75	°C		
Storage Temperature Range — Plastic — Ceramic	T _{stg}	-55 to +150 -55 to +165	°€		

ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2 V ±5.0%) (See Note)

		()°	25°		75°C		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	ΙE		115		110	_	115	mA
Input Current High Pins 3,4,5,6,14,15,16,17 Pins 7,8 Pin 13,18	linH	=	667 437 456	=	417 273 285	=	417 273 285	μΑ
Input Current Low	linL	0.5	_	0.5	-	0.3	_	μΑ
High Output Voltage	Vон	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	VOL	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	VIH	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	VIL	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

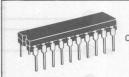
AC PARAMETERS

Propagation Delay	tpd							ns
Data-to-Bus Output		0.8	3.2	1.0	3.2	1.0	3.4	
Select-to-Bus Output	1.35	0.8	3.6	1.0	3.6	1.0	4.0	666
OE-to-Bus Output		0.8	2.4	0.8	2.2	0.8	2.6	
Bus-to-Input		0.8	2.1	0.8	2.1	0.8	2.4	
RE-to-Input		0.8	2.2	0.8	2.2	0.8	2.5	
Rise Time	tr	0.5	2.0	0.8	2.0	0.8	2.0	ns
Fall Time	tf	0.5	2.0	0.8	2.0	0.8	2.0	ns

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.



DUAL BUS DRIVER/RECEIVER WITH 4-TO-1 OUTPUT MULTIPLEXERS



L SUFFIX CERAMIC CASE **CASE 732**

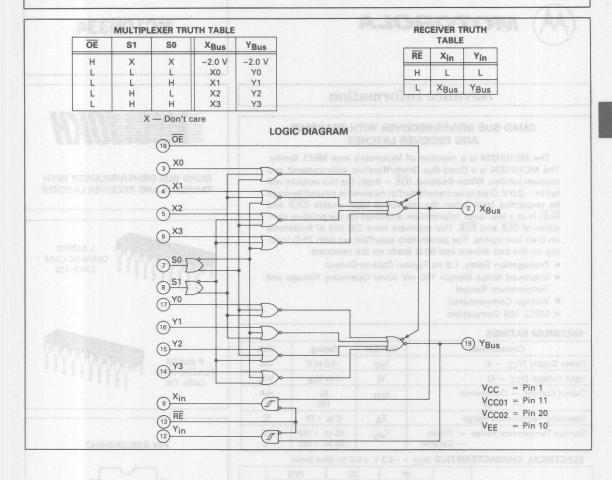
P SUFFIX PLASTIC CASE **CASE 738**



PIN ASSIGNMENT



Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 Ifpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.





Advance Information

QUAD BUS DRIVER/RECEIVER WITH TRANSMIT AND RECEIVER LATCHES

The MC10H334 is a member of Motorola's new MECL family. The MC10H334 is a Quad Bus Driver/Receiver with transmit and receiver latches. When disabled, $(\overline{OE}=\text{high})$ the bus outputs will fall to -2.0 V. Data to be transmitted or received is passed through its respective latch when the respective latch enable $(\overline{DLE}$ and $\overline{RLE})$ is at a low level. Information is latched on the positive transition of \overline{DLE} and \overline{RLE} . The receivers have 200 mV of hysteresis on their bus inputs. The parameters specified are with 25 Ω loading on the bus drivers and 50 Ω loads on the receivers.

- Propagation Delay, 1.6 ns Typical Data-to-Output
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

MAXIMUM RATINGS

WAXINOW HATINGO			
Characteristic	Symbol	Rating	Unit
Power Supply (V _{CC} = 0)	VEE	-8.0 to 0	Vdc
Input Voltage (V _{CC} = 0)	VI	0 to VEE	Vdc
Output Current — Continuous — Surge	lout	50 100	mA
Operating Temperature Range	TA	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T _{stg}	-55 to +150 -55 to +165	℃ ℃

ELECTRICAL CHARACTERISTICS (VEE = -5.2 V ±5.0 %) (See Note)

		()°	25°		75°C			
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit	
Power Supply Current	ΙE	-	161	_	161	-	161	mA	
Input Current High Pins 5,6,15,16 Pin 7, 14 Pin 17	linH	=	397 460 520	=	273 297 357	_	273 297 357	μΑ	
Input Current Low	linL	0.5	-	0.5	_	0.3	_	μΑ	
High Output Voltage	VOH	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc	
Low Output Voltage	VOL	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc	
High Input Voltage	VIH	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc	
Low Input Voltage	VIL	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc	

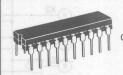
AC PARAMETERS

Propagation Delay	tpd							ns
Data-to-Bus Output		0.5	2.5	0.5	2.5	0.5	2.5	1
DLE-to-Bus Output		1.0	2.7	1.0	2.7	1.0	3.0	
OE-to-Bus Output		0.5	2.5	0.5	2.5	0.5	2.5	
Bus-to-R0		0.5	1.9	0.5	1.9	0.5	1.9	
RLE-to-R0		0.5	2.1	0.5	2.0	0.5	2.1	
Rise Time	tr	0.8	2.2	0.7	2.0	0.8	2.2	ns
Fall Time	tf	0.8	2.2	0.7	2.0	0.8	2.2	ns

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ME TOKH

QUAD BUS DRIVER/RECEIVER WITH TRANSMIT AND RECEIVER LATCHES

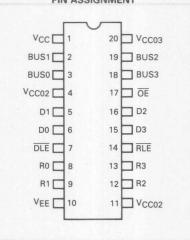


L SUFFIX CERAMIC CASE

P SUFFIX PLASTIC CASE CASE 738

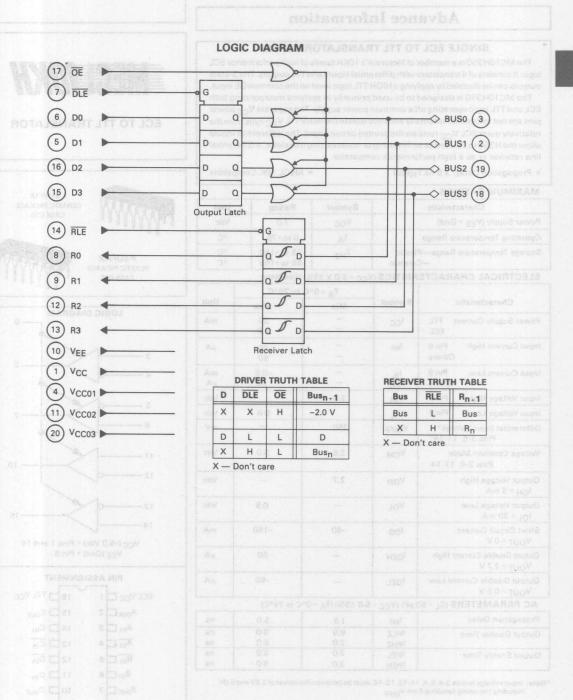


PIN ASSIGNMENT



NOTE

Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.



SINGLE ECL TO TTL TRANSLATOR SUPPLY

The MC10H350 is a member of Motorola's 10KH family of high performance ECL logic. It consists of 4 translators with differential inputs and TTL outputs. The 3-state outputs can be disabled by applying a HIGH TTL logic level on the common OE input.

The MC10H350 is designed to be used primarily in systems incorporating both ECL and TTL logic operating off a common power supply. The separate V_{CC} power pins are not connected internally and thus isolate the noisy TTL V_{CC} runs from the relatively quiet ECL V_{CC} runs on the printed circuit board. The differential inputs allow the H350 to be used as an inverting or noninverting translator, a differential line receiver or as a high performance comparator.

· Propagation Delay, 3.5 ns Typical

• MECL 10K-Compatible

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (VEE = Gnd)	Vcc	7.0	Vdc
Operating Temperature Range	TA	0 to +75	°C
Storage Temperature Range—Plastic —Ceramic	T _{stg}	-55 to +150 -55 to +165	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ±5%) (See Note)

Characteristic	Symbol	T _A = 0°C to 75°C		
		Min	Max	Unit
Power Supply Current TTL ECL	lcc		20 5.0	mA
Input Current High Pin 9 Others	Iн	_ ask	20 50	μА
Input Current Low Pin 9 Others	IIL	_ austr	-0.6 50	mA μA
Input Voltage High Pin 9	VIH	2.0	30 - BUG	Vdc
Input Voltage Low Pin 9	VIL	V 0.5-	0.8	Vdc
Differential Input Voltage* Pins 3-6, 11-14*	VDIFF	350		mV
Voltage Common Mode Pins 3-6, 11-14	V _{CM}	2.8	5.0	Vdc
Output Voltage High IOH = 3 mA	Voн	2.7	-	Vdc
Output Voltage Low I _{OL} = 20 mA	VOL		0.5	Vdc
Short Circuit Current VOUT = 0 V	los	-60	-150	mA
Output Disable Current High V _{OUT} = 2.7 V	Гохн		50	μΑ
Output Disable Current Low VOUT = 0.5 V	IOZL	-	-50	μА

AC PARAMETERS (CL = 50 pF) (VCC = 5.0 ±5%) (TA = 0°C to 75°C)

Propagation Delay	t _{pd}	1.5	5.0	ns
Output Disable Time	tPLZ	2.0	6.0	ns
	tPHZ	2.0	6.0	ns
Output Enable Time	tpZL	2.0	8.0	ns
	tPZH	2.0	8.0	ns

*Note: Input voltalge to pins 3-4, 5-6, 11-12, 13-14, must be between the values of 2.8V and 5.0V including the swing resulting from V_{DIFF}



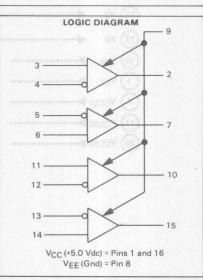
ECL TO TTL TRANSLATOR

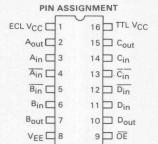


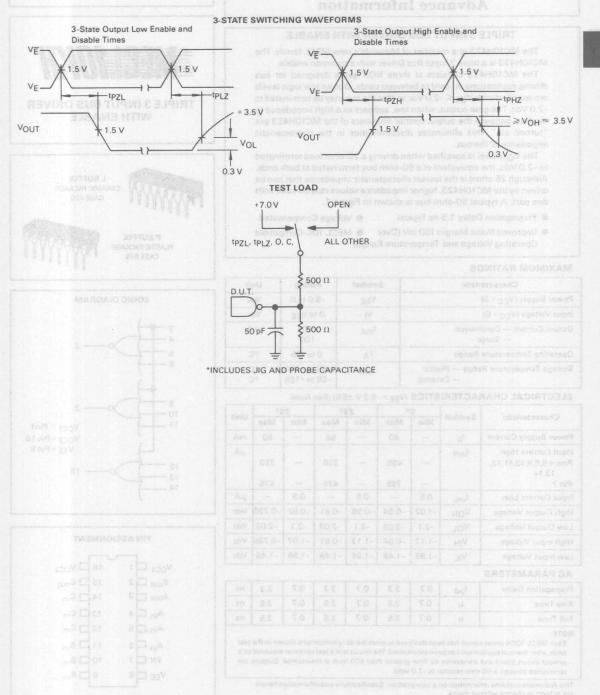
L SUFFIX CERAMIC PACKAGE CASE 620

P SUFFIX PLASTIC PACKAGE CASE 648









MC10H423

Advance Information

TRIPLE 3 INPUT BUS DRIVER WITH ENABLE

The MC10H423 is a member of Motorola's new MECL family. The MC10H423 is a triple 3 Input Bus Driver with a common enable.

The MC10H423 consists of three NOR gates designed for bus driving applications on card or between cards. Output low logic levels are specified with VOL ≤ -2.0 Vdc so that the bus may be terminated to -2.0 Vdc. The gate output, when low, appears as a high impedance to the bus, because the output emitter-followers of the MC10H423 are "turned off." This eliminates discontinuities in the characteristic impedance of the bus.

The VOH level is specified when driving a 25-ohm load terminated to -2.0 Vdc, the equivalent of a 50-ohm bus terminated at both ends. Although 25 ohms is the lowest characteristic impedance that can be driven by the MC10H423, higher impedance values may be used with this part. A typical 50-ohm bus is shown in Figure 1.

- Propagation Delay, 1.5 ns Typical
- Voltage Compensated
- Improved Noise Margin 150 mV (Over MECL 10K-Compatible Operating Voltage and Temperature Range)

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V _{CC} = 0)	VEE	-8.0 to 0	Vdc
Input Voltage (V _{CC} = 0)	. VI	0 to VEE	Vdc
Output Current — Continuous — Surge	lout	50 100	mA
Operating Temperature Range	TA	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T _{stg}	-55 to +150 -55 to +165	°C

ELECTRICAL CHARACTERISTICS (VEE = -5.2 V ±5%) (See Note)

Characteristic	Combat	()°	2	5°	7	5°	
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	1E	-	60	-	56	-	60	mA
Input Current High Pins 4,5,6,9,10,11,12, 13,14 Pin 7	linH	-	495 765	-	310 475	-	310 475	μА
Input Current Low	linL	0.5	-	0.5	-	0.3	-	μΑ
High Output Voltage	Voн	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	VOL	-2.1	-2.03	-2.1	-2.03	-2.1	-2.03	Vdc
High Input Voltage	VIH	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	VIL	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

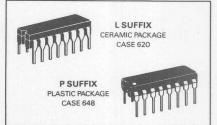
AC PARAMETERS

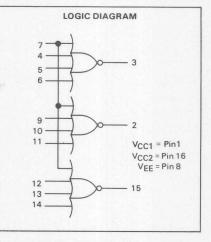
Propagation Delay	tpd	0.7	2.3	0.7	2.3	0.7	2.3	ns
Rise Time	t _r	0.7	2.5	0.7	2.5	0.7	2.5	ns
Fall Time	tf	0.7	2.5	0.7	2.5	0.7	2.5	ns

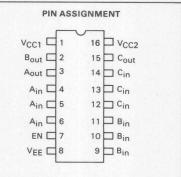
Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 Ifpm is maintained. Outputs are terminated through a 50 ohm resistor to -2.0 volts.

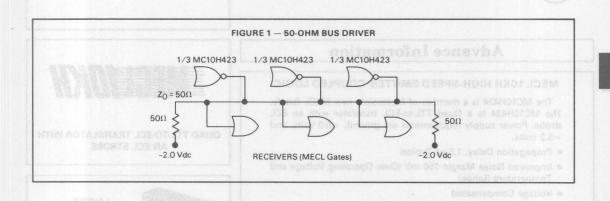
This document contains information on a new product. Specifications and information herein are subject to change without notice.

TRIPLE 3 INPUT BUS DRIVER WITH ENABLE











ow input Voltage Pln X,10,11				

MC10H424

2

Advance Information

MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

The MC10H424 is a member of Motorola's new MECL family. The MC10H424 is a Quad TTL-to-ECL translator with an ECL strobe. Power supply requirements are ground, +5.0 volts, and -5.2 volts.

- Propagation Delay, 1.5 ns Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K -Compatible

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V _{CC} = 5.0 V)	VEE	-8.0 to 0	Vdc
Power Supply (VEE = -5.2 V)	Vcc	0 to +7.0	Vdc
Input Voltage (ECL)	VI	0 to VEE	Vdc
Input Voltage (TTL)	VI	0 to VCC	Vdc
Output Current — Continuous — Surge	lout	50 100	mA
Operating Temperature Range	TA	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T _{stg}	-55 to +150 -55 to +165	°C

ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2 V \pm 5%, V_{CC} = 5.0 V \pm 5.0%)

)°	2	5°	7!	5°C	
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Negative Power Supply Drain Current	IE	-	72	-	66	-	72	mAdd
Positive Power Supply	ІССН	_	16	_	16	_	18	mAdd
Drain Current	ICCL	-	25	-	25	-	25	mAdd
Reverse Current Pin 5,7,10,11	IR	-	50	-	50	-	50	μAdo
Forward Current Pin 5,7,10,11	IF	-	-3.2	-	-3.2	-	-3.2	mAdd
Input HIGH Current Pin 6	linH	-	450	_	310	_	310	μAdo
Input LOW Current Pin 6	linL	0.5	_	0.5	-	0.3	_	μAdo
Input Breakdown Voltage	V(BR)in	5.5	-	5.5	_	5.5	_	Vdc
Input Clamp Voltage	VI	_	-1.5	_	-1.5	_	-1.5	Vdc
High Output Voltage	VOH	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	VOL	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage Pin 5,7,10,11	VIH	2.0	-	2.0	-	+2.0	-	Vdc
Low Input Voltage Pin 5,7,10,11	VIL	-	0.8	-	0.8	-	0.8	Vdc
High Input Voltage Pin 6	VIH	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage Pin 6	VIL	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

This document contains information on a new product. Specifications and information herein are subject to change without notice.



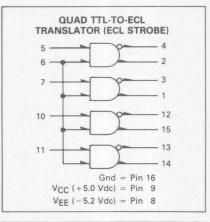
QUAD TTL-TO-ECL TRANSLATOR WITH AN ECL STROBE

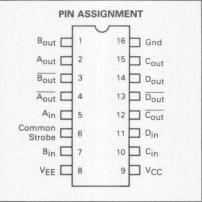


L SUFFIX CERAMIC PACKAGE CASE 620

P SUFFIX PLASTIC PACKAGE CASE 648







AC PARAMETERS

Propagation Delay	tpd	0.7	3.4	0.7	3.0	0.7	3.4	ns
Rise Time	tr	0.5	2.2	0.5	2.0	0.5	2.2	ns
Fall Time	tf	0.5	2.2	0.5	2.0	0.5	2.2	ns

NOTE:

Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 ffpm is maintained. Outputs are terminated through a 50-ohm resistor to $-2.0\,\mathrm{volts}$.

APPLICATIONS INFORMATION

The MC10H424 has TTL-compatible inputs, an ECL strobe and MECL complementary open-emitter outputs that allow use as an inverting/non-inverting translator or as a differential line driver. When the common strobe input is at the low-logic level, it forces all true outputs to a MECL low-logic state and all inverting

outputs to a MECL high-logic state.

An advantage of this device is that TTL-level information can be transmitted differentially, via balanced twisted pair lines, to MECL equipment, where the signal can be received by the MC10H115 or MC10H116 differential line receivers.

Back MIRCL 100th arrive of cut if her bean designed as most the depole ifficultions shown in the test labble, after fragmal equilibrium has been establighted. The cut suit is in a cast model or mourned on a print of create break and renewers as flow greater than 500 figure as not the than 100 figure as not the tained. Outgoing programmented through a 50 of more about to ~20 volts.

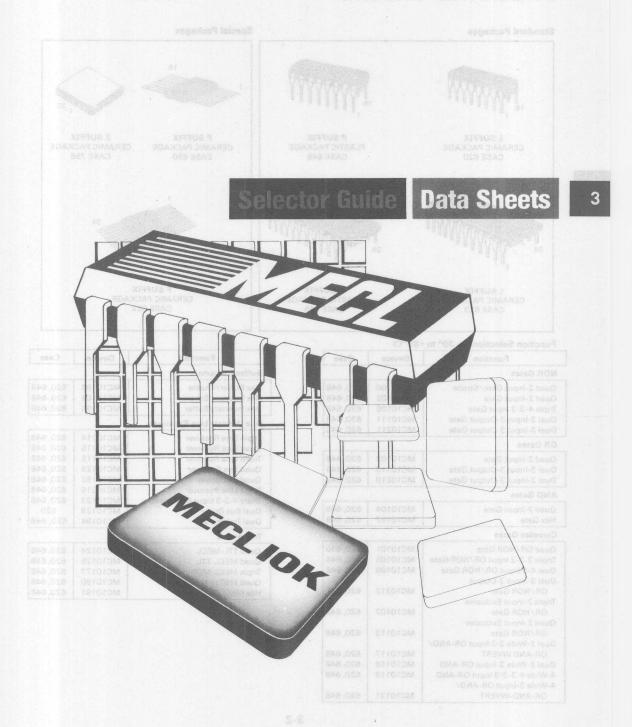


The McnoHaza has TTL-compatible inputs, an ECL strope and MECL complementary open emitter outputs that allow use as an invertingmon-inverting transition or as a differential line driver. When the continon strope input is at the low-logic level, it forces all true outputs to a MECL low-logic state and all inverting

authors to a MECL high-logic state.

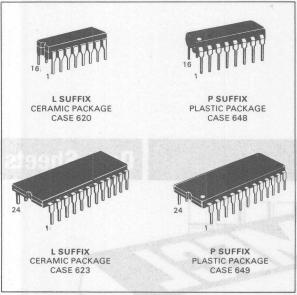
An edvantage of this device is that TTL-level infornation cash be treasmitted differentially, via balanced
wisted pair lines, to MECL equipment where the sigall cash be received by the MC10H115 or MC10H116
lifterential line receivers.

MECL 10K INTEGRATED CIRCUITS



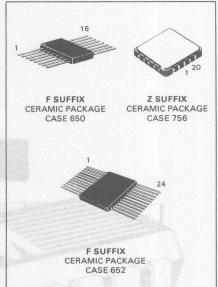
3-1

Standard Packages



Function Device Case

Special Packages



Function Selection—(-30° to +85°C)

runction	Device	Case
NOR Gates		
Quad 2-Input Gate/Strobe	MC10100	620, 648
Quad 2-Input Gate	MC10102	620, 648
Triple 4-3-3 Input Gate	MC10106	620, 648
Dual 3-Input 3-Output Gate	MC10111	620, 648
Dual 3-Input 3-Output Gate	MC10211	620, 648
OR Gates		
Quad 2-Input Gate	MC10103	620, 648
Dual 3-Input 3-Output Gate	MC10110	620, 648
Dual 3-Input 3-Output Gate	MC10210	620, 648
AND Gates		
Quad 2-Input Gate	MC10104	620, 648
Hex Gate	MC10197	620, 648
Complex Gates		
Quad OR/NOR Gate	MC10101	620, 648
Triple 2-3-2 Input OR/NOR Gate	MC10105	620, 648
Dual 4-5 Input OR/NOR Gate Dual 3-Input 3-Output	MC10109	620, 648
OR/NOR Gate	MC10212	620, 648
Triple 2-Input Exclusive		
OR/NOR Gate	MC10107	620, 648
Quad 2-Input Exclusive		
OR/NOR Gate	MC10113	620, 648
Dual 2-Wide 2-3 Input OR-AND/		
OR-AND INVERT	MC10117	620, 648
Dual 2-Wide 3-Input OR-AND	MC10118	620, 648
4-Wide 4-3-3-3 Input OR-AND 4-Wide 3-Input OR-AND/	MC10119	620, 648
OR-AND-INVERT	MC10121	620, 648

Function	Device	Case
Buffers/Inverters		
Hex Buffer/Enable	MC10188	620, 648
Hex Inverter/Enable	MC10189	620, 648
Hex Inverter/Buffer	MC10195	620, 648
Line Drivers/Line Receivers	La Haman	
Triple Line Receiver	MC10114	620, 648
Quad Line Receiver	MC10115	620, 648
Triple Line Receiver	MC10116	620, 648
Quad Bus Receiver	MC10129	620, 648
Quad Bus Driver	MC10192	620, 648
Triple Line Receiver	MC10216	620, 648
Triple 4-3-3 Input Bus Driver	MC10123	620, 648
Dual Bus Driver	MC10128	620
Dual Transceiver	MC10194	620, 648
Translators		
Quad TTL-MECL	MC10124	620, 648
Quad MECL-TTL	MC10125	620, 648
Triple MECL-MOS	MC10177	620, 648
Quad MST to MECL	MC10190	620, 648
Hex MECL-MST	MC10191	620, 648

Function	Device	Case
Flip-Flop/Latches		
Dual D Master Slave Flip-Flop	MC10131	620, 648
Dual J-K Master Slave Flip-Flop	MC10135	620, 648
Hex D Master Slave Flip-Flop	MC10176	620, 648
Hex D Common Reset Flip-Flop	MC10186	620, 648
Dual D Master Slave Flip-Flop	MC10231	620, 648
Quad Latch	MC10133	620, 648
Quint Latch	MC10175	620, 648
Quad/Common Clock Latch	MC10168	620, 648
Quad/Negative Clock Latch	MC10153	620, 648
Dual Latch	MC10130	620, 648
ncoders		
8-Input Encoder	MC10165	620, 648
Decoders All Calling		
Binary to 1-8 (Low)	MC10161	620, 648
Binary to 1-8 (High)	MC10162	620, 648
Dual Binary to 1-4 (Low)	MC10171	620, 648
Dual Binary to 1-4 (High)	MC10172	620, 648
Parity Generator/Checkers		
12-Bit Parity Generator-Checker	MC10160	620, 648
9 + 2 Bit Parity	MC10170	620, 648
Error Detector/Correction		
IBM Code	MC10163	620, 64
		620, 64

Function	Device	Case
Counters		
Hexadecimal	MC10136	620, 648
Decade	MC10137	620, 648
Biquinary	MC10138	620, 648
Binary Down Counter	MC10154	620, 648
Binary	MC10178	620, 648
Arithmetic Functions		
5-Bit Magnitude Comparator	MC10166	620, 648
Look Ahead Carry Block	MC10179	620, 648
Dual 2-Bit Adder/Subtractor	MC10180	620, 648
4-Bit Arithmetic Function Gen.	MC10181	620, 648
2-Bit Arithmetic Function Gen.	MC10182	620, 648
4 × 2 Multiplier	MC10183	623
2-Bit Multiplier	MC10287	620, 648
Shift Register	E ADDRONAL A	
4-Bit Universal	MC10141	620, 64
Multivibrators	awag	Tuol
Monostable Multivibrators	MC10198	620, 64
Multiplexer		
Quad 2-Input/Noninverting	MC10158	620, 64
Dual Multiplexer/Latch	MC10132	620, 64
Dual Multiplexer/Latch	MC10134	620, 64
Quad 2-Input/Inverting	MC10159	620, 64
8-Line	MC10164	620, 64
Quad 2-Input/Latch	MC10173	620, 64
Dual 4-1	MC10174	620, 64





QUAD 2-INPUT NOR GATE WITH STROBE

The MC10100 is a quad NOR gate. Each gate has 3 inputs, two of which are independent and one of which is tied common to all four gates.

P_D = 25 mW typ/gate (No Load)

 $t_{pd} = 2.0 \text{ ns typ}$

 t_{r} , $t_{f} = 2.0$ ns typ (20-80%)

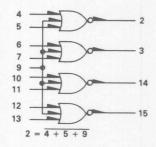
MECL 10K SERIES

QUAD 2-INPUT NOR GATE WITH STROBE

P SUFFIX
PLASTIC PACKAGE
CASE 648

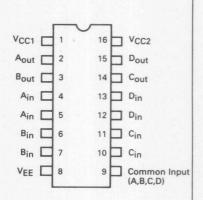
L SUFFIX CERAMIC PACKAGE CASE 620

LOGIC DIAGRAM



V_{CC1} = Pin 1 V_{CC2} = Pin 16 V_{EE} = Pin 8

PIN ASSIGNMENT



		TEST V	OLTAGE	VALUES		
			(Volts)	123	150	_
@ Test Temperature	VIHmax	VILmin	VIHAmin	VILAmax	VEE	
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2	
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2	
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2	

										+85°C	-0.700	-1.825	-1.035	-1.440	-5.2	-
		Pin			M		Test Limit							PLIED TO		
		Under	-30	o°C		+25°C		+8!	5°C			-	ISTED BE			(VCC)
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	VIHmax	VILmin	VIHAmin	VILAmax	VEE	Gnd
Power Supply Drain Current	1E	8	_	29	-	21	26	_	29	mAdc	_	_	- 8	-	8	1,16
Input Current	linH	4* 9		390 750	-	-	245 470	_	245 470	μAdc μAdc	4* 9	=	- 8	_	8	1,16
	linL	4*	0.5	-	0.5	-	-	0.3	_	μAdc	-	4*		-	8	1,16
Logic "1" Output Voltage	Vон	2 14	-1.060 -1.060	-0.890 -0.890	-0.960 -0.960	-	-0.810 -0.810	-0.890 -0.890	-0.700 -0.700	Vdc Vdc	_	=	1 200		8	1,16 1,16
Logic "0" Output Voltage	VOL	2 14	-1.890 -1.890	-1.675 -1.675	-1.850 -1.850	=	-1.650 -1.650	-1.825 -1.825	-1.615 -1.615	Vdc Vdc	4,5,9 9,10,11	=	- 1	_	8	1,16 1,16
Logic "1" Threshold Voltage	VOHA	2 3 14 15	-1.080 -1.080 -1.080 -1.080	-	-0.980 -0.980 -0.980 -0.980	- 10- 10-	-	-0.910 -0.910 -0.910 -0.910	-	Vdc	- 1974	dulolit	1 200	9 9 9	8	1,16
Logic "0" Threshold Voltage	VOLA	2 3 14 15		-1.655 -1.655 -1.655 -1.655		\$- 9_	-1.630 -1.630 -1.630	- - -	-1.595 -1.595 -1.595 -1.595	Vdc	1917	-	9 9 9	0.00	8	1,16
Switching Times (50-ohm load)	H					Ĉ.					977	W.	Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t ₄₊₂₋ t ₄₋₂₊	2 2	1.0 1.0	3.1 3.1	1.0 1.0	2.0	2.9 2.9	1.0 1.0	3.3 3.3	ns	10	200	4 9	2	8	1,16
Rise Time (20% to 80%)	t ₂₊	2	1.1	3.6	1.1		3.3	1.1	3.7			9	13			
Fall Time (20% to 80%)	t ₂₋	2	1.1	3.6	1.1	V	3.3	1,1	3.7	V			1	V	V	1

^{*}Individually test each input applying $V_{\mbox{\scriptsize IH}}$ or $V_{\mbox{\scriptsize IL}}$ to input under test.



MC10101

QUAD OR/NOR GATE

The MC10101 is a quad 2-input OR/NOR gate with one input from each gate common to pin 12.

P_D = 25 mW typ/gate (No Load)

 $t_{pd} = 2.0 \text{ ns typ}$

 t_r , $t_f = 2.0$ ns typ (20%–80%)

MECL 10K SERIES

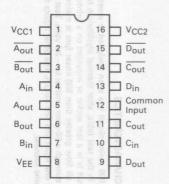
QUAD OR/NOR GATE

P SUFFIX PLASTIC PACKAGE CASE 648

LSUFFIX

CERAMIC PACKAGE CASE 620

PIN ASSIGNMENT



LOGIC DIAGRAM 10 -12 -V_{CC1} = Pin 1 V_{CC2} = Pin 16 V_{EE} = Pin 8

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

	- 1000	TEST	VOLTAGE VAL	UES	
	2-160V		(Volts)	63	166
@ Test Temperature	VIH max	V _{IL min}	VIHA min	VILA max	VEE
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

										+85°C	-0.700	-1.825	-1.035	-1.440	-5.2	
		Pin			N		Test Li				TEST	VOLTAGE A	PPLIED TO PIN	S LISTED BELO	W:	
		Under	-	o°C		+25°C	-		5°C							(Vcc
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	V _{IH} max	VIL min	VIHA min	VILA max	VEE	Gnd
Power Supply Drain Current	1E	8	-	29	-	20	26	-	29	mAdc		1-1	-		8	1,16
Input Current	linH	4	-	425	-	-	265	-	265	μAdc	4		-	0 -	8	1,16
		12	-	850	-	-	535	-	535	μAdc	12		=	5 -	8	1,16
	linL	4	0.5	-	0.5	-	-	0.3	-	μAdc	-	4		12 kg = 1.11	8	1,16
		12	0.5	-	0.5	-	-	0.3	-	μAdc	-	12		(a) -	8	1,16
Logic "1"	VOH	5	-1.060	-0.890	-0.960	-	-0.810	-0.890	-0.700	Vdc	12		-	9-	8	1,16
Output Voltage		5	-1.060	-0.890	-0.960	-	-0.810	-0.890	-0.700	1	4	-		13-		
		2	-1.060	-0.890	-0.960	-	-0.810	-0.890	-0.700		-			8-		
		2	-1.060	-0.890	-0.960	-,	-0.810	-0.890	-0.700	V	_	JUL - 0.6	92	-	V	Y
Logic "0"	VOL	5	-1.890	-1.675	-1.850	-	-1.650	-1.825	-1.615	Vdc		- 5	-	2 - 10	8	1,16
Output Voltage		5	-1.890	-1.675	-1.850	-	-1.650	-1.825	-1.615		-	- 16	2	- 33		
		2	-1.890	-1.675	-1.850	-	-1.650	-1.825	-1.615		12	- 35	3	6 - 50		
		2	-1.890	-1.675	-1.850	-	-1.650	-1.825	-1.615		4	- 1	17	5 - 73	٧	
Logic "1"	VOHA	5	-1.080	-	-0.980	-	-1	-0.910	-	Vdc	-	- 3	12	77 - 44	8	1,16
Threshold Voltage		5	-1.080	-	-0.980	-	7	-0.910	-		-	- 10	4	2- 3	100	
2 2 2		2	-1.080	-	-0.980	-		-0.910	-		-	-	20 00	12	1	-
36 3 3	- 7	2	-1.080	19	-0.980	-	-47	-0.910	-		-		-	4	V	
Logic "0"	VOLA	5	11-	-1.655	-	-	-1.630	-	-1.595	Vdc	-	- 10	a =	12	8	1,16
Threshold Voltage		5	-	-1.655	-	-	-1.630	-	-1.595			- 4	3 3	4		0
11.00		2		-1.655	-	-	-1.630	-	-1.595			- 9	12	- X - X		
< 6.01		2	- 1	-1.655	-		-1.630	-	-1.595			- 19	4	图 10- 雪	V	V
Switching Times (50-ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0
Propagation Delay	t4+2-	2	1.0	3.1	1.0	2.0	2.9	1.0	3.3	ns		- 4	4	2	8	1,16
	t4-2+	2			1	1	1	1		1	_			2	1-	1
	t4+5+	5							1			_		5		
	t4-5-	5			-			-			_			5		
Rise Time	t ₂₊	2	1,1	3.6	1.1		3.3	1.1	3.7		_	- 1		2		11
(20 to 80%)	t5+	5			1		1	1			-	-		5		
Fall Time	t2-	2									_			0 02		
(20 to 80%)	t5-	5	1	1			1		-	-				5		V

QUAD 2-INPUT NOR GATE

The MC10102 is a quad 2-input NOR gate. The MC10102 provides one gate with OR/NOR outputs.

P_D = 25 mW typ/gate (No Load)

 $t_{pd} = 2.0 \text{ ns typ}$

 t_r , $t_f = 2.0 \text{ ns typ } (20\%-80\%)$

MECL 10K SERIES

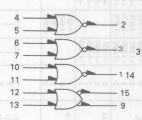
QUAD 2-INPUT NOR GATE



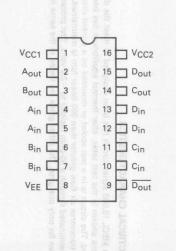
P SUFFIX
PLASTIC PACKAGE
CASE 648



LOGIC DIAGRAM



V_{CC1} = Pin 1 V_{CC2} = Pin 16 V_{EE} = Pin 8 PIN ASSIGNMENT



3-8

		TEST	VOLTAGE VAL	UES	- 0
			(Volts)	- 5	
@ Test Temperature	VIH max	VIL min	VIHA min	VILA max	VEE
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

										100 C	-0.700	-1.025	-1.035	-1.440	-5.2	
	Pin MC10102 Test Limits									TES	T VOLTAGE A	PPI IED TO PIN	S LISTED BELO	w.	1 1	
		Under	-30	o°C		+25°C		+8	5°C		1.20	TOLINGER	1	1		(VCC
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	VIH max	VIL min	VIHA min	VILA max	VEE	Gnd
Power Supply Drain Current	1 _E	8	-	29	-	20	26	-	29	mAdc					8	1,16
Input Current	linH	12	-	425	-	-	265	+	265	μAdc	12		-50.0	2 =	8	1,16
	linL	12	0.5	-	0.5	-	-	0.3		μAdc		12		P. 2	8	1,16
Logic "1" Output Voltage	VOH	9 9 15 15	-1.060 -1.060 -1.060 -1.060	-0.890 -0.890 -0.890 -0.890	-0.960 -0.960 -0.960 -0.960	-	-0.810 -0.810 -0.810 -0.810	-0.890 -0.890 -0.890 -0.890	-0.700 -0.700 -0.700 -0.700	Vdc	12 13 - -	-	= -	014 88	8	1,16
Logic "0" Output Voltage	VOL	9 9 15 15	-1.890 -1.890 -1.890 -1.890	-1.675 -1.675	-1.850 -1.850 -1.850 -1.850	-	-1.650 -1.650 -1.650 -1.650	-1.825 -1.825 -1.825 -1.825	-1.615 -1.615 -1.615 -1.615	Vdc 	- - 12 13	1 8	0 -		8	1,16
Logic ''1'' Threshold Voltage	Vона	9 9 15 15	-1.080 -1.080 -1.080 -1.080	-	-0.980 -0.980 -0.980 -0.980	1		-0.910 -0.910 -0.910 -0.910		Vdc			12 13 -	- 12 13	8	1,16
Logic "ð" Threshold Voltage	VOLA	9 9 15 15		-1.655 -1.655 -1.655 -1.655		-	-1.630 -1.630 -1.630 -1.630	-	-1.595 -1.595 -1.595 -1.595	Vdc 		1 1 1	- - 12 13	12 13 - -	8	1,16
Switching Times (50-ohm load)		1 1	1		-		Ř					2.0	Pulse In	Pulse Out	-3.2 V	+2.0
Propagation Delay	t12+15- t12-15+ t12+9+ t12-9-	15 15 9 9	1.0	3.1	1.0	2.0	2.9	1.0	3.3	ns	-		12	15 15 9 9	8	1,10
Rise Time (20 to 80%) Fall Time (20 to 80%)	t15+ t9+ t15- t9-	15 9 15 9	11	3.6	1.1		3.3	1.1	3.7		-	-		15 9 15 9		



MC10103

QUAD 2-INPUT OR GATE

The MC10103 is a quad 2-input OR gate. The MC10103 provides one gate with OR/NOR outputs.

 $P_D = 25 \text{ mW typ/gate (No Load)}$

 $t_{pd} = 2.0 \text{ ns typ}$

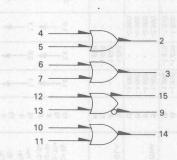
 t_r , $t_f = 2.0 \text{ ns typ } (20\%-80\%)$

MECL 10K SERIES

QUAD 2-INPUT OR GATE

P SUFFIX PLASTIC PACKAGE CASE 648 LSUFFIX CERAMIC PACKAGE CASE 620

LOGIC DIAGRAM



V_{CC1} = Pin 1 V_{CC2} = Pin 16 V_{EE} = Pin 8

PIN ASSIGNMENT



3-10

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to $-2.0\ volts$. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in the same manner.

					121
		TEST V	OLTAGE	VALUES	255
		11	(Volts)	100	36
@ Test Temperature	V _{IHmax}	VILmin	VIHAmin	VILAmax	VEE
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

		MC10103 Test Limits									TEST VOLTAGE APPLIED TO PINS LISTED BELOW:					
		Pin Under	-30	o°c		+25°C	ADILIA.	+8	5°C							(Vcc)
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	VIHmax	VILmin	VIHAmin	VILAmax	VEE	Gnd
Power Supply Drain Current	1 _E	8		29	- 1	21	26	-	29	mAdc	-	A SHALL		10-	8	1,16
Input Current	linH	4*		390	-	-	245	-	245	μAdc	4.	-	-	25-	8	1,16
	linL	4.	0.5	-	0.5	-	-	0.3	-	μAdc	-	4.		g-	8	1,16
Logic "1" Output Voltage	Voн	2 9	-1.060 -1.060	-0.890 -0.890	-0.960 -0.960	-	-0.810 -0.810	-0.890 -0.890	-0.700 -0.700	Vdc Vdc	4,5	_	-	6.25	8	1,16 1,16
Logic "0" Output Voltage	VOL	2 9	-1.890 -1.890	-1.675 -1.675	-1.850 -1.850		-1.650 -1.650	-1.825 -1.825	-1.615 -1.615	Vdc Vdc	12,13	-	- '	4	8	1,16 1,16
Logic "1" Threshold Voltage	VOHA	2 9	-1.080 -1.080		-0.980 -0.980	-		-0.910 -0.910	-	Vdc Vdc	-	1 I	4,5	12,13	8	1,16 1,16
Logic "0" Threshold Voltage	VOLA	2 9	\	-1.655 -1.655	-		-1.630 -1.630	-	-1.595 -1.595	Vdc Vdc		8 - 1 8 - 1	12,13	4,5	8	1,16 1,16
Switching Times (50-ohm load)				1		No.						7 82	Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t ₄₊₂₊ t ₁₂₊₉ .	2 9	1.0	3.1	1.0	2.0	2.9	1.0	3.3 3.3	ns		200	12	9	8	1,16
Rise Time (20% to 80%)	t ₂₊	2	1.1	3.6	1.1	8	3.3	1.1	3.7			1 7	4	2		
Fall Time (20% to 80%)	t ₂₋	2	1.1	3.6	1.1	V	3.3	1.1	3.7	1	=		4	2	V	1

^{*}Individually test each input applying V_{IH} or V_{IL} to input under test.

QUAD 2-INPUT AND GATE

The MC10104 is a quad 2-input AND gate. One of the gates has both AND/NAND outputs available.

P_D = 35 mW typ/gate (No Load)

 $t_{pd} = 2.7 \text{ ns typ}$

 t_r , $t_f = 2.0 \text{ ns typ } (20\%-80\%)$

MECL 10K SERIES

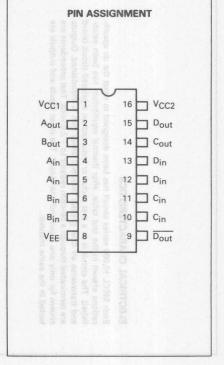
QUAD 2-INPUT AND GATE

P SUFFIX PLASTIC PACKAGE CASE 648

CASE 620



4 LOGIC DIAGRAM V_{CC1} = Pin 1 V_{CC2} = Pin 16 V_{EE} = Pin 8



Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

		TEST V	OLTAGE VA	LUES	
	100		Volts	42	
@ Test Temperature	VIH max	VIL min	VIHA min	VILA max	VEE
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

						MC1010	4 Test L	imits			TEST VO	I TAGE APP	LIED TO PIN	S LISTED BL	FOW.	
			-30	o°C		+25°C		+85	5°C		1231 00	LIAGE AFF	LIED TO THE	S EISTED DE		(VCC)
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	VIH max	VIL min	VIHA min	VILA max	VEE	Gnd
Power Supply Drain Current	1E	8		39			35	114	39	mAdc			-		8	1,16
Input Current	linH*	12 13	Ī	425 350	-	_	265 220	_	265 220	μAdc μAdc	12,13 13	-	= =	-	8	1,16 1,16
	linL	12	0.5	-	0.5	-	-	0.3	-	μAdc	-	12			8	1,16
Logic "1" Output Voltage	Voн	15 9	-1.060 -1.060	-0.890 -0.890	-0.960 -0.960	_	-0.810 -0.810	-0.890 -0.890	-0.700 -0.700	Vdc Vdc	12,13	-	_	-	8	1,16 1,16
Logic "0" Output Voltage	VOL	15 9	-1.890 -1.890	-1.675 -1.675	-1.850 -1.850	-	-1.650 -1.650	-1.825 -1.825	-1.615 -1.615	Vdc Vdc	12,13	-	-		8	1,16 1,16
Logic "1" Threshold Voltage	VOHA	9 9 15 15	-1.090 -1.090 -1.090 -1.090	-	-0.980 -0.980 -0.980 -0.980		1	-0.910 -0.910 -0.910 -0.910	-	Vdc	 12 13	-	- - 13 - 12	12 13	8	1,16
Lgoic "0" Threshold Voltage	VOLA	9 9 15 15		-1.655 -1.655 -1.655 -1.655		=	-1.630 -1.630 -1.630 -1.630		-1.595 -1.595 -1.595 -1.595	Vdc	12 13 - -	1081	13 12 -	12 13	8	1,16
Switching Times* (50-ohm load)	1	3-4	14	10			8				+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0
Propagation Delay	t12+15+ t12-15- t12+9- t12-9+ t13+15+ t13+9-	15 15 9 9 15	1.0	4.3	1.0	2.2	4.0	1.0	4.2	ns	13 V 12 12	d to Utalgo	12 V 13 13	15 15 9 9	8	1,16
Rise Time (20 to 80%)	t ₁₅₊	15 9	1.5	3.7 †	1.5	2.0	3.5	1.5	3.6			E E	8	15 9		
Fall Time (20 to 80%)	t ₁₅₋	15 9	1		+	1	1	1		+	1	1 4	3	15 9	+	+

^{*}Inputs 4, 7, 10, and 13 will behave similarly for ac and l_{inH} values. Inputs 5, 6, 11, and 12 will behave similarly for ac and l_{inH} values.



MC10105

TRIPLE 2-3-2-INPUT OR/NOR GATE

The MC10105 is a triple 2-3-2 input OR/NOR gate.

P_D = 30 mW typ/gate (No Load)

 $t_{pd} = 2.0 \text{ ns typ}$

 t_r , $t_f = 2.0$ ns typ (20%–80%)

MECL 10K SERIES

TRIPLE 2-3-2-INPUT OR/NOR GATE

L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

LOGIC DIAGRAM

4 3 2 9 66 10 7 7 7 11 13 14 12 15

 $\begin{array}{lll} V_{CC1} &=& Pin \ 1 \\ V_{CC2} &=& Pin \ 16 \\ V_{EE} &=& Pin \ 8 \end{array}$

PIN ASSIGNMENT

16 VCC2 VCC1 Aout 2 15 Cout 14 Cout Aout 3 Ain 4 13 Cin Ain 5 12 Cin 11 🔲 Bin Bout 6 10 Bin Bout 7 9 Bin VEE 2 8

3-14

3

8 J E	Mil Colts	TEST	VOLTAGE VAL	UES	1 833
112-3			(Volts)		9
@ Test Temperature	V _{IH max}	VIL min	VIHA min	VILA max	VEE
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

								777		+85°C	-0.700	-1.825	-1.035	-1.440	-5.2	
		Pin		3. V.	٨	AC 10105	Test Li	mits			TEST	VOLTAGE A	PPLIED TO PINS	LISTED BELO	N:	
	19 7 8 Y	Under	-30	оС		+25°C		+85	5°C	-	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	TOE THOU A	12120 1011110	T		(VCC)
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	VIH max	VIL min	VIHA min	VILA max	VEE	Gnd
Power Supply Drain Current	1E	8	-	23	-	17	21	- 1	23	mAdc	-	-			8	1,16
Input Current	linH	4		425	-		265	-	265	μAdc	4		N	-	8	1,16
	linL	4	0.5	-	0.5	-	-	0.3	-	μAdc		4	-		8	1,16
Logic "1" Output Voltage	Vон	3 2	-1.060 -1.060	-0.890 -0.890	-0.960 -0.960	-	-0.810 -0.810	-0.890 -0.890	-0.700 -0.700	Vdc Vdc	4	Ī	=	_	8	1,16 1,16
Logic "0" Output Voltage	VOL	3 2	-1.890 -1.890		-1.850 -1.850	-	-1.650 -1.650	-1.825 -1.825	-1.615 -1.615	Vdc Vdc	4			. NE	8	1,16
Logic "1" Threshold Voltage	Vона	3 2	-1.080 -1.080	102	-0.980 -0.980		-	-0.910 -0.910	-	Vdc Vdc		_	4	4 -	8	1,16 1,16
Logic "0" Threshold Voltage	VOLA	3 2		-1.655 -1.655	-	-	-1.630 -1.630	İ	-1.595 -1.595	Vdc Vdc		-87	4	- 4	8	1,16 1,16
Switching Times (50-ohm load)				8								1 8	Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t4+3- t4-3+ t4+2+ t4-2-	3 3 2 2	1.0	3.1	1.0	2.0	2,9	1.0	3.3	ns	-	100 100 100 100 100 100 100 100 100 100	4	3 3 2 2	8	1,16
Rise Time (20 to 80%) Fall Time (20 to 80%)	t ₃₊ t ₂₊ t ₃₋ t ₂₋	3 2 3 2	11	3.6	11	-	3.3	1.1	3.7			-8 1 -8 1	30 CUM	3 2 3 2		

TRIPLE 4-3-3-INPUT NOR GATE

The MC10106 is a triple 4-3-3 input NOR gate.

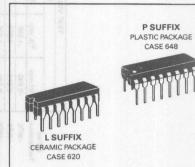
P_D = 30 mW typ/gate (No Load)

 $t_{pd} = 2.0 \text{ ns typ}$

 t_r , $t_f = 2.0$ ns typ (20%–80%)

MECL 10K SERIES

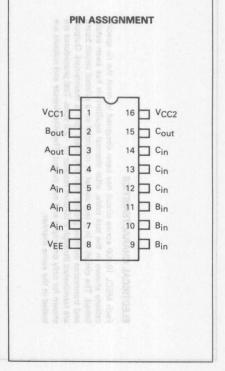
TRIPLE 4-3-3-INPUT NOR GATE



LOGIC DIAGRAM

4
5
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10
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13
14

VCC1 = Pin 1
VCC2 = Pin 16
VEE = Pin 8



		TEST \	OLTAGE VALL	JES	59
@ Test	923		(Volts)	AN 155	
Temperature	VIH max	VIL min	VIHA min	VILA max	VEE
-30°C	-0.890	-1.890	-1,205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

										+85°C	-0.700	-1.825	-1.035	-1.440	-5.2	
	10000	Pin			٨	/C1010	6 Test Li	imits			TEST	VOLTAGE A	PPLIED TO PIN	S LISTED BEL	ow:	
		Under	-3	0°C		+25°C		+85	5°C							(Vcc)
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	VIH max	V _{IL} min	VIHA min	VILA max	VEE	Gnd
Power Supply Drain Current	1E	8	-	23	-	17	21	-	23	mAdc	-	-	-		8	1,16
Input Current	linH	4	-	425	-	-	265	-	265	μAdc	4	-	-	E	8	1,16
	linL	4	0.5	-	0.5	-	-	0.3	-	μAdc		4		=	8	1,16
Logic "1" Output Voltage	Voн	3 2	-1.060 -1.060	-0.890 -0.890	-0.960 -0.960	-	-0.810 -0.810	-0.890 -0.890	-0.700 -0.700	Vdc	Ξ	1	_		8	1,16 1,16
Logic "0" Output Voltage	VOL	3 2	-1.890 -1.890		-1.850 -1.850	-	-1.650 -1.650	-1.825 -1.825	-1.615 -1.615	Vdc	4 9	= =	e -	1 - 2	8 8	1,16 1,16
Logic "1" Threshold Voltage	Vона	3 2	-1.080 -1.080		-0.980 -0.980	-	-	-0.910 -0.910		Vdc	=		2 -	4 9	8	1,16 1,16
Logic ''0'' Threshold Voltage	VOLA	3 2	-	-1.655 -1.655	-	-	-1.630 -1.630	-11	-1.595 -1.595	Vdc	===	- 28	4 9	- 13 - 12 - 12	8	1,16 1,16
Switching Times (50-ohm load)	++		173	1			N.C.					2008	Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t4+3-	3	1.0	3.1	1.0	2.0	2.9	1.0	3.3	ns	-	-3 4	4	3	8	1,16
9성성	t4-3+		1.0	3.1	1.0		2.9	1.0	3.3		- V	3.4		9 2		
Rise Time (20 to 80%)	t3+		1.1	3.6	1.1		3.3	1.1	3.7			-9 1	Viro.	8 6		
Fall Time (20 to 80%)	t3_		1.1	3.6	1.1	*	3.3	1.1	3.7	*	-	40.0	7	3.5	*	*



MC10107

TRIPLE 2-INPUT EXCLUSIVE "OR"/EXCLUSIVE "NOR"

The MC10107 is a triple-2 input exclusive OR/NOR gate.

P_D = 40 mW typ/gate (No Load)

 $t_{pd} = 2.8 \text{ ns typ}$

3

 t_r , $t_f = 2.5 \text{ ns typ } (20\%-80\%)$

MECL 10K SERIES

TRIPLE 2-INPUT EXCLUSIVE "OR"/EXCLUSIVE "NOR"

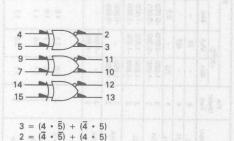
P.S.
PLASTIC
CA

L SUFFIX
CFRAMIC PACKAGE

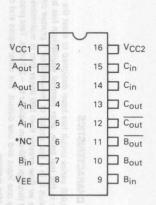
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

LOGIC DIAGRAM



V_{CC1} = Pin 1 V_{CC2} = Pin 16 V_{EE} = Pin 8 PIN ASSIGNMENT



*NC = No Connection

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

	7.3110.4	TEST	VOLTAGE VAL	UES	
			(Volts)		
@ Test Temperature	V _{IH} max	VIL min	VIHA min	VILA max	VEE
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

the territory of the same of t		and the same of the same								+85-C	-0.700	-1.825	-1.035	-1,440	-5.2	No Line
		Pin			٨	VIC101	07 Test				TECT	VOLTAGE A	DELLED TO BIN	S LISTED BELOW	7	1
		Under	-30	0°C		+250	C	+8	5°C		1 E S 1	VOLTAGE A	PLIED TO FIN	S LISTED BELOW		(Vcc)
Characteristic	Symbol	Test	Min	Max	Mir	n	Max	Min	Max	Unit	VIH max	VIL min	VIHA min	VILA max	VEE	Gnd
Power Supply Drain Current	IE .	8		31	-		28	1 -	31	mAdc	5,7,15	-	-	-	8	1,16
Input Current	lin H	4,9,14 5,7,15		425 350	=		265 220	1	265 220	μAdc μAdc	:	=	5		8	1,16 1,16
	lin L		0.5	-	0.5		-	0.3	-	μAdc	-		-	-	8	1,16
Logic "1" Output Voltage	Voн	2 2 3 3	-1.060 -1.060 -1.060 -1.060	-0.890 -0.890 -0.890 -0.890	-0.96 -0.96 -0.96	50	-0.810 -0.810 -0.810 -0.810	-0.890 -0.890 -0.890 -0.890	-0.700 -0.700 -0.700 -0.700	Vdc	4,5 - 4 5	=	Ē		8	1,16
Logic "0" Output Voltage	VOL	2 2 3 3	-1.890 -1.890 -1.890 -1.890	-1.675 -1.675 -1.675 -1.675	-1.85 -1.85 -1.85	50 50 50	-1.650 -1.650 -1.650 -1.650	-1.825 -1.825 -1.825 -1.825	-1.615 -1.615 -1.615 -1.615	Vdc	4 5 4,5	-	9 -	16	8	1,16
Logic "1" Threshold Voltage	Vона	2 2 3 3	-1.080 -1.080 -1.080 -1.080	-	-0.98 -0.98 -0.98	30	-	-0.910 -0.910 -0.910 -0.910	=	Vdc	5 - - -	3 <u>-</u>	4 - 4 5	- 4 -	8	1,16
Logic "0" Threshold Voltage	VOLA	2 2 3 3	P-0-1	-1.655 -1.655 -1.655 -1.655		- 8	-1.630 -1.630 -1.630 -1.630	-	-1.595 -1.595 -1.595 -1.595	Vdc	- - 5 -	-	4 5 4	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	8	1,16
Switching Times (50 Ω Load)	100	1000	1 2 2		Min	Тур	Max	MINISTER STATE		Unit	+1.1 V	25 40	Pulse In	Pulse Out	-3.2 V	+2.0 \
Propagation Delay	t++ t+- t-+ t	Inputs 4, 9 or 14 to either Output	1.1	3.8	1.1	2.0	3.7	1.1	4.0	ns	5,7,15	1 % - 8 · 1	Input 4, 9, or 14	Corresponding Ex-OR/Ex-NOR Outputs	8	1,16
	t++ t+- t-+ t	5,7, or 15 to either Output				2.8					4,9,14	=	5, 7, or 15	Corresponding Ex-OR/Ex-NOR Outputs		
Rise Time (20 to 80%)	t+		1.1	3.5		2.5	3.5		3.8		4,9,14	4.5	Any Input	Corresponding Ex-OR/Ex NOR		
Fall Time (20 to 80%)	t-		1.1	3.5	*	2.5	3.5		3.8	*	4,9,14	-	Any Input	Outputs	*	*

^{*}Individually test each input applying V_{IH} or V_{IL} to input under test. **Any Output

3

MECL 10K SERIES

DUAL 4-5-INPUT "OR/NOR" GATE

DUAL 4-5-INPUT "OR/NOR" GATE

The MC10109 is a dual 4-5 input OR/NOR gate.

PD = 30 mW typ/gate (No Load)

 $t_{pd} = 2.0 \text{ ns typ}$

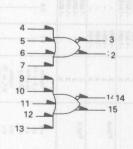
 t_r , $t_f = 2.0$ ns typ (20%–80%)

CERAMIC PACKAGE CASE 620

P SUFFIX PLASTIC PACKAGE CASE 648

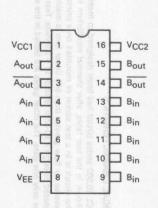


LOGIC DIAGRAM



V_{CC1} = Pin 1 V_{CC2} = Pin 16 V_{EE} = Pin 8

PIN ASSIGNMENT



3-20

2 2 5		TEST	VOLTAGE VAL	UES	
U.S. L.	34123		(Volts)	len len	8
@ Test Temperature	VIH max	V _{IL min}	VIHA min	VILA max	VEE
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

										+85°C	-0.700	-1.825	-1.035	-1,440	-5.2	-
		Pin				VC 1010	9 Test L	imits			1	EST VOLTAG	E APPLIED TO	PINS BELOW:		
	No. 1	Under	-30	o°C		+25°C		+8	5°C						-	(VCC)
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	VIH max	VIL min	VIHA min	VILA max	VEE	Gnd
Power Supply Drain Current	1E	8	-	15	-	11	14	-	15	mAdc		- 0	9 -6 5		8	1,16
Input Current	linH	4		425	-	-	265	-	265	μAdc	4	-91	-88		8	1,16
	linL	4	0.5	-	0.5	-	-	0.3		μAdc		4	1 - 1 3		8	1,16
High Output Voltage	Vон	2 3	-1.060 -1.060		-0.960 -0.960		-0.810 -0.810	-0.890 -0.890	-0.700 -0.700	Vdc Vdc	4	2.3	17 78 8		8 8	1,16 1,16
Low Output Voltage	VOL	2 3	-1.890 -1.890		-1.850 -1.850		-1.650 -1.650	-1.825 -1.825	-1.615 -1.615	Vdc Vdc	- 4	- 9	3 -28	= =	8	1,16 1,16
High Threshold Voltage	VOHA	2 3	-1.080 -1.080		-0.980 -0.980	_	-	-0.910 -0.910	-	Vdc Vdc	E-W	- 1	4	4	8	1,16 1,16
Low Threshold Voltage	VOLA	2 3	1	-1.655 -1.655	-		-1.630 -1.630	1	-1.595 -1.595	Vdc Vdc	8 4-5	3 8	4 4 8	4 -	8 8	1,16 1,16
Switching Times (50-ohm load)							55			,	T S E	80 8	Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t4+2+ t4-2- t4+3- t4-3+	2 2 3 3	1.0	3.7	1.0	2.0	2.9	1.0	3.7	ns	Ab Garage	Se Aboli	4	2 2 3 3	8	1,16
Rise Time (20 to 80%)	t ₂₊ t ₃₊	2 3	1.1	4.0	1.1		3.3	1.1	1.0		5 518	1 2 2	量 星星	2 3		
Fall Time (20 to 80%)	t ₂₋	2 3	1	200		+	1		1	4	L L-R	- 53		2 3	*	*

3

MC10110

DUAL 3-INPUT 3-OUTPUT "OR" GATE

The MC10110 is designed to drive up to three transmission lines simultaneously. The multiple outputs of this device also allow the wire "OR" ing of several levels of gating for minimization of gate and package count.

The ability to control three parallel lines from a single point makes the MC10110 particularly useful in clock distribution applications where minimum clock skew is desired. Three $V_{\mbox{CC}}$ pins are provided and each one should be used.

P_D = 80 mW typ/gate (No Load)

t_{pd} = 2.4 ns typ (All Outputs Loaded)

 t_r , $t_f = 2.2 \text{ ns typ } (20\%-80\%)$

MECL 10K SERIES

DUAL 3-INPUT 3-OUTPUT "OR" GATE

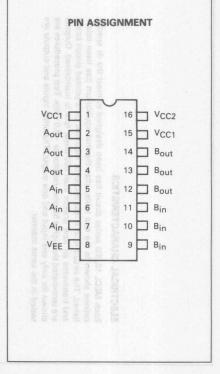
P SUFFIX
PLASTIC PACKAGE
CASE 648



L SUFFIX CERAMIC PACKAGE CASE 620



Section 2 2 2 3 4 4 4 9 9 10 12 12 12 13 14 14 14 15 VCC1 = Pin 1, 15 VCC2 = Pin 16 VEE = Pin 8



		TEST \	OLTAGE VA	LUES	
			(Volts)	7 59	
@ Test Temperature	VIH max	VIL min	VIHA min	VILA max	VEE
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

		-								.00 0	0.700	1.020	1.000	1.440	0.2	
		Pin			N	AC10110	Test Lim	its			TECT	OL TACE AD	DI IED TO DIA	S LISTED BEL	OW.	
		Under	-30	o°C		+25°C		+8	5°C	-	I IEST VI	JL TAGE AF	PLIED TO PIN	45 LISTED BEL	.Ovv.	(VCC
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	VIH max	VIL min	VIHA min	VILA max	VEE	Gnd
Power Supply Drain Current	1 _E	8	-	42	-	30	38	1 - 7	42	mAdc	-	-	_	-	8	1,15,1
Input Current	linH	5,6,7	-	680	-	-	425	-	425	μAdc		-	-	-	8	1,15,1
	linL	5,6,7	0.5	-	0.5	-	- 1-11	0.3	-	μAdc	-	3.0	- 63	-	8	1,15,1
Logic "1" Output Voltage	VOH	2 3 4	-1.060 -1.060 -1.060	-0.890 -0.890 -0.890	-0.960 -0.960 -0.960	-	-0.810 -0.810 -0.810	-0.890 -0.890 -0.890	-0.700 -0.700 -0.700	Vdc Vdc Vdc	5 6 7	8-8 g	12 8		8 8 8	1,15, 1,15, 1,15,
Logic ''0'' Output Voltage	VOL	2 3 4	-1.890 -1.890 -1.890	-1.675 -1.675 -1.675	-1.850 -1.850 -1.850	-	-1.650 -1.650 -1.650	-1.825 -1.825 -1.825	-1.615 -1.615 -1.615	Vdc Vdc Vdc	=	8-5 8	4 8 1	=	8 8 8	1,15,1 1,15,1 1,15,1
Logic ''1'' Threshold Voltage	Vона	2 3 4	-1.080 -1.080 -1.080	-	-0.980 -0.980 -0.980	=	_	-0.910 -0.910 -0.910	=	Vdc Vdc Vdc	9	\$ <u>-</u> 8	5 6 7	- 12	8 8 8	1,15,1 1,15,1 1,15,1
Logic "0" Threshold Voltage	VOLA	2 3 4		-1.655 -1.655 -1.655	<u>-</u>	-	-1.630 -1.630 -1.630		-1.595 -1.595 -1.595	Vdc Vdc Vdc	2 -	0 0 0	54	5 6 7	8 8 8	1,15,1 1,15,1 1,15,1
Switching Times (50-ohm load)		表走了								10	2	1573	Pulse In	Pulse Out	-3.2 V	+2.0
Propagation Delay	t5+2+ t5-2- t5+3+ t5-3- t5+4+ t5-4-	2 2 3 3 4 4	1.4	3.5	1.4	2.4	3.5	1.5	3.8	ns	1 1 1 1 1 1 1		5	2 2 3 3 4 4	8	1,15,1
Rise Time (20 to 80%)	t ₂₊ t ₃₊ t ₄₊	2 3 4	1.0		1.1	2.2		1.2		10/10	66 - 1 -		d form	2 3 4		
Fall Time (20 to 80%)	t2- t3- t4-	2 3 4						1		1	2 ₂ =		104 BILL	2 3 4	1	

^{*}Individually test each input using the pin connections shown.

DUAL 3-INPUT 3-OUTPUT "NOR" GATE

The MC10111 is designed to drive up to three transmission lines simultaneously. The multiple outputs of this device also allow the wire "OR"-ing of several levels of gating for minimization of gate and package count.

The ability to control three parallel lines from a single point makes the MC10111 particularly useful in clock distribution applications where minimum clock skew is desired. Three V_{CC} pins are provided and each one should be used.

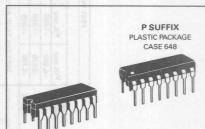
P_D = 80 mW typ/gate (No Load)

tpd = 2.4 ns typ (All Outputs Loaded)

 t_r , $t_f = 2.2 \text{ ns typ } (20\%-80\%)$

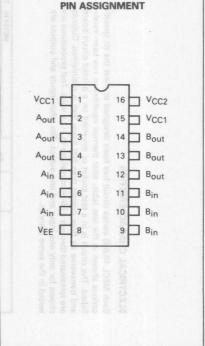
MECL 10K SERIES

DUAL 3-INPUT 3-OUTPUT "NOR" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 620

LOGIC DIAGRAM 2 3 6 7 12 9 13 14 VCC1 = Pin 1, 15 VCC2 = Pin 16 VEE = Pin 8



Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to $-2.0 \ \text{volts}$. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in the same manner.

		TEST \	OLTAGE VA	LUES	
			(Volts)		
@ Test Temperature	VIH max	VIL min	VIHA min	VILA max	VEE
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

							and the second			+85°C	-0.700	-1.825	-1.035	-1.440	-5.2	E COLUMN
		Pin			N	AC10111	Test Lin	its			TECT V	OL TACE AD	DI JED TO BIA	IS LISTED BEI	OW.	
		Under	-30	o°C		+25°C		+85	°C		I IEST VI	DL TAGE AP	PLIED TO PIN	IS LISTED BEI	.Ovv.	(VCC
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	VIH max	VIL min	VIHA min	VILA max	VEE	Gnd
Power Supply Drain Current	1E	8	-	42	-	-	38	-	42	mAdc	-		-2 %	B	8	1,15,
Input Current	linH	5,6,7	-	680	-	-	425	-	425	μAdc		-	-7 19	B -	8	1,15,
	linL	5,6,7	0.5	-	0.5	-	-	0.3	-	μAdc	-		- 4	B 1	8	1,15,
Logic "1" Output Voltage	Voн	2 3 4	-1.060 -1.060 -1.060	-0.890 -0.890 -0.890	-0.960 -0.960 -0.960	-	-0.810 -0.810 -0.810	-0.890 -0.890 -0.890	-0.700 -0.700 -0.700	Vdc Vdc Vdc	=	Ē	구를	-	8 8 8	1,15, 1,15, 1,15,
Logic "0" Output Voltage	VOL	2 3 4	-1.890 -1.890 -1.890	-1.675 -1.675 -1.675	-1.850 -1.850 -1.850	-	-1.650 -1.650 -1.650	-1.825 -1.825 -1.825	-1.615 -1.615 -1.615	Vdc Vdc Vdc	5 6 7		78.0		8 8 8	1,15, 1,15, 1,15,
Logic "1" Threshold Voltage	VOHA	2 3 4	-1.080 -1.080 -1.080		-0.980 -0.980 -0.980	-	=	-0.910 -0.910 -0.910		Vdc Vdc Vdc	- 08	98.5	- 1-65 A	5 6 7	8 8 8	1,15, 1,15, 1,15,
Logic "0" Threshold Voltage	VOLA	2 3 4	-	-1.655 -1.655 -1.655	-	=	-1.630 -1.630 -1.630	=	-1.595 -1.595 -1.595	Vdc Vdc Vdc	-0		5 6 7	8 - 8	8 8 8	1,15, 1,15, 1,15,
Switching Times (50-ohm load)	2						5				13	100	Pulse In	Pulse Out	-3.2 V	+2.0
Propagation Delay	t5+2- t5-2+ t5+3- t5-3+ t5+4- t5-4+	2 2 3 3 4 4	1.4	3.5	1.4	2.4	3.5	1,5	3.8	ns	20 65 1	TIPS SEE THE	5	2 2 3 3 4 4	8	1,15,
Rise Time (20 to 80%)	t ₂₊ t ₃₊ t ₄₊	2 3 4	1.0	The same	1.1	2.2	3.5	1.2	3.8		= #	i t	Trop to	2 3 4		
Fall Time (20 to 80%)	t2- t3- t4-	2 3 4	1 2	-	•		•				-74	-	uor la	2 3 4		

^{*}Individually test each input using the pin connections shown.

3

QUAD EXCLUSIVE OR GATE

The MC10113 is a quad Exclusive OR gate, with an enable common to all four gates. The outputs may be wire-ORed together to perform a 4-bit comparison function (A=B). The enable is active low.

P_D = 175 mW typ/pkg (No Load)

 $t_{pd} = 2.5 \text{ ns typ}$

 t_r , $t_f = 2.0$ ns typ (20% to 80%)

MECL 10K SERIES

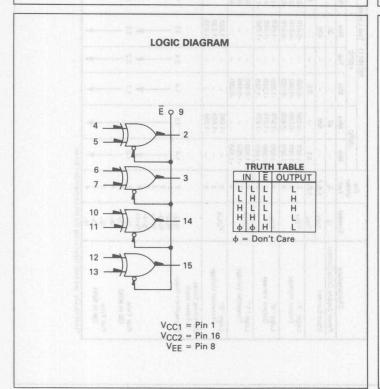
QUAD EXCLUSIVE OR GATE

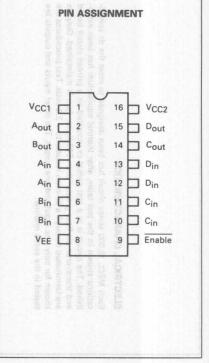


CASE 620

P SUFFIX PLASTIC PACKAGE CASE 648







@ Test		TEST V	OLTAGE VAL	UES	
Temperature	VIH max	V _{IL} min	VIHA min	VILA max	VEE
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

										+85°C	-0.700	-1.825	-1.035	-1.440	-5.2	
		D:-		Fall III	MC1	0113	Test I	Limits		00000	TEST VO	L TACE ADD	LIED TO BIN	S LISTED BEI	OW:	
		Pin Under	-30	o°C	+	25°C		+85	o°C		TEST VO	LIAGE APP	LIED TO PIN	S LISTED BEI	LOW.	(Vcc)
Characteristic	Symbol	Test	Min	Max	Min	M	lax	Min	Max	Unit	VIH max	V _{IL} min	VIHA min	VILA max	VEE	Gnd
Power Supply Drain Current	1E	8	-	46	-	4	12	1 +	46	mAdc	-		- 1		8	1,16
Input Current	lin H	4,7,10,13	-	425	-	2	65	114	265	μAdc			-	-	8	1,16
		5,6,11,12	-	350	-	2	20		220	μAdc				-	8	1,16
		9	-	870	-	5	45		545	μAdc	9	5	E - E -	9 = 1	8	1,16
	lin L	*	0.5	-	0.5		-	0.3	-	μAdc		100	- 10 0	W 7	8	1,16
Logic "1"	VOH	2	-1.060	-0.890	-0.960	-0.	810	-0.890	-0.700	Vdc	4	-51	2 - 2	7 - 7	8	1,16
Output Voltage		3	-1.060	-0.890	-0.960	-0.	810	-0.890	-0.700		7	-9 3	S - 10 T		8	8 3
		14	-1.060	-0.890	-0.960	-0.	810	-0.890	-0.700	1845	11		3 -0 5	8 2 5 1		2 1 3
		15	-1.060	-0.890	-0.960	0 -0.	810	-0.890	-0.700		13	-9 8	H'A		1	- 1
Logic "0"	VOL	2	-1.890	-1.675	-1.850) -1.	650	-1.825	-1.615	Vdc		4	- 60		8	1,16
Output Voltage		3	-1.890	-1.675	-1.850	-1.	650	-1.825	-1.615	1 12	- E	7	4 - 2 3	5 4 5		OH 4
		14	-1.890	-1.675	-1.850	-1.	650	-1.825	-1.615			11	F	5 - 5	200	0 1
		15	-1.890	-1.675	-1.850	-1.	650	-1.825	-1.615	V	P -	13	B - H :		V	2 1 3
Logic "1"	VOHA	2	-1.080	-	-0.980		-	-0.910	_	Vdc	9 -	-0.45	4	E 2 1	8	1,16
Threshold Voltage		3	-1.080		-0.980)		-0.910	-	4	dr-	-20	6	문 등 유	1 3 3	20 11 9
		14	-1.080	- 0	-0.980)	-	-0.910	-	8 9	6 -	-12-5	10	8 月玉	0 2	
		15	-1.080		-0.980)		-0.910	-	- 6	10 A	4	12	= =	V	- 1
Logic "0"	VOLA	2	1	-1.655		-1.	630		-1.595	Vdc	3 -3	-5 3	- 2	5	8	1,16
Threshold Voltage		3	and -	-1.655	-	-1.	630	14	-1.595	1	华曼	-2-5	F - 6 4	7	105	2.4
		14	-	-1.655	-	73004	630	-	-1.595		9 -5	-5.6	6 -33	5 11	1 3	
		15	-	-1.655	-	-1.	630	4	-1.595	14	7 -2	-13-5	8 - 1	13	V	3 -
Switching Times (50 Ω Load)					Min	Тур	Max			Unit	+1.11 V	5.6	Pulse In	Pulse Out	-3.2 V	+2.0 \
Propagation Delay	t4+2+	2	1.1	4.7	1.3	2.6	4.5	1.3	5.0	ns	7 -3	-8.9	4	2	8	1,16
	t4-2-	2	1.1	4.7	1.3	2.6	4.5	1.3	5.0	19 19	H2 _2m	-29	4		3 8	F 9
	t9+2-	2	1.3	5.2	1.5	3.4	5.0	1.5	5.5	B 1	4	-35 8	9	2 0	1 5	
	t9-2+	2	1.3	5.2	1.5	3.4	5.0	1.5	5.5	100	4	-9-13	9	19 . 2		5 9
Rise Time (20 to 80%)	t ₂₊	2	1.1	4.2	1.1	2.5	3.9	1.1	4.4	4	4.5	-5 E	4	8 8	etua etua	870
Fall Time (20 to 80%)	t ₂₋	2	1.1	4.2	1.1	2.5	3.9	1.1	4.4	*	-	3 5 2	4	10 10 10		5.0

^{*}Individually test each input applying VIH or VIL to input under test.

TRIPLE LINE RECEIVER

The MC10114 is a triple line receiver designed for use in sensing differential signals over long lines. An active current source and translated emitter follower inputs provide the line receiver with a common mode noise rejection limit of one volt in either the positive or the negative direction. This allows a large amount of common mode noise immunity for extra long lines.

Another feature of the MC10114 is that the OR outputs go to a logic low level whenever the inputs are left floating. The outputs are each capable of driving 50 ohm transmission lines.

This device is useful in high speed central processors, minicomputers, peripheral controllers, digital communication systems, testing and instrumentation systems. The MC10114 can also be used for MOS to MECL interfacing and it is ideal as a sense amplifier for MOS RAM's.

A VBB reference is provided which is useful in making the MC10114 a Schmitt trigger, allowing single-ended driving of the inputs, or other applications where a stable reference voltage is necessary.

 $P_D = 145 \text{ mW typ/pkg}$

t_{nd} = 2.4 ns typ (Single Ended Input)

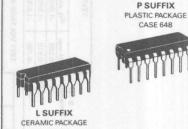
t_{pd} = 2.0 ns typ (Differential Input)

 t_r , $t_f = 2.1$ ns typ (20% to 80%)

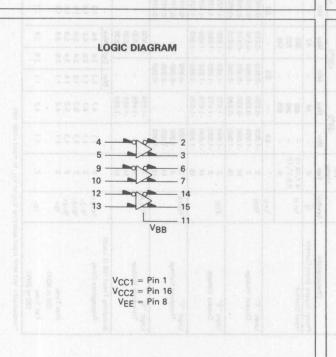
MC10114

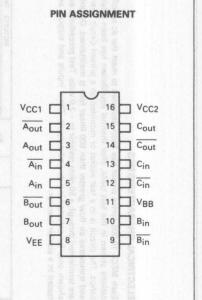
MECL 10K SERIES

TRIPLE LINE RECEIVER









Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

	13	TEST VOLTAGE VALUES														
	(Volts)															
@ Test Temperature	VIH max	VIL min	VIHA min	VILA max	VBB	VIHH*	VILH*	VIHL*	VILL.	VEE						
-30°C	-0.890	-1.890	-1.205	-1.500	From	+0.110	-0.890	-1.890	-2.890	-5.2						
+25°C	-0.810	-1.850	⊿1.105	-1.475	Pin	+0.190	-0.850	-1.810	-2.850	-5.2						
+85°C	-0.700	-1.825	-1.035	-1.440	- 11	+0.300	-0.825	-1.700	-2.825	-5.2						

The second secon										+00 C	-0.700	-1,020	-1.035	-1.440	1.1	+0.300	-0.020	-1.700	-2.020	-0.2	1
			Pin	MC10114 Test Limits								TEST VOLTAGE APPLIED TO PINS BELOW:									
Characteristic	Symbol	Under	Min	0°C Max	Min	+25°C	Max	+8! Min	5°C Max	Unit	VIH max	VIL min	V _{IHA} min	VILA max	VBB	VIHH*	VILH*	VIHL*	VILL.	VEE	(VCC
Power Supply Drain Current	1 _E	8	-	39	-	28	35	-	39	mAdc	-	4,9,12	-	-9	5,10,13	-//	9 20	-	-	8	1,16
Input Current	linH	4	-	70	-	-	45	-	45	μAdc	4	9,12	-	- 23	5,10,13	-	0.70	-	-	8	1,16
	Ісво	4	-	1.5	-	-	1.0	-	1.0	μAdc	-	9,12	-	-53	5,10,13	-5	90. 42. 5	1 -	-	8,4	1,1
ogic "1" Output Voltage	VOH	2 3	-1.060 -1.060	-0.890 -0.890	-0.960 -0.960	_	-0.810 -0.810	-0.890 -0.890	-0.700 -0.700	Vdc Vdc	9,12	9,12	-	- 18	5,10,13 5,10,13	-	3 43	-	-	8	1,1
ogic "0" Output Voltage	VOL	2 3	-1.890 -1.890	-1.675 -1.675	-1.850 -1.850	-	-1.650 -1.650	-1.825 -1.825	-1.615 -1.615	Vdc Vdc	9,12	4 9,12	- 68	- 10	5,10,13 5,10,13	-8	1 54	-	-	8	1,1
ogic "1" Threshold Voltage	VOHA	2 3	-1.080 -1.080	-	-0.980 -0.980	_	-	-0.910 -0.910	-	Vdc Vdc	9,12	9,12	4	4	5,10,13 5,10,13	-	E 7	TIN	-	8 8	1,1
Logic "O" Threshold Voltage	VOLA	2 3	21	-1.655 -1.655	-	_	-1.630 -1.630	- 3	-1.595 -1.595	Vdc Vdc	9,12	9,12	4	4	5,10,13 5,10,13	78	1 50	- 1	-	8	1,1
Reference Voltage	VBB	11	-1.420	-1.280	-1.350	-	-1.230	-1.295	-1.150	Vdc	-	- 1	-1	-83	5,10,13	-62	(+ P)	y - 0	-	8	1,1
Common Mode Rejection Test	VOH	2 3	-1.060 -1.060	-0.890 -0.890	-0.960 -0.960	-	-0.810 -0.810	-0.890 -0.890	-0.700 -0.700	Vdc Vdc	_	- 8	- 14	- 15	1 45 0	4	5	- 5	4	8	1,1
BI 10 75	VOL	2 3	-1.890 -1.890	-1.675 -1.675	-1.850 -1.850	-	-1.650 -1.650	-1.825 -1.825	-1.615 -1.615	Vdc Vdc	-	- 2	218	- 0	072	4	5	5 -	4	8 8	1,1
Switching Times (50-ohm Load)			Min	Max	Min	Тур	Max	Min	Max				Pulse In	Pulse Out	2 cs	10	5.0			-3.2 V	+2.0
Propagation Delay**	t4+2+ t4-2- t4+3- t4-3+	2 2 3 3	1.0	4.4	1.0	2.4	4.0	0.9	4.3	ns	-	1111	84 W 052	2 2 3 3	5,10,13	1787	15,1 4,3 to		-	8	1,10
Rise Time (20% to 80%)	t ₂₊ t ₃₊	2 3	1.5	3.8	1.5	2.1	3.5	1.5	3.7		-	- 4	11 11	2 3	108	2 - 5 2 - 1	18.48	-	_		
Fall Time (20% to 80%)	t2- t3-	2 3	*	*	*		*			V	-	1 4	2.95	2 3		800	1	3 -	-	+	

^{*}V_{IHH} - Input logic "1" level shifted positive one volt for common mode rejection tests

 V_{ILH} - Input logic "0" level shifted positive one volt for common mode rejection tests V_{IHL} - Input logic "1" level shifted negative one volt for common mode rejection tests

V_{ILL} - Input logic "0" level shifted negative one volt for common mode rejection tests

^{**}Delay is 2.0 ns with differential input

3

QUAD LINE RECEIVER

The MC10115 is a quad differential amplifier designed for use in sensing differential signals over long lines. The base bias supply (VBB) is made available at pin 9 to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necessary.

Active current sources provide the MC10115 with excellent common mode noise rejection. If any amplifier in a package is not used, one input of that amplifier must be connected to VBB (pin 9) to prevent upsetting the current source bias network.

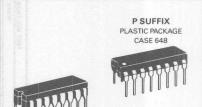
 $P_D = 110 \text{ mW typ/pkg (No Load)}$

 $t_{pd} = 2.0 \text{ ns typ}$

 t_r , $t_f = 2.0$ ns typ (20%–80%)

MECL 10K SERIES

QUAD LINE RECEIVER

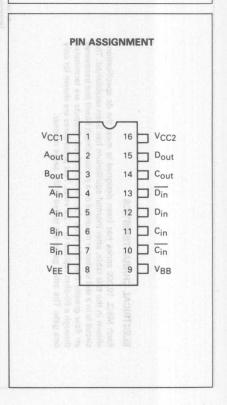


CERAMIC PACKAGE CASE 620

LOGIC DIAGRAM

4
5
7
6
3
10
14
11
13
15
15
VBB
9

VCC1 = Pin 1
VCC2 = Pin 16
VEE = Pin 8



Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

	@ Test	TEST VOLTAGE VALUES														
	Temperature	V _{IH} max	VIL min	VIHA min	VILA max	VBB	VEE									
	-30°C	-0.890	-1.890	-1.205	-1.500	From	-5.2									
	+25°C +85°C	-0.810	-1.850	-1.105	-1.475	Pin	-5.2									
		-0.700	-1.825	-1.035	-1.440	9	-5.2									

										01100						
Characteristic	177 187 1	Pin Under	MC10115 Test Limits													
	100		-30°C		+25°C		+85°C			TEST VOLTAGE APPLIED TO PINS LISTED BELOW:						(Vcc)
	Symbol	Test	Min	Max	Min	Max	Min	Max	Unit	VIH max	VIL min	VIHA min	VILA max	VBB	VEE	Gnd
Power Supply Drain Current	1E	8	-	29	-	26	-	29	mAdc	- 0	4,7,10,13	10 m	北上四	5,6,11,12	8	1,16
Input Current	lin H	4	-	150	-	95	-	95	μAdc	4	7,10,13	2 5	- a - B	5,6,11,12	8	1,16
	СВО	4	-	1.5	-	1.0	-	1.0	μAdc	- 9	7,10,13	-	12 5	5,6,11,12	8,4	1,16
Logic "1" Output Voltage	VOH	2	-1.060	-0.890	-0.960	-0.810	-0.890	-0.700	Vdc	7,10,13	4	5 to to	8 7 8	5,6,11,12	8	1,16
Logic "0" Output Voltage	VOL	2	-1.890	-1.675	-1.850	-1.650	-1.825	-1.615	Vdc	4	7,10,13	- 10 to	0 2 2	5,6,11,12	8	1,16
Logic "1" Threshold Voltage	VOHA	2	-1.080	E/ - 500	-0.980		-0.910	-	Vdc	2 - 3	7,10,13		4	5,6,11,12	8	1,16
Logic "0" Threshold Voltage	VOLA	2	-	-1.655	-	-1.630	-	-1.595	Vdc	- 3	7,10,13	4	1 to 10	5,6,11,12	8	1,16
Reference Voltage	VBB	9	1.420	1.280	-1.350	-1.230	1.295	-1.150	Vdc	- 3	文学 5	e # P	7.5 8	5,6,11,12	8	1,16
Switching Times (50 Ω Load)	5	31.8	DA B	3			1		6	Puls	eIn	Pulse Out		161	-3.2 V	+2.0 V
Propagation Delay	t4-2+ t4+2-	2 2	1.0	3.1 3.1	1.0	2.9 2.9	1.0	3.3 3.3	ns	4 5 9 9		10 01	2 5,6,11,1		8	1,16
Rise Time (20% to 80%)	t ₂₊	2	1.1	3.6	1.1	3.3	1.1	3.7	8 8		3 2 9		1 4 2 5	300		
Fall Time (20% to 80%)	t2-	2	1.1	3.6	1.1	3.3	1.1	3.7	. 1	E 18	1 2 2 3 1	1255				



MC10116

TRIPLE LINE RECEIVER

The MC10116 is a triple differential amplifier designed for use in sensing differential signals over long lines. The base bias supply (VBB) is made available at pin 11 to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necessary.

Active current sources provide the MC10116 with excellent common mode noise rejection. If any amplifier in a package is not used, one input of that amplifier must be connected to VBB (pin 11) to prevent upsetting the current source bias network.

Complementary outputs are provided to allow driving twisted pair lines, to enable cascading of several amplifiers in a chain, or simply to provide complement outputs of the input logic function.

 $P_D = 85 \text{ mW typ/pkg (No Load)}$

 $t_{pd} = 2.0 \text{ ns typ}$

 t_r , $t_f = 2.0$ ns typ (20%–80%)

MECL 10K SERIES

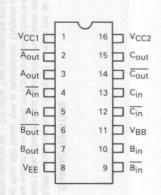
TRIPLE LINE RECEIVER

P SUFFIX
PLASTIC PACKAGE
CASE 648



CASE 620





LOGIC DIAGRAM

2
5
9
6
10
7
12
13
15
VBB

VCC1 = Pin 1
VCC2 = Pin 16
VEE = Pin 8

Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

a li senzi		TE	ST VOLTAGE	VALUES		
1 10 115			(Volts)		44.65	199
@ Test					8 5	3.0
Temperature	VIH max	VIL min	VIHA min	VILA max	VBB	VEE
-30°C	-0.890	-1.890	-1.205	-1.500	From	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	Pin	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	11	-5.2

										+85°C	-0.700	-1.825	-1.035	-1.440	11	-5.2	
		Pin			M	IC10116	Test Limi	ts				TEST VOLT	AGE APPLIED	TO DINE DE	1.014		
		Under	-3	0°C		+25°C		+8	5°C			TEST VOLT	AGE AFFLIEL	TOPINS BE	LOW.		(Vcc
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	VIH max	V _{IL} min	VIHA min	VILA max	VBB	VEE	Gnd
Power Supply Drain Current	1E	8		23	-	17	21	-	23	mAdc	-	4,9,12	- 37	ō	5,10,13	8	1,16
Input Current	linH	4	-	150	-	-	95	3	95	μAdc	4	9,12	- 9	-	5,10,13	8	1,16
	СВО	4	-	1.5	-	-	1.0		1.0	μAdc	-	9,12	- 3	-	5,10,13	8,4	1,16
High Output Voltage	VOH	2 3	-1.060 -1.060	-0.890 -0.890	-0.960 -0.960	-	-0.810 -0.810	-0.890 -0.890	-0.700 -0.700	Vdc Vdc	4 9,12	9,12 4	-18	9100	5,10,13 5,10,13	8 8	1,16 1,16
Low Output Voltage	VOL	2 3	-1.890 -1.890	-1.675 -1.675	-1.850 -1.850	-	-1.650 -1.650	-1.825 -1.825	-1.615 -1.615	Vdc Vdc	9,12 4	4 9,12	1 5	-	5,10,13 5,10,13	8	1,16 1,16
High Threshold Voltage	VOHA	2 3	-1.080 -1.080	-	-0.980 -0.980	_	_	-0.910 -0.910	-	Vdc Vdc	9,12	9,12	4	4	5,10,13 5,10,13	8	1,16 -1,16
Low Threshold Voltage	VOLA	2 3	-	-1.655 -1.655	1-	-	-1.630 -1.630		-1.595 -1.595	Vdc Vdc	9,12	9,12	4	4 -	5,10,13 5,10,13	8	1,16
Reference Voltage	VBB	11	-1.420	-1.280	-1.350	-	-1.230	-1.295	-1.150	Vdc	- 1	2 - 3	- 1	3 - 3	5,10,13	8	1,16
Switching Times (50 12 Load)			Min	Max	Min	Тур	Max	Min	Max			1 2	Pulse In	Pulse Out		-3.2 V	+2.0
Propagation Delay	t ₄₊₂₊ t ₄₋₂₋ t ₄₊₃₋ t ₄₋₃₊	2 2 3 3 3	1.0	3.1	1.0	2.0	2.9	1.0	3.3	ns	-	- lake a	4 600 98	2 2 3 3 3	5,10,13	8	1,16
Rise Time (20% to 80%)	t ₂₊	3	1.1	3.6	1.1		3.3	1.1	3.7		-	2 2 8	100	3			
Fall Time (20% to 80%)	t2- t3-	2						+			-	12 12 T		2 3	8	+	

3

DUAL 2-WIDE 2-3-INPUT "OR-AND/OR-AND-INVERT" GATE

The MC10117 is a general purpose logic element designed for use in data control, such as digital multiplexing or data distribution. Pin 9 is common to both gates.

P_D = 100 mW typ/pkg (No Load)

 $t_{pd} = 2.3 \text{ ns typ}$

 t_r , $t_f = 2.2 \text{ ns typ } (20\%-80\%)$

MECL 10K SERIES

DUAL 2-WIDE 2-3-INPUT
"OR-AND/OR-AND-INVERT"
GATE

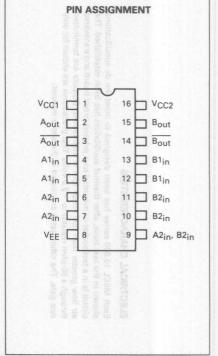


CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648



VCC1 = Pin 1 VCC2 = Pin 16 VEE = Pin 8



Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

		TEST	OLTAGE VA	LUES		
			(Volts)			
@ Test Temperature	VIH max	VIL min	VIHA min	VILA max	VEE	
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2	
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2	
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2	

									+85-C	-0.700	-1.825	-1.035	-1.440	-5.2	7.72b
	D:				MC10	117 Test	Limits		200	TEOT 14		DI IED TO DIA	C LICTED DEL	OW	
		-30	°C		+25°C		+8	5°C		IEST VI	DL TAGE AP	PLIED TO PIN	IS LISTED BEL	.Ow:	(Vcc)
Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	VIH max	V _{IL min}	VIHA min	VILA max	VEE	Gnd
1E	8	-	29	-	20	26	-	29	mAdc	-	-	- 5	-	8	1,16
lin H*	6	-	425	-	-	265	-	265	μAdc	4	-	- 9	-	8	1,16
	9	-	560	-	-	350	-		μAdc	9	7	-	E	100	1,16
	4	-	390	-	-	245	-	245	μAdc	-	4	- w	-	8	1,16
lin L	4	0.5	-	0.5	-	-	0.3	-	μAdc	-	9	- /6 /	-	8	1,16
VOH	2	-1.060	890	-0.960	-	810	-0.890	2000	Vdc	4,9	- 1	- 8		8	1,16
	3	-1.060	-0.780	-0.960	-	-0.700	-Q.890	-0.590	Vdc	-	- 9	- m	the manufacture of	8	1,16
VOL	2	-1.890	-1.675	-1.850	-	-1.650	-1.825	-1.615	Vdc	- 3	-0	- 2	#4.0	8	1,16
	-		-1.675			-1.650		-1.615	Vdc	4,9	- 5	-	7 - 5		1,16
VOHA	2	-1.080	-0	-0.980	-	-	-0.910	-	Vdc	9	- 63	4	2 5 %	8	1,16
	3	-1.080	-	-0.980	-	10 -	-0.910	-	Vdc		- 8	- 3	4	8	1,16
VOLA	2	-	-1.655	-	-	-1.630	-	-1.595	Vdc	-	- 5	- 8	4	8	1,16
	3	1-1	-1.655	/ -	-	-1.630	-	-1.595	Vdc	9		4	-	8	1,16
						12				+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 \
t4+2+	2	1.4	3.9	1.4	2.3	3.4	1.4	3.8	ns	9	0-5	4	2	8	1,16
t4-2-		PIP	979	PF				10 VA	1		2 - E	1 5		1	
						1					1 7-3				
	The state of			V				V					3		
t ₂₊	3	0.9	4.1	1.1	2.2	4.0	1.1	4.6			-	05	2 3		
t2-	2										g-a		2		
	IE Iin H* Iin L VOH VOL VOHA VOLA **t4+2+ **t4-2- **t4+3- **t4-3+ **t4-3+ **t3+	IE 8 In H* 9 4 Iin L 4 VOH 2 3 VOL 2 3 VOLA 2 3 VOLA 2 3 VOLA 2 3 14+2+ 14-2- 14-3- 14-3+ 12- 13+ 12- 2	Under -30	Under -30°C	Under -30°C	Pin -30°C	Pin -30°C	Symbol Test Min Max Min Typ Max Min IE	Pin Under Test Min Max Min Typ Max Min Max Min Max Min Typ Max Min Max	Pin Under Test Min Max Min Typ Max Min Max Min	Pin Under Test Min Max Min Typ Max Min Max Min Min Max Min Typ Max Min Max Min Min Max Min Min	Pin Under Test Test Test Test Test Test Vol TAGE AP	Pin Under Test Te	Pin Under Test Min Max Min Typ Max Min Max Min	Pin Under Test Te

^{*} Inputs 4, 5, 12 and 13 Have Same I_{in H} Limit Inputs 6, 7, 10 and 11 Have Same I_{in H} Limit

MC10118

DUAL 2-WIDE 3-INPUT "OR-AND" GATE

The MC10118 is a basic logic building block providing the OR/ AND function, useful in data control and digital multiplexing applications.

P_D = 100 mW typ/pkg (No Load)

 $t_{pd} = 2.3 \text{ ns typ}$

 t_{Γ} , $t_{f} = 2.5 \text{ ns typ } (20\%-80\%)$

MECL 10K SERIES

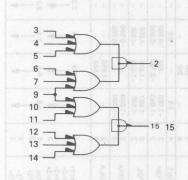
DUAL 2-WIDE 3-INPUT "OR-AND" GATE

> P SUFFIX PLASTIC PACKAGE CASE 648



L SUFFIX CERAMIC PACKAGE CASE 620

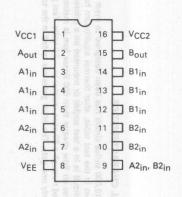
LOGIC DIAGRAM



V_{CC1} = Pin 1 V_{CC2} = Pin 16 V_{EE} = Pin 8

3-30

PIN ASSIGNMENT



3

Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

8		TEST	VOLTAGE VAL	UES	
			(Volts)		
@ Test Temperature	VIH max	VIL min	VIHA min	VILA max	VEE
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

	T		1							-00 0	0.700	1.020	, 11000			1
		Pin			М	-	3 Test Lin	-	-		TEST \	OLTAGE AP	PLIED TO PIN	S LISTED BEL	OW:	1
		Under	-30	-		+25°C		-	5°C			.,	.,	T v	V	(VCC)
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	VIH max	VIL min	VIHA min	VILA max	VEE	Gnd
Power Supply Drain Current	1E	8	-	29	-	20	26	-	29	mAdc	-	-	-1		8	1,16
Input Current	lin H*	6 12	-	425	-		265	1	265	μAdc	6		-	-	8	1,16
		12	-	390		-	245	-	245	1	7				1	1
		9	-	560	-		350	+	350		9	-		-	V	V
	lin L	6	0.5	-	0.5	-	-	0.3	-	μAdc	-	6	9 -		8	1,16
		7	1	-	4	-	-	1	-	1		7	5 -	4 4 W		
		9	*	-	٧	-	77-		-		-	9		17-10		,
Logic "1" Output Voltage	VOH	2	-1.060	-0.890	-0.960	-	-0.810	-0.890	-0.700	Vdc	3,9	- 3	B - 13	是平	8	1,16
Logic "0" Output Voltage	VOL	2	-1.890	-1.675	-1.850	-	-1.650	-1.825	-1.615	Vdc	-	2	6 - 4		8	1,16
Logic "1" Threshold Voltage	VOHA	2	-1.080	-	-0.980	-	At-	-0.910	-	Vdc	9	-	3	G- A-	8	1,16
Logic "0" Threshold Voltage	VOLA	2	-	-1.655	-	-	-1.630	-	-1.595	Vdc			9 - 31	3	8	1,16
Switching Times (50 \(\Omega \) Load)	-						- 63	11.1	1000		+1.11 V	9 9	Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t6 + 2+	2	1.4	3.9	1.4	2.3	3.4	1.4	3.8	ns	3	2 7	6	2	8	1,16
	t6 - 2-	L	1.4	3.9	1.4	2.3	3.4	1.4	3.8	1	1	2 3	7 1 8	12		
Rise Time (20 to 80%)	t+		0.8	4.1	1.5	2.5	4.0	1.5	4.6			2 2	8 8			
Fall Time (20 to 80%)	2 t-		0.8	4.1	1.5	2.5	4.0	1.5	4.6			-				

^{*} Inputs 3, 4, 5, 12, 13 and 14 Have Same I $_{\rm in~H}$ Limit Inputs 6, 7, 10 and 11 have same I $_{\rm in~H}$ Limit

3

4-WIDE 4-3-3-3-INPUT "OR-AND" GATE

The MC10119 is a 4-Wide 4-3-3-3-Input OR/AND gate with one input from two gates common to pin 10.

P_D = 100 mW typ/pkg (No Load)

 $t_{pd} = 2.3 \text{ ns typ}$

 t_r , $t_f = 2.5$ ns typ (20%–80%)

MECL 10K SERIES

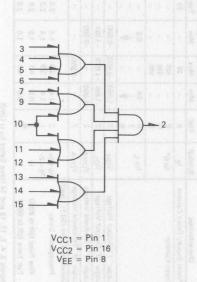
4-WIDE 4-3-3-3-INPUT "OR-AND" GATE



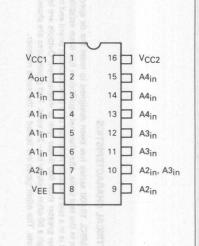
P SUFFIX PLASTIC PACKAGE CASE 648



LOGIC DIAGRAM



PIN ASSIGNMENT



Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

		TEST	OLTAGE VAL	UES	
			(Volts)		
@ Test Temperature	V _{IH max}	VIL min	VIHA min	VILA max	VEE
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

		Pin			M	C10119	Test Lin	nits			TEST	OLTAGE AP	PLIED TO PIN	S LISTED BEL	ow:	
		Under	-30	°C		+25°C		+85	5°C					1		(VCC)
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	VIH max	VIL min	VIHA min	VILA max	VEE	Gnd
Power Supply Drain Current	1E	8	1 - 1	29	-	20	26	-	29	mAdc		D	- 1, 5	21-	8	1,16
Input Current	lin H*	3	-	390	-	-	245	-	245	μAdc	7	2 - 2	- 克音	C)-	8	1,16
		10	-	495	-	-	310	-	310	*	10	9 - =	-09	-	*	-
	lin L	7	0.5	-	0.5	-	-	0.3	-	μAdc		7	7 6 3	33-	8	1,16
Logic "1" Output Voltage	VOH	2	-1.060	-0.890	-0.960	-	-0.810	-0.890	-0.700	Vdc	3,10,15	15 - 五	= -13	51-	8	1,16
Logic "0" Output Voltage	VOL	2	-1.890	-1.675	-1.850	-	-1.650	-1.825	-1.615	Vdc	-	0 0 3	583	55-04	8	1,16
Logic "1" Threshold Voltage	VOHA	2	-1.080	-	-0.980	-	5	-0.910	-	Vdc	10,15	3 7 5	3	1,-13	8	1,16
Logic "0" Threshold Voltage	VOLA	2	4-	-1.655	-	-	-1.630	-	-1.595	Vdc		5 5 7	e T 9	3	8	1,16
Switching Times (50 Ω Load)		100	1	1		111/8	2	KAN			+1.11 V	进 打 事	Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t3+2+	2	1.4	3.9	1.4	2.3	3.4	1.4	3.8	ns	10,13		3 2 6	2	8	1,16
	t3-2-	111	1.4	3.9	1.4	2.3	3.4	1:4	3.8			K 1 1	125			
Rise Time (20 to 80%)	t+		0.8	4.1	1.5	2.5	4.0	1.5	4.6	5.1		15 g- Q	1 2 4	- 12		
Fall Time (20 to 80%)	t-		0.8	4.1	1.5	2.5	4.0	1.5	4.6	*	*		*	V	-	

^{*}Inputs 3,4,5,6,7,9,11,12,13,14,15 Have Same I_{in H} Limit

MC10121

4-WIDE "OR-AND/OR-AND-INVERT" GATE

The MC10121 is a basic logic building block providing the simultaneous OR-AND/OR-AND-INVERT function, useful in data control and digital multiplexing applications.

 $P_D = 100 \text{ mW typ/pkg (No Load)}$

 $t_{pd} = 2.3 \text{ ns typ}$

 t_r , $t_f = 2.5 \text{ ns typ } (20\%-80\%)$

MECL 10K SERIES

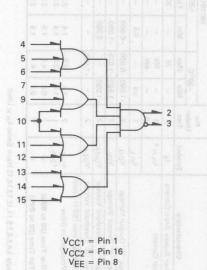
4-WIDE
"OR-AND/OR-AND-INVERT"
GATE

P SUFFIX PLASTIC PACKAGE CASE 648

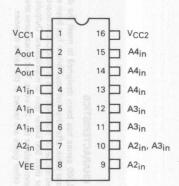


L SUFFIX CERAMIC PACKAGE CASE 620

LOGIC DIAGRAM



PIN ASSIGNMENT



3

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

		TEST	VOLTAGE VA	LUES	
			(Volts)		
@ Test Temperatur	viH max	VIL min	VIHA min	VILA max	VEE
-30°	C -0.890	-1.890	-1.205	-1.500	-5.2
+25°	C -0.810	-1.850	-1.105	-1.475	-5.2
+850	C _0.700	-1.825	-1 035	-1 440	-5.2

										+85-C	-0.700	-1.825	-1.035	-1.440	-5.2	1
		D:				MC10	121 Test Li	mits	la balance		750714			C LIETER DE	OW	
		Pin Under	-30	oC .		+25°C		+85	5°C		TEST VI	JL1AGE AP	PLIED TO PIN	IS LISTED BEI	.Ow:	(Vcc
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	VIH max	VIL min	VIHA min	VILA max	VEE	Gnd
Power Supply Drain Current	1E	8	-	29	-	20	26	-	29	mAdc	- 8	0 23	- 40	4 4 5	8	1,16
Input Current	lin H	7 9 10	-	390 390 495	-	-	245 245 310	-	245 245 310	μAdc	7 9 10	nuba Naka pre j	P P P		8	1,16
	lin L	7 9 10	0.5	81-	0.5	- 100	-	0.3	-	μAdc	1 1 1	7 9 10	ar s a	Set change	8	1,16
Logic ''1'' Output Voltage	VOH	3	-1.060 -1.060	-0.890 -0.890	-0.960 -0.960	-	-0.8 <u>10</u> -0.8 <u>10</u>	-0.890 -0.890	-0.700 -0.700	Vdc Vdc	4,10,13	100 H	10.4 6	日本計画	8	1,16 1,16
Logic ''0'' Output Voltage	VOL	3 2	- <u>1.890</u> -1.890	-1.675 -1.675	-1.850 -1.850	Z	-1.650 -1.650	-1.825 -1.825	-1.615 -1.615	Vdc Vdc	4,10,13	25.5		0 5 3 8	8	1,16 1,16
Logic "1" Threshold Voltage	Vона	3 2	-1.080 -1.080	282	-0.980 -0.980	Ē	18 -	-0.910 -0.910	- 23	Vdc Vdc	10,13	A	4	4 -	8	1,16 1,16
Logic "0" Threshold Voltage	VOLA	3 2	(A.T.)	-1.655 -1.655	11=		-1.630 -1.630	17.	-1.595 -1.595	Vdc Vdc	10,13	9 4 6	4	4	8	1,16 1,16
Switching Times (50 \O Load)	38		9	10 10	- 0 /0	1 1	N 19		0.5	3.0	+1.11 V	2 1/2	Pulse In	Pulse Out	-3.2 V	+2.0
Propagation Delay	t4+3- t4-3+ t4+2+ t4-2-	3 3 2 2	1.4	3.6	1.4	2.3	3.4	1.4	3.5	ns a	10,13	o perqui	49a EST Organish	3 3 2 2	8	1,16
Rise Time (20 to 80%)	t3+ t2+	3 2	0.9	4.1	1.1	2,5	4.0	1.1	4.6		580	1 S T S		3 2		
Fall Time (20 to 80%)	t3- t2-	3 2	+	+		V		*	1		19 9	2 4 4	20 6 3	3 2		

^{*}This is advance information and specifications are subject to change without notice.



MC10123

TRIPLE 4-3-3 INPUT BUS DRIVER

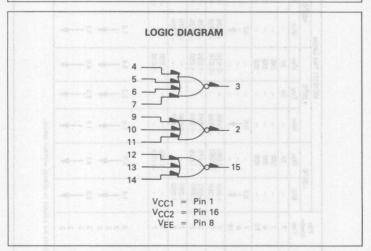
The MC10123 consists of three NOR gates designed for bus driving applications on card or between cards. Output low logic levels are specified with $V_{\text{OL}} \leqslant -2.0$ Vdc so that the bus may be terminated to -2.0 Vdc. The gate output, when low, appears as a high impedance to the bus, because the output emitter-followers of the MC10123 are "turned-off." This eliminates discontinuities in the characteristic impedance of the bus.

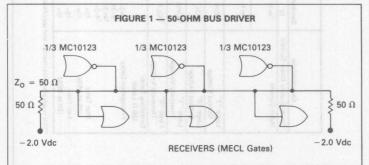
The V_{OH} level is specified when driving a 25-ohm load terminated to -2.0 Vdc, the equivalent of a 50-ohm bus terminated at both ends. Although 25 ohms is the lowest characteristic impedance that can be driven by the MC10123, higher impedance values may be used with this part. A typical 50-ohm bus is shown in Figure 1.

P_D = 310 mW typ/pkg (No Load)

 $t_{pd} = 3.0 \text{ ns typ}$

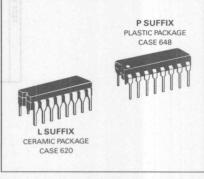
 t_r , $t_f = 2.5 \text{ ns typ } (20\%-80\%9)$

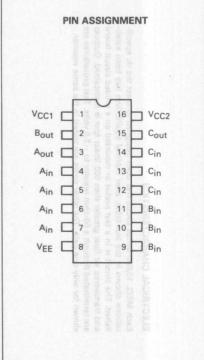




MECL 10K SERIES

TRIPLE 4-3-3 INPUT BUS DRIVER





Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 25-ohm resistor to $-2.1\,\text{volts}$. Test procedures are shown for only one input an one output. The other inputs and outputs are tested in the same manner.

444		TEST V	OLTAGE VALU	JES	Salet.
@ Test			(Volts)		
Temperature	VIH max	VIL min	V _{IHA} min	VILA max	VEE
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

										.00 0	0.700	1.020	1.000	- Part - 172 - 175 - 175	0.0	99
		Pin		J. HE	P	VC1012	3 Test L	imits			TEST	VOLTAGE A	PPLIED TO PIN	S LISTED BEL	.ow:	
		Under	-30	0°C		+25°C		+85	°C	O.	350	0.59	UT 10 10 10	13 3 0 5		(Vcc)
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	VIH max	VIL min	VIHA min	VILA max	VEE	Gnd
Power Supply Drain Current	1E	8	-	82	-	71	75	-	82	mAdc	4,5,6,7,9,10 11,12,13,14	DYSE IN	Option of the contract of the	1111	8	1,16
Input Current	linH	4	-	350	-	-	220	1-1	220	μAdc	4	7 - 9	2 2	27-23	8	1,16
	linL	4	-	- 1	0.5	-	-	-	-	μAdc	2 2 3 3	4	E B C A	をかたら	8	1,16
Logic "1" Output Voltage	Voн	3	-1.060	-0.890	-0.960	-	-0.810	-0.890	-0.700	Vdc	2233	240		1 11 1	8	1,16
Logic "0" Output Voltage	VOL	3	-2.15	-2.030	-2.15	-	-2.030	-2.15	-2.030	Vdc	4,5,6,7,9,12	335		1000	8	1,16
Logic "1" Threshold Voltage	Vона	3	-1.080	- 1	-0.980	-	1	-0.910	49	Vdc	10 14 15 16 16 16 16 16 16 16 16 16 16 16 16 16	1978		4,5,6,7	8	1,16
Logic "0" Threshold Voltage	VOLA	3	A-1	-2.010	-	-	-2.010	1-1	-2.010	Vdc	9,12	1011	4,5,6,7	8 94 8	8	1,16
Switching Times (25-ohm load)		-					2		54	44 A	2555	1 3 a 3	Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t ₄₊₃₋	3	1.2	4.6	1.2	3.0	4.4	1.2	4.8	ns	E E E E	1 1 2 1	4	3	8	1,16
	t4-3+		1.2	4.6	1.2	3.0	4.4	1.2	4.8	1	N-10 - 12 -	1 4 5 5	17151	3 3 6 5		
Rise Time (20 to 80%)	t ₃₊		1.0	3.7	1.0	2.5	3.5	1.0	3.9		100	8 8 8 8		SA S	1 8	
Fall Time (20 to 80%)	t3_	*	1.0	3.7	1.0	2.5	3.5	1.0	3.9		8888	100	8 4 8 8	11111		*



MC10124

QUAD TTL TO MECL TRANSLATOR

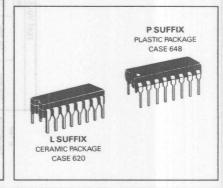
The MC10124 is a quad translator for interfacing data and control signals between a saturated logic section and the MECL section of digital systems. The MC10124 has TTL compatible inputs, and MECL complementary open-emitter outputs that allow use as an inverting/non-inverting translator or as a differential line driver. When the common strobe input is at the low logic level, it forces all true outputs to a MECL low logic state and all inverting outputs to a MECL high logic state.

Power supply requirements are ground, +5.0 Volts, and -5.2 Volts. Propagation delay of the MC10124 is typically 3.5 ns. The dc levels are standard or Schottky TTL in, MECL 10,000 out.

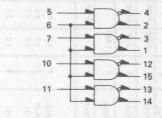
An advantage of this device is that TTL level information can be transmitted differentially, via balanced twisted pair lines, to the MECL equipment, where the signal can be received by the MC10115 or MC10116 differential line receivers. The MC10124 is useful in computers, instrumentation, peripheral controllers, test equipment, and digital communications systems.

 P_D = 380 mW typ/pkg (No Load) t_{pd} = 3.5 ns typ (+ 1.5 Vdc in to 50% out) t_{r} , t_{f} = 2.5 ns typ (20%–80%) MECL 10K SERIES

QUAD TTL TO MECL TRANSLATOR

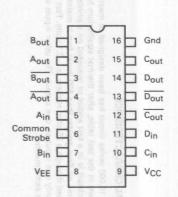


LOGIC DIAGRAM



Gnd = Pin 16 $V_{CC} (+5.0 Vdc) = Pin 9$ $V_{EE} (-5.2 Vdc) = Pin 8$

PIN ASSIGNMENT



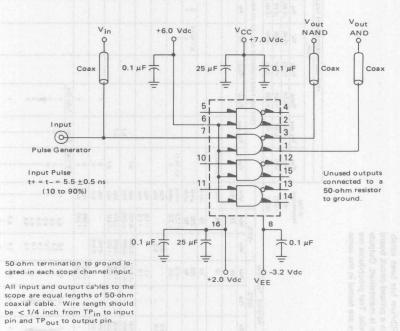
Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to $-2.0\,$ volts. Test procedures are shown for only one translator. The other translators are tested in the same manner.

			TE	ST VOLTA	GE/CURRE	NT VALU	ES			
	and the same			V	olts	2			f	nA
@ Test Temperature	VIH	V _{1L max}	V _{IHA}	VILA.	VF	VR	Vcc	VEE	14	lin
- 30°C	+4.0	+0.40	+2.00	+1.10	+0.40	+2.40	+5.00	-5.2	-10	+1.0
+25°C	+4.0	+0.40	+1.80	+1.10	+0.40	+2.40	+5.00	-5.2	-10	+1.0
+85°C	+4.0	+0.40	£1.80	+0:90	+0.40	+2.40	+5.00	-5.2	-10	+1.0

		Elizabeth with					1755		7	00 C	+4.0	+0.40	+1.80	+0.90	+0.40	+2.40	+5.00	-5.2		T1.0	
		Pin			MC	10124 T	est Limits			1	1	1/			1 1						The Maria
	1 3 1 4 5	Under	-3	0°C		+25°C		+8	5°C			TE:	ST VOLTAG	E/CURRE	NT APPLIED	TO PINS	S LISTED B	ELOW:			5 - 1
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	VIH	VIL max	VIHA'	VILA'	VF	VR	Vcc	VEE	h	Iin	Gnd
Negative Power Supply Drain Current	1E	8		72			-66		72	mAdc	1 7 1	1.1	A to			-	9	8			16
Positive Power Supply Drain Current	Іссн	9		16		-	16	- 10	18	mAdc	5,6,7,10,11						9	8			16
	ICCL	9		25			25	1 -71	25	mAdc	19	11/19	3124-				9	8			5,6,7,10,11,10
Reverse Current	IR.	6 7	-	200 50		-	200 50		200 50	μAdc μAdc					5,7,10,11	6 7	9 9	8			16 16
Forward Current	1F	6 7		-12.8 -3.2		-	-12.8 -3.2		- 12.8 - 3.2	mAdc mAdc	5,7,10,11				6 7		9 9	8 8			16 16
Input Breakdown Voltage	BVin	6 7	5.5 5.5	9.0	5.5 5.5	-	-	5.5 5.5		Vdc Vdc							9	8 8		6 7	5,7,10,11,16 6,16
Clamp Input Voltage	VI	6 7		-1.5 -1.5		-	-1.5 -1.5		- 1.5 - 1.5	Vdc Vdc							9 9	8	6 7		16 16
High Output Voltage	VOH	1 3	-1.060 -1.060	-0.890 -0.890	-0.960 -0.960		-0.810 -0.810	-0.890 -0.890	-0.700 -0.700	Vdc Vdc	6,7	6,7		3			9 9	8 8	1		16 16
Low Output Voltage	VOL	1 3	-1.890 -1.890	-1.675 -1.675	-1.850 -1.850	10	-1.650 -1.650	-1.825 -1.825	-1.615 -1.615	Vdc Vdc	6,7	6,7					9	8			16 16
High Threshold Voltage	VOHA	1 3	-1,080 -1,080	-	-0.980 -0.980		1 1	-0.910 -0.910		Vdc Vdc	6 6		7	7	75		9 9	8			16 16
Low Threshold Voltage	VOLA	1 3		-1.655 -1.655	- 1		-1.630 -1.630		-1.595 -1.595	Vdc Vdc	6		7	7			9 9	8 8			16 16
Switching Time (50-52 load)						0 2 6 3				10	+6.0 Vdc	Pulse In	Pulse Out			7	+7.0 Vdc	-3.2 Vdc			+2.0 Vdc
Propagation Delay (+3.5 Vdc to 50%)①	¹ 6+1+ ¹ 6-1- ¹ 7+1+ ¹ 7-1- ¹ 7+3- ¹ 7-3+	3 3	1.5 1.0 1.5 1.0 1.5 1.0	6.8 6.0 6.8 6.0 6.8 6.0	1.0	3.5	6.0	1.0 1.5 1.0 1.5 1.0 1.5	6.0 6.8 6.0 6.8 6.0 6.8	ns	7 7 6	6 6 7	3 3				9	8			16
Rise Time (20% to 80%)	11+	1	1.0	4.2	1.1	2.5	3.9	1.1	4.3				1								
Fall Time (80% to 20%)	31.	1	¥	*	1.1	2.5	3.9	V	V	-	-		1				-				-

① See switching time test circuit. Propagation delay for this circuit is specified from +1.5 Vdc in to the 50% point on the output waveform. The +3.5 Vdc is shown here because all logic and supply levels are shifted 2 volts positive.)





NOTE: All power supply and logic levels are shown shifted 2 volts positive.

MECL 10K SERIES

QUAD MECL TO TTL

TRANSLATOR



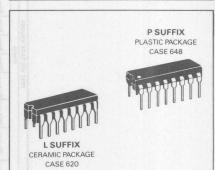
QUAD MECL TO TTL TRANSLATOR

The MC10125 is a quad translator for interfacing data and control signals between the MECL section and saturated logic sections of digital systems. The MC10125 incorporates differential inputs and Schottky TTL "totem pole" outputs. Differential inputs allow for use as an inverting/non-inverting translator or as a differential line receiver. The VBB reference voltage is available on pin 1 for use in single-ended input biasing. The outputs of the MC10125 go to a low logic level whenever the inputs are left floating.

Power supply requirements are ground, +5.0 Volts and -5.2 Volts. Propagation delay of the MC10125 is typically 4.5 ns. The MC10125 has fanout of 10 TTL loads. The dc levels are MECL 10,000 in and Schottky TTL, or TTL out. This device has an input common mode noise rejection of \pm 1.0 Volt.

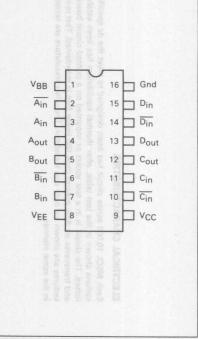
An advantage of this device is that MECL level information can be received, via balanced twisted pair lines, in the TTL equipment. This isolates the MECL logic from the noisy TTL environment. This device is useful in computers, instrumentation, peripheral controllers, test equipment and digital communications systems.

 P_D = 380 mW typ/pkg (No Load) t_{pd} = 4.5 ns typ (50% to + 1.5 Vdc out) t_{r} , t_{f} = 2.5 ns typ (1.0 V to 2.0 V)



PIN ASSIGNMENT

2 3 4 6 7 5 10 12 14 15 VBB Gnd = Pin 16 VCC (+5.0 Vdc) = Pin 9 VFF (-5.2 Vdc) = Pin 9 VFF (-5.2 Vdc) = Pin 8

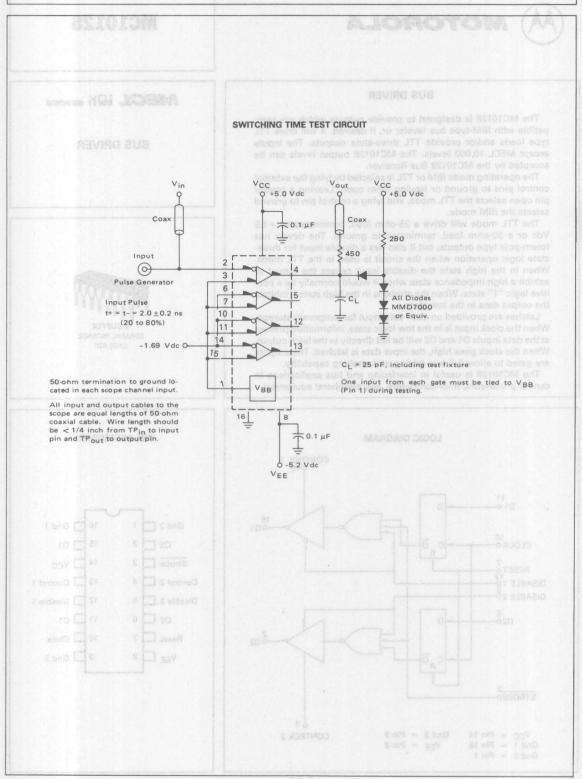


Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Test procedures are shown for only one translator. The other translators are tested in the same manner.

				TEST	VOLTA (Vo	AGE VA	LUES	1		Allower.	
@ Test Temperature	VIH max	VIL min	VIHAmin	VILAmax	VIHH	VILH	VIHL	VILL	VBB	vcc	VEE
-30°C	-0.890	-1.890	-1.205	-1.500	+0.110	-0.890	-1.890	-2890	From	+5.0	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	+0.190	-0.850	-1.810	-2.850	Pin	+5.0	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	+0.300	-0.825	-1.700	-2.825	1	+5.0	-5.2

		Pin			MC1	0125 T	est Limits						TEST V	OLTAGE A	PPLIE	D TO P	NS LIS	TED BE	LOW:		3		
		Under	-30	°С		+25°C		+8	5°C		-	1	1							52 NV	6		Output
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	VIH max	VIL min	VIHA min	VILAmax	VIHH	VILH	VIHL	VILL	VBB	Vcc	VEE	Gnd	Conditio
Negative Power Supply Drain Current	1E	8	-	44	-	-	40		44	mAdc	-	action and a	5-6	- 3	0	7-0	-	1	3,7,11,15	9	. 8	16	-
Positive Power Supply	ССН	9	-	52	-	-	52	-	52	mAdc	2,6,10,14	-	<- N	B - 3	2	25° N	-	1 43	3,7,11,15	9	8	16	-
Drain Current	ICCL	9		39		-	39	+	39	mAdc	1 -	2,6,10,14	11-1	-	1	- 3	- 1	-57	3,7,11,15	9	8	16	-
Input Current	In H ①	2		180	-	-	115	-	115	μAdc	2,6,10,14	9.3		-, 1	1	E-9	-		3,7,11,15	9	8	16	16 .
Input Leakage Current	СВО	2	-	1.5	-	-	1.0	+ 1	1.0	μAdc	- 6	m	-	- 0	- 2	U	-	8 -55	3,7,11,15	9	2,6,8,10,14	16	
High Output Voltage	VOH	4	2.5	-	2.5	-	-	2.5	-	Vdc	-	2,6,10,14		- 1	10	-	-	5-1	3,7,11,15	9	8	16	-2.0 mA
Low Output Voltage	VOL	4	-	0.5	-	-	0.5	-	0.5	Vdc	2,6,10,14	- 9	-0-	-	-	0-1	-	-	3,7,11,15	9	8	16	20 mA
High Threshold Voltage	VOHA	4	2.5	-	2.5	-	-	2.5	-	Vdc) 22	6,10,14	11-	2	-	10-	-	-5	3,7,11,15	9	8	16	-2.0 mA
Low Threshold Voltage	VOLA	4	- 0	0.5	-	-	0.5	+	0.5	Vdc	6,10,14	3 3	2	3 -4 2	-	-17	-	-	3,7,11,15	9	8	16	20 mA
Indeterminate Input Protection Tests	VOLS1	4	-	0.5	-	-	0.5	1	0.5	Vdc	3 4	5 9	g-2	EE:	- in	2-5	-	7	3 7 5	9	2,3,6,7,8, 10,11,14,15	16	20 mA
	VOLS2	4	-	0.5	1 -	-	0.5	+ 1	0.5	Vdc	-	=	30-01	0	-		-	-	9 5 6	9	8	16	20 mA
Short-Circuit Current	los	4	40	100	40	-	100	40	100	mA		2,6,10,14	3-11	- 1	-	-	-	+7	3,7,11,15	9	8	4,16	
Reference Voltage	VBB	1	-1.420	-1.28	-1.350	-	-1.230	-1.295	-1.150	Vdc	1 2	2,6,10,14	0-1-	-	-	-	-	-	3,7,11,15	12-10	17 - 20	57-	-
Common Mode	VOH	4	2.5	W- 1	2.5	-	-	2.5	-	Vdc	3	5 5		-	3	2	-		D = 1	9	8	16	-2.0 mA
Rejection Tests		4	2.5	B- I	2.5	-	(-)	2.5	-			**	07-85	P 3 0		-17	3	2	0 3 5	9	8	16	-2.0 mA
	VOL	4	_	0.5 0.5		-	0.5 0.5	-	0.5 0.5	Vdc	2 6	= 5	8-8	1 1	2	3	2	3	0 4 9	9	8 8	16 16	20 mA 20 mA
Switching Times	126	8 13	9.11	O5 (5)	1.60		100			10	Pulse In	Pulse Out	CL (pF)	F 65	9	5 18		F 10	D 6 -	10 10	6	-	
Propagation Delay (50% to +1.5 Vdc)	t6+5- t6-5+ t2+4- t2-4+	5 5 4	1.0	6.0	1.0	4.5	6.0	1.0	6.0	ns	6 6 2	5 5 4	25	Polishing Polishing	DISTOR	5-1 3-1 3-8	-	Split Spe	3,7,11,15	9	8	16	=
Rise Time (+1.0 Vdc to 2.0 Vdc) Fall Time (+1.0 Vdc to 2.0 Vdc)	t4+ t4-		-	3.3	1	-	3.3 3.3	-	3.3	1	1		1 de	0 10	10.10	8-3	-	13			2	+	-

¹ Individually test each input, apply VIH max to pin under test.



BUS DRIVER

The MC10128 is designed to provide outputs which are compatible with IBM-type bus levels; or, if desired, it will drive TTL type loads and/or provide TTL three-state outputs. The inputs accept MECL 10,000 levels. The MC10128 output levels can be accepted by the MC10129 Bus Receiver.

The operating mode IBM or TTL is selected by tying the external control pins to ground or leaving them open. Leaving a control pin open selects the TTL mode, and tying a control pin to ground selects the IBM mode.

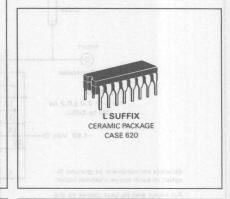
The TTL mode will drive a 25-ohm load, terminated to +1.5 Vdc or a 50-ohm load, terminated to ground. The device has totem-pole type outputs, but it also has a disable input for three-state logic operation when the circuit is used in the TTL mode. When in the high state the disable input causes the output to exhibit a high impedance state when it would normally be a positive logic "1" state. When the strobe is in the high state it inhibits the output data in the low state.

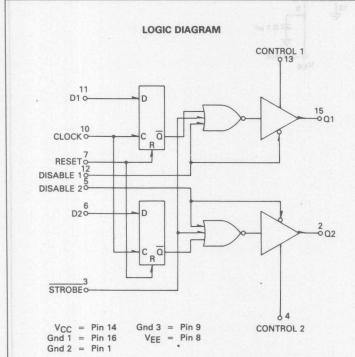
Latches are provided on each data input for temporary storage. When the clock input is in the low logic state, information present at the data inputs D1 and D2 will be fed directly to the latch output. When the clock goes high, the input data is latched. The outputs are gated to allow full bus driving and strobing capability.

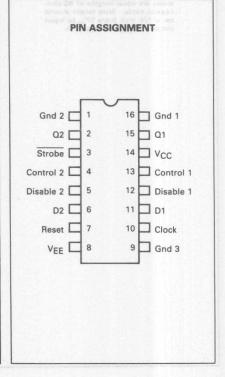
The MC10128 is useful in interfacing and bus applications in central processors, mini-computers, and peripheral equipment.

MECL 10K SERIES

BUS DRIVER







ELECTRICAL CHARACTERISTICS — TTL MODE

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained.

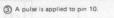
			TEST	VOLTAGE/	CURRE	NT VA	LUES		
		TEST V	OLTAGE V	ALUES	distal.	1	mAdc	μAdc	mAdc
			Volts				1		
@ Test Temperature	VIHmax	VILmin	VIHAmin	VILAmax	VEE	Vcc	ГОН1	10Н2	lor
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2	5.00	-50	-100	+56
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2	5.00	-50	-100	+56
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2	5.00	-50	-100	+56

Negative Power Supply Drain Current Positive Power Supply Drain Current	Symbol IE ICC	Under Test 8 14	-30 Min -	0°C Max 100	H2!	Max 91	+8! Min	Max 100	Unit mAdc	VIHmax 6.11	VILmin		VILAmax	VEE	Vcc	I _{OH1}	I _{OH2}	lor	Gnd
Negative Power Supply Drain Current Positive Power Supply Drain Current Input Leakage Current	IE ICC	8 14 3 7	8-	100	Min	91					VILmin	VIHAmin	VILAmax	VEE	Vcc	IOH1	IOH2	IOL	Gnd
Drain Current Positive Power Supply Drain Current Input Leakage Current	lcc	14 3 7	7	50	0 -			100	mAdc	0.11									
Drain Current Input Leakage Current	1237-5	3 7	13	513	1	50			1 3	0,11	-	- 40°		8	14			-	1, 9,16
	linH	7	-			n la		50	mAdc	6,11	1		- 1	8	14		1		1, 9,16
	1	10	1	490 560 425	-	620 350 265		620 350 265	μAdc	3 7 10	0X-140	L U A Trosto	- 	8	14	-	i i		1, 9,16
Contact Digen is from Countries	100	11 12	Ī	425 775	80] 162]	265 485)6] 6]	265 485	3	11 12		E		1	* +	13	Ī		
	linL	All	0.5	10.4.9	0.5	-	0.3	20	μAdc	- 1		- 3	-	8	14	-	+	-	1, .9 .10
Logic "1" Output Voltage	VOH	15 15	2.5	-	2.5	1	2.5	-	Vdc Vdc	11		T I	10.0	8	14 14	2,15	2,15		1, ,9 ,10
Logic "0" Output Voltage	VOL	15 2	-	0.5		0.5	id.	0.5 0.5	Vdc Vdc	3				8	14 14		1	2,15 2,15	1, .9 .10
Logic "1" V Threshold Voltage	Vона	15 2	2.5	1	2.5		2.5		Vdc Vdc	11	7 7		10 3 3 10 3	8	14 14	2,15 2,15	-t-		1, .9 ,10
Logic ''0'' V Threshold Voltage	VOLA	15	1	0.5	1	0.5 0.5		0.5	Vdc Vdc	11	7,10 7,10	3		8	14 14		T	2,15 2,15	1, ,9 ,10
Output Short Circuit Current	¹sc	15 2	-	260 260		260 260	-	260 260	mAdc mAdc	11 6		E	= -	8	14		T I	1	1,2, ,9 ,15 1,2, ,9 ,15
Switching Times † Propagation Delay	3000				8		ē,		6 h.	-0.890 V	-1.690 V	Pulse In	Pulse Out						
Clock Input t ₁₀	11+15+ 11-15- 10-15+	15 15 15 ①	1.0 1.0 1.0	17 17 20	1.0 1.0 1.0	18 18 20	1.C 1.0 1.0	24 24 25	ns	90 - 91	10 10	11 11 10,11	15	8	14		Ī		1, 9 ,1
Reset Input t7	7+15- 17+2-	15 ② 15 ② 2 ②	1.0 1.0 1.0	20 20 20	1.0 1.0 1.0	20 20 20	1.0 1.0 1.0	25 25 25	bs les	11		10,11 7,10 7,10	2		8 A	10 10	1 10	H,	1 Ass
STROBE Input t3	3+15- 3-15+ t3+2-	15 15 2	1.0 1.0 1.0	17 17 17	1.0 1.0 1.0	18 18 18	1.0 1.0 1.0	24 24 24		11 - 6	10	3 10	15 15	11901	D HER	e triĝi et	BELDIN'		
t	t3-2+ setupH	2	1.0	17	1.0	18	1.0	24	100 pl	200	N + 48	10.11	2		0.3	00.1-2	3 - 3		
man goo moss the tee	setupL	15		43	0.5	0.8	-	-	- 20,0	T 011	n - 13		PE -1.80		8 8 6	G27 - 8			
th.	holdL	15 15		-	0.6	0.8	200	-	e i er	-	10	11					1		
	t15-	15	1.0	9.0	1.0	8.0	1.0	9.0	+		10	11		1	1		- I	1-2-	1

Apply VILmin individually to pin under test.

1 Output latched to logic Low state prior to test.

† See waveforms

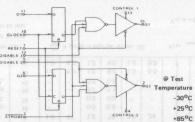


VILA 100 nsec min

② Output latched to logic High state prior to test.

ELECTRICAL CHARACTERISTICS - IBM MODE

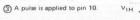
Each MECL 10,000 series circuit has been designed to meet the dc specifications AESE10 shown in the test table, after thermal DISABLE 20equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained.

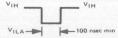


	TEST V	OLTAGE V	ALLIES		7	mAdc		dc
	I COI V		ALUES			mauc	μе	I I
	10 -	Volts						
VIHmax	VILmin	VIHAmin	VILAmax	VEE	Vcc	10Н1	10Н2	IOL
-0.890	-1.890	-1.205	-1.500	-5.2	+6.00	-59.3	-30	-230
-0.810	-1.850	-1.105	-1.475	-5.2	+6.00	-59.3	-30	-230
-0.700	-1.825	-1.035	-1.440	-5.2	+6.00	-59.3	-30	- 230

	10	Pin		1 8	1000 F 100	128 Te	st Lim	its			TE	ST VOLTA	GE APPLIE	тор	INS LIS	STED BEI	ow.		
	1448-	Under	-30	o°C	+25	5°C	+8	5°C		12	10 1	3 1	16						
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Unit	VIHmax	VILmin	VIHAmin	VILAmax	VEE	Vcc	IOH1	I _{OH2}	IOL	Gnd
Negative Power Supply Drain Current	JE .	8	0 1	107	-	97	-	107	mAdc	6,11		7 LE -	1-11	8	14				1,4,9,13,16
Positive Power Supply Drain Current	lcc	14	o F	73	1	73	- 5	73	mAdc	6,11	0 -	-	1-11	8	14				1,4,9,13,16
Input Leakage Current	linH	3 7 10	Ī	990 560 425	Ī	620 350 265		620 350 265	μAdc	3 7 10	EQ AL DA	- - 1 1	- oni	8	14				1,4,9,13,16
	IR I	11 12	-3	425 775	-31	265 485	_	265 485		11 12	1	2 1		1	1				3 15 6
	linL	All	0.5	-	0.5	-	0.3	- 1	μAdc	8 - 3	-0 .	-	- 1 8	8	14			BILL	1,4,9,13,16
Logic "1" Output Voltage	VOH	15 15	3.11	5.85	3.11	5.85	3.11	5.85	Vdc Vdc	11		-	WIT I	8	14	2,15	2,15		1,4,9,13,16 1,4,9,13,16
Logic "0" Output Voltage	VOL	15 2	-0.5 -0.5	0.15 0.15	-0.5 -0.5	0.15 0.15	-0.5	0.15 0.15	Vdc Vdc	3	-			8	14		1 5	2,15 2,15	1,4,9,13,16 1,4,9,13,16
Logic "1" Threshold Voltage	VOHA	15 2	3.11	T	3.11	TS	3.11	TIV	Vdc Vdc	11	7	-	10 3 3	8	14 14	2,15 2,15	18 1.		1,4,9,13,16 1,4,9,13,16
Logic "0" Threshold Voltage	VOLA	15 2	-0.5 -0.5	0.25	-0.5 -0.5	0.25 0.25	-0.5 -0.5	0.25	Vdc Vdc	11	7,10 7,10	3	-	8	14	1		2,15 2,15	1,4,9,13,16 1,4,9,13,16
Output Short Circuit Current	Isc	15	İ	320 320	E	320 320	- 8	320 320	mAdc mAdc	11 6	1	-		8	14	-			1,2,4,9,13,15,
Switching Times † Propagation Delay	out -		51 %	9 -	Min	Max	1 38	0 0	reje	-0.890 V	-1.690 V	Pulse In	Pulse Out						Line 1
Data Input	t11+15+ t11-15-	15 15	1.0 T	21	1.0	23.0	1.0	33.0	ns	120 -	10 10	11 11	15	8	14				1,4,9,13,16
Clock Input	t10-15+ t10-15-	15 ① 15 ②	10	20				0 4	erqs.	111 -	-	10,11		28		1			F 8'18
Reset Input	t7+15- t7+2-	15 ② 2 ②	10 150	20	er ve	24	o ge	×	ent. K	11 6	miri Vi	7,10 7,10	2 A	al le	200	1 10	61 16		010
STROBE Input	t3+15- t3-15+	15 15		21	10. 30	ine:				11	10	ori3de	15	DINE.	188	REFOM			
	t3+2- t3-2+	2 2	1	21	+	+	+	198.	6	6	100	100	2 2	21	0 -		00 9	6	
Setup Time	t _{setupH}	15 15	=	-	.7	1.0	-	-35)		1980 -/	830 - 1	10,11	15		0 -1		10	9	
Hold Time 16 164 Brocker &	tholdH tholdL	15 15	bZau	artio artic	.7	1.1	-	1300			3			4	-				
Rise Time (20% to 80%) Fall Time (20% to 80%)	t 15+	15	1.0	8.0	1.0	8.0	1.0	9.0	1	18	10	11	12	1	1	di Thy	es un	ge	

Apply V_{ILmin} individually to pin under test.

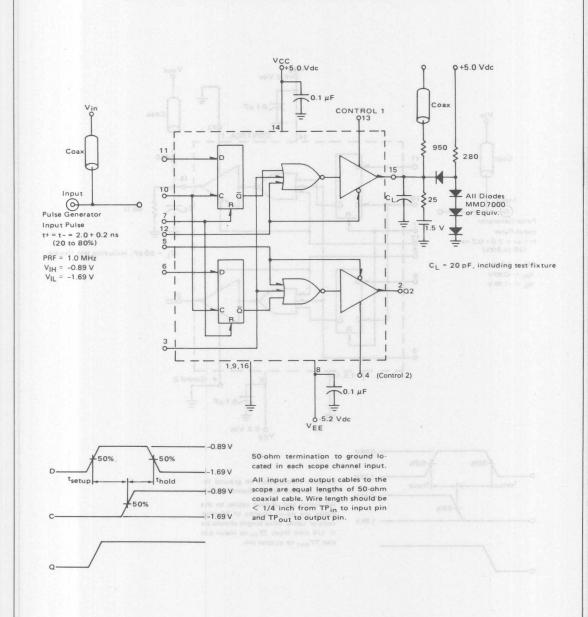




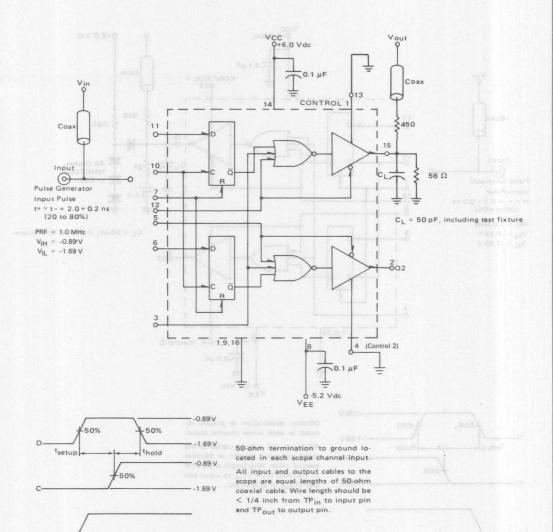
① Output latched to logic Low state prior to test.

② Output latched to logic High state prior to test. † See waveforms

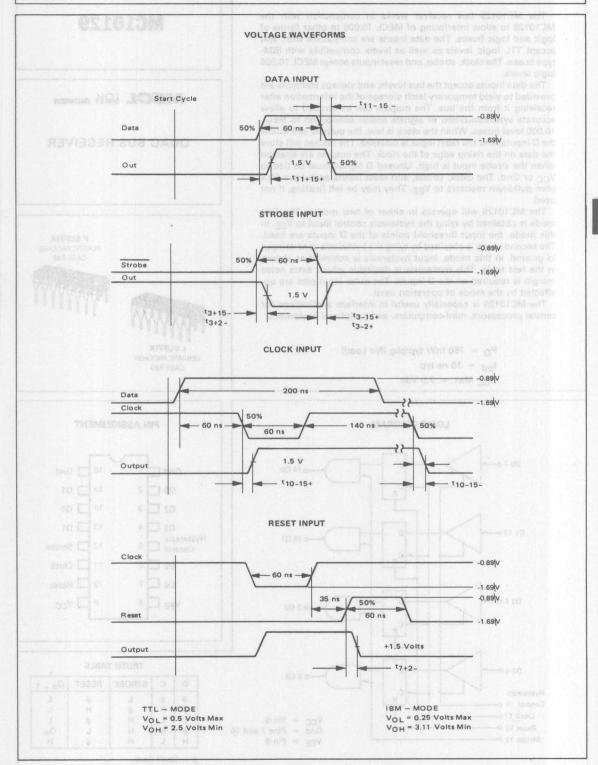
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C - TTL MODE



SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C - IBM MODE







QUAD BUS RECEIVER

The MC10129 bus receiver works in conjunction with the MC10128 to allow interfacing of MECL 10,000 to other forms of logic and logic buses. The data inputs are compatible with, and accept TTL logic levels as well as levels compatible with IBM-type buses. The clock, strobe, and reset inputs accept MECL 10,000 logic levels.

The data inputs accept the bus levels, and storage elements are provided to yield temporary latch storage of the information after receiving it from the bus. The outputs can be strobed to allow accurate synchronization of signals and/or connection to MECL 10,000 level buses. When the clock is low, the outputs will follow the D inputs, and the reset input is disabled. The latches will store the data on the rising edge of the clock. The outputs are enabled when the strobe input is high. Unused D inputs must be tied to VCC or Gnd. The clock, strobe, and reset inputs each have 50 k ohm pulldown resistors to VEE. They may be left floating, if not used.

The MC10129 will operate in either of two modes. The first mode is obtained by tying the hysteresis control input to V_{EE}. In this mode, the input threshold points of the D inputs are fixed. The second mode is obtained by tying the hysteresis control input to ground. In this mode, input hysteresis is achieved as shown in the test table. This hysteresis is desirable where extra noise margin is required on the D inputs. The outer input pins are unaffected by the mode of operation used.

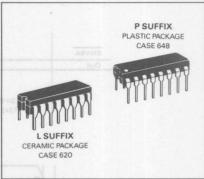
The MC10129 is especially useful in interface applications for central processors, mini-computers, and peripheral equipment.

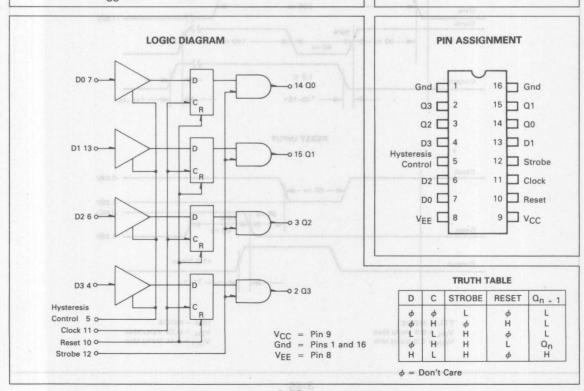
 $P_D = 750 \text{ mW typ/pkg (No Load)}$ $t_{pd} = 10 \text{ ns typ}$ $V_{CC} \text{ Max} = 7.0 \text{ Vdc}$

MC10129

MECL 10K SERIES

QUAD BUS RECEIVER





Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one input/output combination. Other combinations are tested in the same manner.

												_	-	-	-			_	(V	olts)	_			-			1	_	-
											MEC	L 10,000	INPUT LE	VELS		* TTL IN	PUT LEV	ELS		"IBM IN	PUT LEVE	LS		HYSTERI	ESIS MOD	E			
									@ Te Temper	ature	VIHmax	VILmin		VILAmax		VIL	VIHA.	VILA	VIH	VIL	VIHA.	VILA.	VIHA"	VILA"	VIHA	VILA"	v _{cc} ①		
										30°C	-0.890	-1.890	-1.205	-1 500	3 000		2.000	0.800	3.11	0.150	-	100	2.90	2.00	2.20	1.30	+5.0	-5.2	
										25°C	-0.810	-1.850	-1 105	-1.475	3.000		2.000	0.800		0.150	1.700	0.70	2.600	1.700	1.900	1.000	+5.0	-5.2	
									+1	85°C	-0.700	-1.825	-1.035	-1.440	3 000	0.400	2 000	0.800	3.11	0.150	- 1	-	2.30	1.400	1.60	0.70	+5.0	-5.2	1
		Pin			MC	10129	Test Limit	1							TEST	OI TAGE	APPLIED	TO PINS	LIETE	n BELOW									
	C.	Under	-3	0°C		+25°C		+81	5°C													1.7							
Characteristic	Symbol	Yest	Min	Мах	Min	Тур	Мах	Min	Max	Unit	VIHmax	VILmin	VIHAmir	VILAmax	VIH	VIL	VIHA.	VILA.	VIH	VIL	VIHA.	VILA.	VIHA"	VILA"	VIHA	VILA"	Vcc ①	VEE	Gnd
Negative Power Supply Drain Current	ıε	8	7	167 189			152 172		167	mAdo mAdo	11	12	1			14-1	1	1			1	4		1	-	-	9	8 5.8	1,5,16
Positive Power Supply Drain Current	Icc	9		8.0			8.0		8.0	mAdo						4.6.7.13		ME.		4,6,7,13	-	3	1	11-	-	-	9	5,8	1,16
Input Current	linH	4	-	150	111	1	95		95	μAdc	-				4	-			4				-	1	-		9	R	1,16
S AUGUST	THE STATE OF THE S	6 7 10 11 12 13		150 150 720 390 390 150			95 95 450 245 245 95		95 95 450 245 245 95		10,11 11 12		E	1	6 7		h		6 7		J				70,04	11111		Ì	Tenan
	cso	6 7	-	1.5	3	-	10		1.0	μAdc	V					6 7				6 7			15	1:4	-31	-	9	8	1.16
	link	13	0.5	-	- 1.0 0.5	1		0.3	-		1	10				13	1133		1	13	5	de l		-	51	1.4	60		18
		11			1		1 -			1		12											1	1				+	1
Logic "1" Output Voltage	Voн	2 3 2	-1.060	-0.890	-0.960	1	-0.810	-0.890	-0.700	Velo	12	10.11			4 6 4				4 6 4		-		-	1-1	3		9	5,8 5,8 8	1,16 1,16 1,5,16
	-	3		,	,	1		1	,	,	1	,			6				6	-		12.	-		- 1	-	-	8	1,5,16
Logic "0" Output Voltage	VOL	3 2 3	-1.89	-1.675	-1.850		-1.650	-1.825	-1 615	Vric	12	10,11				6 4				4 6 4 6		E	6	1:	10.00		9	5,8 5,8 8	1,16 1,16 1,5,16 1,5,16
ogic "1"	VOHA	2 (4)	-1.08		-0.980			-0.910	1	Vdc	11,12		11-11	10	4		7		4		-			1	-		9	5.8	1,16
Threshold Voltage	O.T.	2 2 2							1	1	10,12	10,11	12	ñ	4		4	1	4		1	: \	- 4			-		1	1,5,16
79		2 0		-		1 3		1		+	*	1					1		1	-	1-	-	1-	-	4	- 1	*	8	1,5,16
Logic "0" Threshold Voltage	VOLA	2 (d) 2 (d) 2 (d) 2 (d) 2 (d) 2 (d)		-1.655	1		-1.630		-1.595	Vric	11,12 	10,11	10	12	4 4 4	1 1 1		4	4 4		11111	4	100000	- 4	11.1.1.1	11111	9	5,8	1,16
		2 3	23	7	-13	10	7				7					100		200			, L	34	4	1 -	-	4	*	8	1,5,16
Switching Times	1 118			TE ST	-	40	-		-	-	+1,11 V	+0.31 V	Pulse In	Pulse Out	+5.0 V	+2.40 V	Fig	ure	+5.0 V	+2.40 V	Fig	gure	_				+7.0 V	-32 V	+2.0 V
Propagation Delay Data Input	17+14+	14 14	3.7 3.7	15 15	3.7 3.7	10.0	15 15	3.7	30 40	ns	12	10,11	7 7	14 14				1	1	-		1	-	-	1	-	8	5,8	1,16
	111-14+ 111-14-	14 14	2.7	11	2.7	5.0	9.0	2.7	11		12	10	7,11	14 14			1					4	-	-	-	T	0 6		1
Strobe Input	t12+14+ t12-14-	14	1.6	8.0	1.6	4.0	7.0	1.6	8.0		100	10,11	12	14	7			2	7			2	-	116	1	I			
Reset Input Hysteresis Mode	110+14-	14	2.0 6.6	8.0	6.7	5.0	6.5	6.6	30		12	10.11	10,11	14	7	7			7			3		-	2 1			8	1,5,16
Setup Time	t7-14- tsetup	14	3.7	17	3.7 2.75	10.0	15	3.7	40	10	12	10,11	7,11	14				- 8		2		1			-	-		8 5.8	1,5,16
Hold Time	thold	14	0	-	-2.0	15.0		-2.0			12	10	7,11	14			8		-		1	5	-		-	1		1	1
	14	14	1.5	5.0	1.5	2.0	4.3	1.5	5.0	1.0	12	10.11	2	14					1					144		100			
Rise Time																													

*When testing choose either TTL or IBM Input Levels.

"Whan testing choose either TTL or 18M Input Levels.

(i) Operation and milms shown also apply for Vog. - 46.0 V.

(i) Input level on data input taken from +0.4 V up to voltage level goven.

(i) Input level on data input taken from +0.4 V v down to voltage level goven.

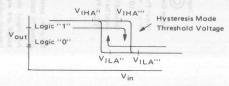
(i) Output is ached to logic high state grinor to state.

(ii) Usuput is ached to logic high state grinor to state.

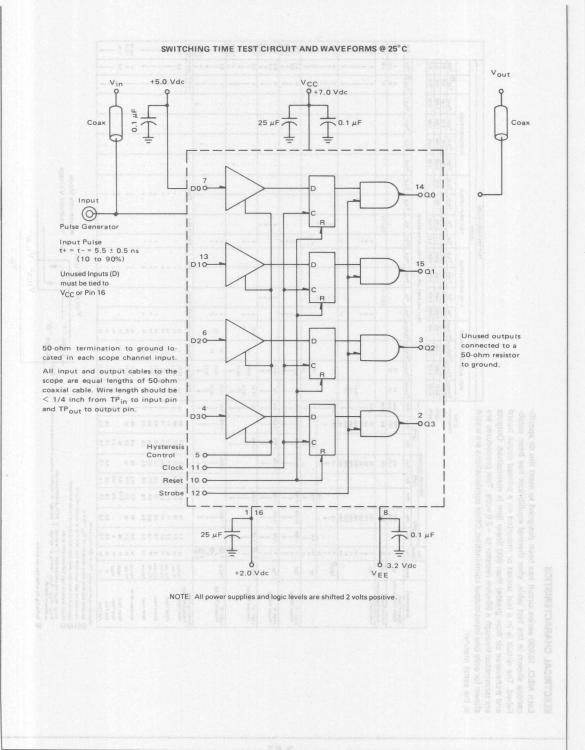
(iii) ViHA, "VILA," VIHA," with "I'm and logic "I" and logic "O" rhyrehold voltages.

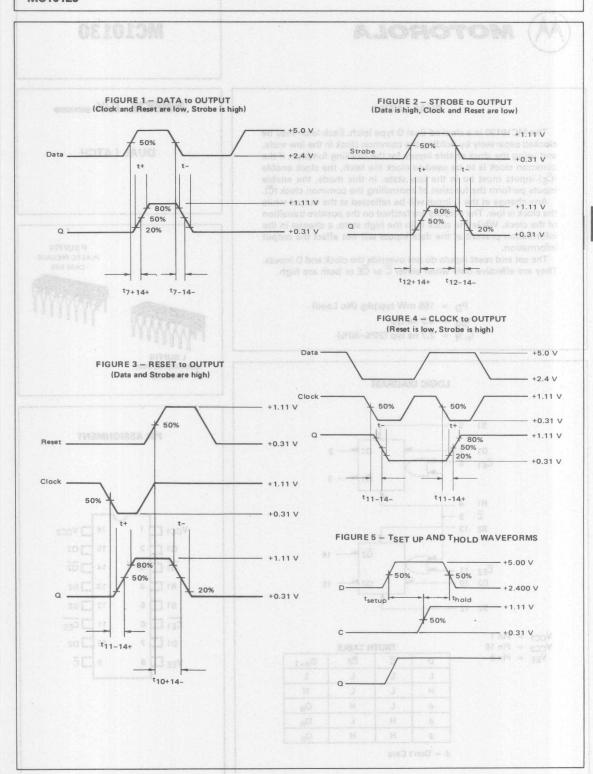
(iii) India, "VILA," VIHA," with "I'm and VILA," are logic "I" and logic "O" rhyrehold voltage in those in ordingerm.

(5) Pin 5 to Vgg. Vil to Date input one at a time



TEST VOLTAGE VALUES





3

DUAL LATCH

The MC10130 is a clocked dual D type latch. Each latch may be clocked separately by holding the common clock in the low state, and using the clock enable inputs for the clocking function. If the common clock is to be used to clock the latch, the clock enable (CF) inputs must be in the low state. In this mode, the enable inputs perform the function of controlling the common clock $(\overline{\mathbb{C}})$.

Any change at the D input will be reflected at the output while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information.

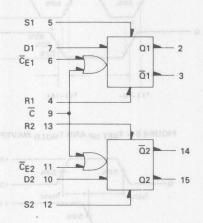
The set and reset inputs do not override the clock and D inputs. They are effective only when either C or CE or both are high.

 $P_D = 155 \text{ mW typ/pkg (No Load)}$

 $t_{pd} = 2.5 \text{ ns typ}$

 t_r , $t_f = 2.7$ ns typ (20%–80%)

LOGIC DIAGRAM



V_{CC1} = Pin 1 V_{CC2} = Pin 16 V_{EE} = Pin 8

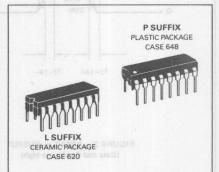
TRUTH TABLE

D	C	CE	Q _{n+1}
L	L	L	L
Н	L	L	Н
φ	L	Н	Qn
φ	Н	L	Qn
φ	Н	Н	Qn

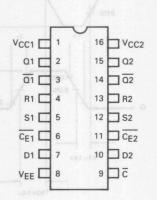
 $\phi = Don't Care$

MECL 10K SERIES

DUAL LATCH



PIN ASSIGNMENT



		TEST	VOLTAGE V	ALUES	940
0.7	439		(Volts)		- 92
@ Test Temperature	VIHmax	VILmin	VIHAmin	VILAmax	VEE
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

				And the second						100 0	-0.700	-1.020	-1.035	-1.440	-0.2	
		Pin			MC	10130	Test Lin	nits			TEST VOI	TAGE AP	PLIED TO PI	NS LISTED B	FLOW-	
		Under	-3	0°C		+25°C		+8	5°C		1201 101	I TAGE AT	1	1		(Vcc
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	VIHmax	VILmin	VIHAmin	VILAmax	VEE	Gnd
Power Supply Drain Current	1 _E	8	-	38	-	30	35	-	38	mAdc	- 3	E 6- 1	2 7 5	1 2 4	8	1,16
Input Current	linH H (S	6,11 9 4,5,7 10,12,13		350 425 - 450	-	1.1.1.1	220 265 - 285	-	220 265 — 285	μAdc	6,11 9 4,5 7,10,12,13	- - - 9	ni sida arii arii	Part of	8	1,16
7 4 4 6 8	linL	4*	0.5	-	0.5	-	-	0.3	-	μAdc	- 3	4	6.2.6	122	8	1,16
Logic "1" Output Voltage	Vон	2	-1.060	-0.890	-0.960	107	-0.810	-0.890	-0.700	Vdc	5	B B-	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	192	8	1,16
Logic "0" Output Voltage	VOL	2	-1.890	-1.675	-1.850	1-	-1.650	-1.825	-1.615	Vdc	4	\$ P-	and the second	169	8	1,16
Logic "1" Threshold Voltage	VOHA	2	-1.080	-	-0.980	6-	-	-0.910	3	Vdc	- 10	9	7	188	8	1,16
Logic "0" Threshold Voltage	VOLA	2	F	-1.655	-	-	-1.630	-	-1.595	Vdc	- 1	9	Blyto Colfe	100	8	1,16
Switching Times (50 Ω Load) (See Figure 1) Propagation Delay	t7+2+ t5+2+	2	1.0	3.6	1.0	2.5 2.7	3.5	1.0	3.8 3.9	ns 	+1.11 V		Pulse In 7 5	Pulse Out	-3.2 V	1,16
I LAKE	t4+2- t6-2+			4.3		2.7	4.0	*	3.9 4.1	8 9	6	3 - 5 5 - 5	6			
Rise Time (20% to 80%) - Fall Time (20% to 80%)	t ₂₊	2 1	¥ =	3.6	1.1	2.7	3.5	1.1	3.8	+	aval	N 100 1	7 7	30	*	*
Setup Time	tsetup	2	2.5	0.3	2.5	15	72-	2.5	-	ns	1	0. %-3 !	6,7	2	8	1,16
Hold Time	thold	2	1.5		1.5	-	-	1.5	-	ns	1	\$ 5-7 B	6,7	2	8	1,16

^{*}All other inputs are tested in the same manner

DUAL TYPE D MASTER-SLAVE FLIP-FLOP

The MC10131 is a dual master-slave type D flip-flop. Asynchronous Set (S) and Reset (R) override Clock (C_C) and $\overline{\text{Clock}}$ $\overline{\text{Enable}}$ (C_E) inputs. Each flip-flop may be clocked separately by holding the common clock in the low state and using the enable inputs for the clocking function. If the common clock is to be used to clock the flip-flop, the $\overline{\text{Clock}}$ $\overline{\text{Enable}}$ inputs must be in the low state. In this case, the enable inputs perform the function of controlling the common clock.

The output states of the flip-flop change on the positive transition of the clock. A change in the information present at the data (D) input will not affect the output information at any other time due to master slave construction.

PD = 235 mW typ/pkg (No Load)

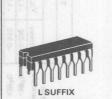
f_{Tog} = 160 MHz typ

 $t_{pd} = 3.0 \text{ ns typ}$

 t_r , $t_f = 2.5$ ns typ (20%–80%)

MECL 10K SERIES

DUAL TYPE D MASTER-SLAVE FLIP-FLOP

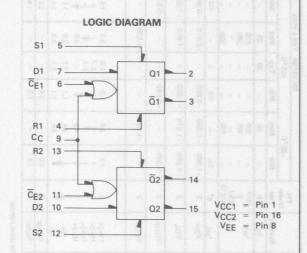


P SUFFIX

PLASTIC PACKAGE

CASE 648

L SUFFIX CERAMIC PACKAGE CASE 620



CLOCKED TRUTH TABLE

С	D	Q _{n+1}
L	φ	Qn
Н	L 3	L
Н	н	Н

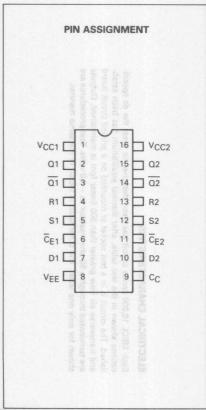
 $\phi = \text{Don't Care}$

C = C_E + C_C. A clock H is a clock transition from a low to a high state.

R-S TRUTH TABLE

R	S	Q _{n+1}
L	L	Qn
L	Н	Н
Ho	L	E &
Н	Н	N.D.

N.D. = Not Defined



Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs tested in the same manner.

	TEST VOLTAGE VALUES (Volts)													
@ Test Temperature														
	V _{IH max}	VIL min	VIHA min	VILA max	VEE									
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2									
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2									
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2									

W E3	1 30	0:		No.	MC10	131 T	est Limits			4 10	VOLTAGE APPLIED TO PINS LISTED BELOW:					
	1 3	Pin	-30	°c		+25°C		+8!	5°C	66	2542000	TOTAL ATTE	ED TOTTING ER	T DECOVE	132	(Vcc)
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	VIH max	VIL min	VIHA min	VILA max	VEE	Gnd
Power Supply Drain Current	1E	8	-	62	-	45	56	- 1	62	mAdc	- A	-	-	-	8	1, 16
Input Current	linH	4	-	525	-	-	330	-	330	μAdc	4	-	-		8	1, 16
		5	-	525			330	-51	330		5		and Tanana			
		7		350 390	_	-	220 245		220 245		7			-		25 7
		9	-	425	_	_	265	_	265	*	9	_				
Input Leakage Current	linL	4,5,* 6,7,9*	0.5 0.5	-	0.5 0.5	-	=	0.3 0.3	_	μAdc μAdc					8 8	1, 16 1, 16
Logic "1" Output Voltage	VOH	2 2†	-1.060 -1.060	-0.890 -0.890	-0.960 -0.960	_	-0.810 -0.810	-0.890 -0.890	-0.700 -0.700	Vdc Vdc	5 7	8 3-1-2	10 A 10 A	£ = £ 5	8	1, 16 1, 16
Logic "0" Output Voltage	VOL	3 3†	-1.890 -1.890	-1.675 -1.675	-1.850 -1.850	6-	-1.650 -1.650	-1.825 -1.825	-1.615 -1.615	Vdc Vdc	5 7	9 K-9 S	100	1	8	1, 16 1, 16
Logic "1" Threshold Voltage	Vона	2 2†	-1.080 -1.080	736	-0.980 -0.980	60T	_	-0.910 -0.910	_	Vdc Vdc	基直引	2 8 2 8	5 7	9	8 8	1, 16 1, 16
Logic "0" Threshold Voltage	VOLA	3 3†	_	- 1.655 - 1.655	_	_	-1.630 -1.630		-1.595 -1.595	Vdc Vdc	\$4.E		5 7	9	8	1, 16 1, 16
Switching Times Clock Input									- Silvi	B (1) fe	+1.11 Vdc	NA STEEL	Pulse In	Pulse Out	-3.2 Vdc	+2.0 Vd
Propagation Delay	t9+2- t9+2+ t6+2+	2 2 2	1.7	4.6	1.8	3.0	4.5	1.8	5.0	ns	7 7	\$ 3-2 d	9 9 6	2 2 2 2	8	1, 16
Rise Time (20 to 80%)	t6+2- t2+	2 2	1.0	(1)	1.1	2.5	2	1.1	4.9	550	7	2 2-0 0	6	2	1 10	
Fall Time (20 to 80%)	t2-	2	1.0		1.1	2.5	1	1.1	4.9		9 3-7 7	2 2 0 8	9	2	1	
Set Input Propagation Delay	t5+2+ t12+15+	2 15	1.7	4.4	1.8	2.8	4.3	1.8	4.8	ns	- 6	10 10 10 10 10 10 10 10 10 10 10 10 10 1	5	2 15	8	1, 16
00-000-8	t5+3- t12+14-	3 14	+					•	-	9.	9	0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	5 12	3 14		
Reset Input Propagation Delay	t4+2- t13+15- t4+3-	2 15 3	1.7	4.4	1.8	2.8	4.3	1.8	4.8	ns	6 A	1 978 pe 1 9	4 13 4	2 15 3	8	1, 16
エトトコストトラ	t13+14+	14		1	*	*				*	9	3 1-5 3	13	14	*	
Setup Time	tsetup	7	2.5	Z)-181	2.5	75	-	2.5	-	ns	1-1-1 E	0.5-0.5	6,7	2	8	1, 16
Hold Time	thold	7	1.5	-	1.5	-	-	1.5	-	ns	9 8-3 1	長 第一年 シー	6,7	2	8	1, 16
Toggle Frequency (Max)	fTog	2	125	-	125	160	-	125	-	MHz	2 7-6 5	0 0-2 0	6	2	8	1, 16

*Individually test each input; apply VIL min to pin under test.

†Output level to be measured after a clock pulse has been applied to the \bar{C}_E input (pin 6) VIA min

3

MC10132

DUAL MULTIPLEXER WITH LATCH AND COMMON RESET

The MC10132 is a dual multiplexer with clocked D type latches. It incorporates common data select and reset inputs. Each latch may be clocked separately by holding the common clock in the low state, and using the clock enable inputs for a clocking function. If the common clock is to be used to clock the latch, the clock enable $(\overline{\text{CE}})$ inputs must be in the low state. In this mode, the enable inputs perform the function of controlling the common clock (C_C).

The data select (A) input determines which data input is enabled. A high (H) level enables data inputs D12 and D22 and a low (L) level enables data inputs D11 and D21. Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information. The reset input is enabled when the clock is in the high state, and disabled when the clock is low.

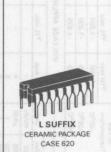
PD = 225 mW typ/pkg (No Load)

 $t_{pd} = 3.0 \text{ ns typ}$

 t_r , $t_f = 2.5 \text{ ns typ } (20\%-80\%)$

MECL 10K SERIES

DUAL MULTIPLEXER WITH LATCH AND COMMON RESET





			- 0	LOG	IC DIAGRAM	
		A 1	1-	2		
	D	11	4			2 01
	D	12	5 —	+		9 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
	(EO 1	0 — 7 —	•	D	3 01
			9 —	4		15 Q2
	D		3	2020		303020
	D	22 1	2	4 4 5		14 02
	T	RUTH	TABL	F		
R	D	СС	CE	Q _{n+1}	D = (Ā ● D1	1) + (A • D12)
φ L L	L L L	L H H	H	L Q _n Q _n	* 150 to state of the country of the	V _{CC1} = Pin 1 V _{CC2} = Pin 16
φ	Н	L	L	Н	12 3 14	VEE = Pin 8

 Q_n

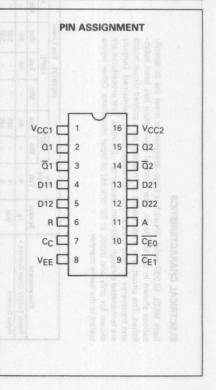
L

HH

Н

H

 $\phi = Don't Care$



Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one latch. The outer latches are tested in the same manner.

					-										
	TEST VOLTAGE VALUES														
		(Volts)													
@ Test															
Temperature	VIH max	VIL min	VIHA min	VILA max	VEE										
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2										
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2										
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2										

										+85-0	-0.700	-1.825	-1.035	-1.440	-5.2	
		Pin	1000		MC101	132 Te	st Limits				TEST VC	I TAGE APP	LIED TO PIN	STISTED BE	LOW:	
		Under	-30°C		+25°C		Title 1	+85°C			TEST VOLTAGE ATT		T TOTAL	S EISTED BE	LOW.	(VC
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	VIH max	VIL min	VIHA min	VILA max	VEE	Gn
	1E	8	-	60	-	44	55	-	60	mAdc	-	200	F-20 1	r 00 -	8	1,1
- 12	lin H	4	73.	460	-	-	290	-	290	μAdc	4	25	@= T	- 2 -	8	1,1
	100	5	-		-	-		=				0.45 2	2 4 3	3 -		
	100		-		-	-					6	是 当 息	67 57	28 -		
		1	Challes !			-		Curry Ca			7	F-5	12 0 3	-		
			1									No. 10 100	F 0 1	0 -		
	-			425		_	1000000		265	,	11.		0 0 0	133 -		-
12	lin L	4*	0.5	-/	0.5	-		0.3	-	μAdc	-	4	- 5	er -	8	1,1
	VOH	2	-1.060		-0.960		-0.810	-0.890	-0.700	Vdc	4	7,9,10	2-30	2 -	8	1,1
		2	-1.060	-0.890	-0.960	-	-0.810	-0.890	-0.700	Vdc	5,11	7,9,10	2 3 3	0 -	8	1,1
10.0	VOL	3	-1.890	-1.675	-1.850	-	-1.650	-1.825	-1.615	Vdc	4	7,9,10	7-53	12 -	8	1,
		3	-1.890	-1.675	-1.850	10 -	-1.650	-1.825	-1.615	Vdc	5,11	7,9,10	-	12	8	1,
-	VOHA	2	-1.080	-	-0.980	9 7	1 -	-0.910	-	Vdc	A -	7,9,10	4	0 - 7	8	1,
		2	-1.080	- 0	-0.980	-	-	-0.910	-	Vdc	11	7,9,10	5	4 10 - 20	8	1,1
	VOLA	3		-1.655	- 1	2 -	-1.630	-	-1.595	Vdc	5 -	7,9,10	4	ES - IP	8	1,
		3	-	-1.655	-	-	-1.630	-	-1.595	Vdc	11	7,9,10	5	12 - 100	8	1,1
load)		- b-		4		6				5 6	+1.11 V	+0.31 V	Pulse In	Pulse Out	-3.2 V	+2.0
Data	taun	2	10	3.6	1.0	0	33	1.0	3.7	ns	10	7910	4	2 2	8	1,1
Reset		11	1			-		1		41.0	7	0 -1 12	6	i i	Ĭ	
Clock		11 7			1.0	-	5.7				_ 4	0.5 %	7	8		
Select	t11+2+	V		4.8	1.0	-	4.6	V	5.0	-	5	7	11	- E		1
Data	tsetup	2	2.5	-	2.5	-	1 -	2.5		ns	-	11	4,10	2	8	1,
Select	tsetup	2	3.5	-	3.5	-	-	3.5		ns	5	7	10,11	2 2	8	1,
Data	thold	2	1.5	-	1.5	-	1 -	1.5	-	ns	-	11	4,10	2	8	1,
Select	thold	2	1.0	-	1.0	-	-	1.0	-	ns	5	7	10,11	2	8	1,
	t2+	2	1.5	3.7	1.5	-	3.5	1.5	3.8	ns	-	7,9,10	4	2	8	1,
	A CONTRACTOR OF THE PARTY OF TH	02 4			1.5	_	3.5	200		ns	_	79.10	4	2	8	1,1
	Data Reset Clock Select Data Select Data	IE	Symbol Test	Symbol Test Min Symbol Test Min Max Symbol Fin Under -30°C	Symbol Fin Under -30°C +25°C	Pin Under -30°C	Symbol Test Min Max Min Typ Max Min Pin Under Test Min Max Min Typ Max Min Max M	Pin Under Test Min Max Min Typ Max Min Max Max Min Typ Max Min Max M	Pin Under Test Min Max Min Typ Max Min Max M	Pin Under Test Min Max Min Typ Max Min Pin Under 1-30°C 1-25°C 1-85°C Pin Under Test MC10132 Test Limits TEST VOLTAGE APPLIED TO PINS LISTED BE	Pin					

^{*}All other inputs tested in the same manner.

M) MOTOROLA

QUAD LATCH

The MC10133 is a high speed, low power, quad latch consisting of four bistable latch circuits with D type inputs and gated Q outputs, allowing direct wiring to a bus. When the clock is high, outputs will follow D inputs. Information is latched on the negative going transition of the clock.

The outputs are gated when the output enable (\overline{G}) is low. All four latches may be clocked at one time with the common clock $(C_{\overline{C}})$, or each half may be clocked separately with its clock enable (\overline{CE}) .

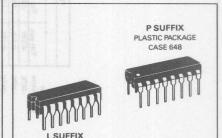
PD = 310 mW typ/pkg (No Load)

 $t_{pd} = 4.0 \text{ ns typ}$

 t_r , $t_f = 2.0 \text{ ns typ } (20\%-80\%)$

MECL 10K SERIES

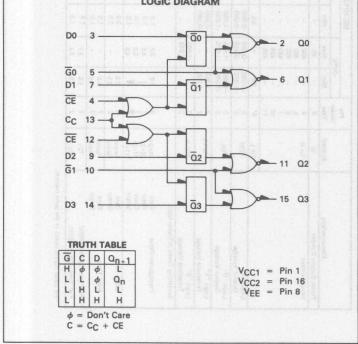
QUAD LATCH

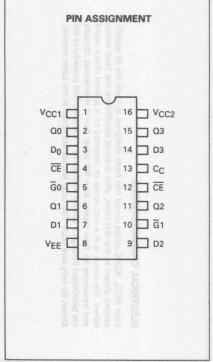


CERAMIC PACKAGE CASE 620

LOGIC DIAGRAM

DO 3 2 Q0





Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

	TEST VOLTAGE VALUES														
		(Volts)													
@ Test Temperature	VIH max	VIL min	VIHA min	VILA max	VEE										
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2										
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2										
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2										

										100 C	-0.700	-1.020	-1.055	-1,440	-0.2	1.0
ar U	(2)- 10	n:-	MC10133 Test Limits								TEST VOLTAGE APPLIED TO PINS LISTED BELOW:					
	P 2	Pin Under	-30°C			+25°C		+8	5°C					1997	_	(Vcc
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	VIH max	VIL min	VIHA min	VILA max	VEE	Gnd
Power Supply Drain Current	1 _E	8	-	82	-	-	75	-	82	mAdc	-	13	-	-	8	1,16
Input Current	linH	3	-	390	-	-	245	-	245	μAdc	3	-	-	-	8	1,16
		5		425 560	-	_	265 350	_	265 350		5	-	1			
		13		560		_	350		350		13	_	_	_		
	linL	3	0.5	_	0.5	-	-	0.3	-	μAdc	-	3		-	8	1,16
Logic "1" Output Voltage	VOH	2 2	-1.060 -1.060	-0.890 -0.890	-0.960 -0.960	-	-0.810 -0.810	-0.890 -0.890	-0.700 -0.700	Vdc Vdc	3,4 3,13	\$ £ £ 1	1 1 5	1333	8	1,16 1,16
Logic ''0'' Output Voltage	VOL	2 2 2	-1.890	-1.675	-1.850	-	-1.650	-1.825	-1.615	Vdc	13 3,5,13 4	3 - 3	11 61	2 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	8	1,16
Logic "1" Threshold Voltage	VOHA	2 2 2	-1.080	= 1	-0.980		-	-0.910	8 - 2 -	Vdc	3,4 4 3,4		3	5	8	1,16
188		2† 2†† 2†† 2 2		- - -		1 - 1 - 3		200 - E07	200 C	Too Blue	3 - - 3 3		- - 4 - 13	4	9880	
Logic ''0'' Threshold Voltage	VOLA	2 2 2 2 2† 2†† 2††		-1.655			-1.630	20 m sh	-1.595	Vdc	3,4 4 4 - 3 3	SC hard so	5	3 13	8	1,16
Switching Times (50 Ω Load)					7			1 1		3	+1.11 V	1 8 3	Pulse In	Pulse Out	-3.2 V	+2.0 \
Propagation Delay	t3+2+ t4+2+ t5-2+ tSetup tHold	2 2 2 3 3	1.0 ↓ 2.5 1.5	5.6 5.4 3.2 —	1.0 2.5 1.5	4.0 4.0 2.0 0.7 0.7	5.4 5.4 3.1 -	1.1 1.2 1.0 2.5 1.5	5.9 6.0 3.4	ns	4 3 * - -		3 4 5 3	2 2 2 2 2	8	1,16
Rise Time (20% to 80%) Fall Time (20% to 80%)	t ₂₊	2 2	1.0	3.6 3.6	1.1	2.0	3.5 3.5	1.1	3.8 3.8		4	201	3	2 2		+

[†]Output level to be measured after a clock pulse has been applied to the clock input (Pin 4).

VIH max

^{*} Latch set to zero state before test.

^{††}Data input at proper high/low level while clock pulse is high so that device latches at proper high/low level for test. Levels are measured after device has latched.

3

MC10134

DUAL MULTIPLEXER WITH LATCH

The MC10134 is a dual multiplexer with clocked D type latches. Each latch may be clocked separately by holding the common clock in the low state, and using the clock enable inputs for the clocking function. If the common clock is to be used to clock the latch, the clock enable $(\overline{\text{CE}})$ inputs must be in the low state. In this mode, the enable inputs perform the function of controlling the common clock (CC).

The data select inputs determine which data input is enabled. A high (H) level on the A0 input enables data input D12 and a low (L) level on the A0 input enables data input D11. A high (H) level on the A1 input enables data input D22 and a low (L) level on the A1 input enables data input D21.

Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information.

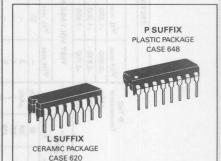
PD = 225 mW typ/pkg (No Load)

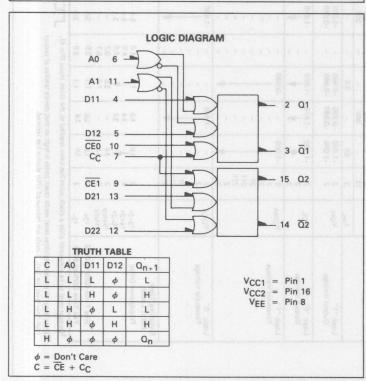
 $t_{pd} = 3.0 \text{ ns typ}$

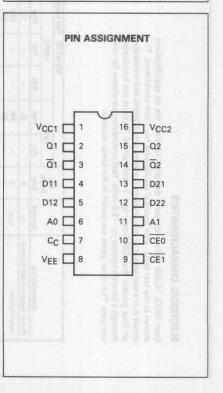
 t_r , $t_f = 2.5 \text{ ns typ } (20\%-80\%)$

MECL 10K SERIES

DUAL MULTIPLEXER
WITH LATCH







ELECTRICAL CHARACTERISTICS TO TO TO

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one latch. The other latches are tested in the same manner.

	- wildle	TEST V	OLTAGE VA	LUES	- 3								
	(Volts)												
@ Test emperature	VIH max	V _{IL min}	VIHA min	VILA max	VEE								
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2								
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2								
+85°C	-0.700	-1.625	-1.035	-1.440	-5.2								

										+85°C	-0.700	-1.625	-1.035	-1 440	-5.2	-
			Pin			C10134					TEST VO	LTAGE APPL	LIED TO PINS	LISTED BEL	ow	
			Under	-30	0°C	+2!	5°C	+8!	5°C							(VCC
Characteristic	0 4	Symbol	Test	Min	Max	Min	Max	Min	Max	Unit	VIH max	VIL min	VIHA min	VILA max	VEE	Gnd
Power Supply Drain Current		1E	8	-	60	-	55	-	60	mAdc		- 8	5 - B	-	8	1,16
Input Current	1 1 1	lin H	4 5	-	460 460		290 290	-	290 290	μAdc	4 5	1 9	- 10°	è -	8	1,16
			6	-	425	-	265	-	265		6		2 E - E	-0		
			7	-	460 425	-	290 265	-	290 265		7 10	- 10	4- 4	1		
		lin L	4*	0.5	-	0.5	-	0.3	1-1	μAdc	-8	4	15-8	g	8	1,16
Logic "1" Output Voltage		VOH	2 2	-1.060 -1.060	-0.890 -0.890	-0.960 -0.960	-0.810 -0.810	-0.890 -0.890	-0.700 -0.700	Vdc Vdc	4 5,6	6,7,10, 7,10	\$ AT . 1	9	8 8 .	1,16
Logic "0" Output Voltage		VOL	2 2	-1.890 -1.890	-1.675 -1.675	-1.850 -1.850	-1.650 -1.650	-1.825 -1.825	-1.615 -1.615	Vdc Vdc	6	4,6,7,10, 5,7,10	1.62.5	8 -	8 8	1,16
Logic "1" Threshold Voltage		VOHA	2 2	-1.080 -1.080	-	-0.980 -0.980	-	-0.910 -0.910	-	Vdc Vdc	-0	6,7,10 7,10	4 5	0 - 1	8 8	1,16
Logic "0" Threshold Voltage		VOLA	2 2	-	-1.655 -1.655	3-1	-1.630 -1.630	15	-1.595 -1.595	Vdc Vdc	6	6,7,10 7,10	1 H 1 H	4 5	8 8	1,16
Switching Times (50-ohm load)			helia,	-		40%		12		W 86	+1.11 V	+0.31 V	Pulse In	Pulse Out	-3.2 V	+2.0
Propagation Delay	Data Clock Select	t4+2+ t10-2+ t6+2+	2	1.0 1.0 1.0	3.5 6.0 4.8	1.0 1.0 1.0	3.3 5.7 4.6	1.0 1.0 1.0	3.6 6.3 5.0	ns	4 5	6,7,10 7 7,10	4 10 6	2	8	1,16
Setup Time	Data Select	t _{setup}	2 2	2.5 3.5	_	2.5 3.5	10	2.5 3.5	-	ns ns	5	6,7 7,11	4,10 6,10	2 2	8	1,16
Hold Time	Data Select	thold thold	2 2	1.5	(6F)	1.5	60 -	1.5	-	ns ns .	5	6,7 7,11	4,10 6,10	2 2	8	1,16 1,16
Rise Time (20% to 80%)		t2+	2	1.5	3.7	1.5	3.5	1.5	3.8	ns	- 7	6,7,10	4	2	8	1,16
Fall Time (20% to 80%)		t2-	2	1.5	3.7	1.5	3.5	1.5	3.8	ns	1	6,7,10	4	2	8	1,16

^{*}All other inputs tested in the same manner

DUAL J-K MASTER-SLAVE FLIP-FLOP

The MC10135 is a dual master-slave dc coupled J-K flip-flop. Asynchronous set (S) and reset (R) are provided. The set and reset inputs override the clock.

A common clock is provided with separate \overline{J} - \overline{K} inputs. When the clock is static, the \overline{J} - \overline{K} inputs do not effect the output.

The output states of the flip-flop change on the positive transition of the clock.

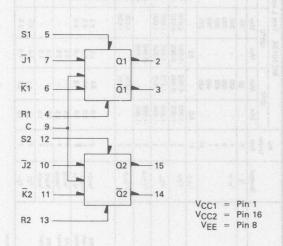
PD = 280 mW typ/pkg (No Load)

fTog = 140 MHz typ

 $t_{pd} = 3.0 \text{ ns typ}$

 t_r , $t_f = 2.5 \text{ ns typ } (20\%-80\%)$

LOGIC DIAGRAM



R-S TRUTH TABLE

R	S	Q _{n+1}
L	L	Qn
L	Н	Q _n
H	L	L
Н	H	N.D.

N.D. = Not Defined

CLOCK J-K TRUTH TABLE*

J	K	Q _{n+1}
L	L	Qn
Н	L	L
L	Н	H
Н	Н	Qn

*Output states change on positive transition of clock for J-K input condition present.

MECL 10K SERIES

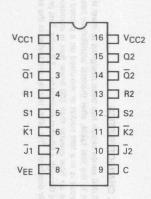
DUAL J-K MASTER-SLAVE FLIP-FLOP



L SUFFIX CERAMIC PACKAGE CASE 620

P SUFFIX PLASTIC PACKAGE CASE 648





ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established in an ambient temperature of 25°C, while the circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs tested in the same manner.

		TEST V	OLTAGE VA	LUES	你
			Vdc ± 1%	17 30	- 34
@ Test Temperature	V _{IH} max	VIL min	VIHA min	VILA max	VEE
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

			Name of the						- 2	+85°C	-0.700	-1.825	-1.035	-1.440	-5.2	1130
	14 14	Pin	al hat	The Life	M	C1013	5 Test Li	imits	100		VOL	TACE ADDLL	ED TO PINS L	ICTED DEL	NA.	
	8 8	Under	-3	0°C		+25°C		+8	5°C	2	VOL	I AGE APPLI	ED TO FINS L	ISTED BELL	JVV.	(Vcc)
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	VIH max	VIL min	VIHA min	VILA max	VEE	Gnd
Power Supply Drain Current	ΙE	8		75	-	54	68	-	75	mAdc		- 1	-	V=	8	1,16
Input Current	lin H	6,7,9,10,11 4,5,12,13	-	425 620	=	-	265 390	-	265 390	μAdc μAdc	1		_	-	8 8	1,16 1,16
Input Leakage Current	lin L	4,5,6,7,9, 10,11,12,13	0.5 0.5	-	0.5 0.5	-	_	0.3		μAdc μAdc		0	-		8	1,16 1,16
Logic "1" Output Voltage	VOH	2 2 3	-1.060 -1.060	-0.890 -0.890	-0.960 -0.960	_	-0.810 -0.810	-0.890 -0.890	-0.700 -0.700	Vdc Vdc	5 6	-	5.5	_	8	1,16 1,16
Logic "0" Output Voltage	VOL	3 3 ③	-1.890 -1.890	-1.675 -1.675	-1.850 -1.850	-	-1.650 -1.650	-1.825 -1.825	-1.615 -1.615	Vdc Vdc	5	5 ± -2	5.51	3-	8	1,16 1,16
Logic "1" Threshold Voltage	VOHA	2 2 4	-1.080 -1.080	=	-0.980 -0.980	_	-	-0.910 -0.910	_	Vdc Vdc	6	3 328	5 -	1 2	8	1,16 1,16
Logic "0" Threshold Voltage	VOLA	3 3 ④	I	-1.655 -1.655	-	_	-1.630 -1.630	-	-1.595 -1.595	Vdc Vdc	6	\$ 8-4 \$ 8-4	5 –	# - # -	8	1,16 1,16
Switching Times Clock Input Propagation Delay Rise Time (20 to 80%)	t9+2+ t9+2- t2+,t3+	2 2 2 2.3	1.8 1.8	5.0 5.0 4.8	1.8 1.8 1.1	3.0 3.0 2.0	4.5	1.8 1.8	4.6 4.6 4.7	ns	1 (19) 4411 1 stud quan 1 stud quan 1 stud quan	onni ribg pertendin pertendin	Pulse In 9 9	Pulse Out 2 2 2 3	-3.2 Vdc	1,16
Fall Time (20 to 80%)	t2-,t3-	2,3	1.1	4.8	1.1	2.0	1	1.1	4.7	*	1326	8 6-2	9	2,3		*
Set Input Propagation Delay	t5+2+ t12+15+ t5+3- t12+14-	2 15 3 14	1.8	5.6	1.8	3.0	5.0	1.8 - - -	5.2	ns	De Esse Chaladeles Sections	e priming	5 12 5 12	2 15 3 14	8	1,16
Reset Input Propagation Delay	t4+2- t4+3+ t13+15- t13+14+	2 3 15 14	1.8	5.6	1.8	3.0	5.0	1.8	5.2	ns	Market to the second of the se	100 mm	4 4 13 13	2 3 15 14	8	1,16
Setup Time	tsetup	7	2.5	-	2.5	1.0	n 6	2.5	-	ns			6,9 ⑤	2	8	1,16
Hold Time	thold	7	1.5	-	1.5	1.0	95	1.5	-	ns	10 B B	8 6-2 6	6,9 ⑤	2	8	1,16
Toggle Frequency	fTog	2	125		125	140	-	125	-	MHz	1 1 2 5	N 4-1 1	90	2	9	1,16

NOTES:

- \bigcirc Individually test each input; apply $V_{IH\ max}$ to pin under test.
- $\ \ \, \bigcirc$ Individually test each input; apply VIL min to pin under test.
- Individually test each input; apply V_{IL} min to pin under test.
 Output level to be measured after a clock pulse has been applied to the C input (pin 9)
- Output level to be measured after a clock pulse has been applied to the C input (pin 9)
 VIHA min
 VILA max
 VILA max
- (5) See Figure 2 for timing test diagram.

UNIVERSAL HEXADECIMAL COUNTER

The MC10136 is a high speed synchronous counter that can count up, count down, preset, or stop count at frequencies exceeding 100 MHz. The flexibility of this device allows the designer to use one basic counter for most applications, and the synchronous count feature makes the MC10136 suitable for either computers or instrumentation.

Three control lines (S1, S2, and Carry In) determine the operation mode of the counter. Lines S1 and S2 determine one of four operations; preset (program), increment (count up), decrement (count down), or hold (stop count). Note that in the preset mode a clock pulse is necessary to load the counter, and the information present on the data inputs (D0, D1, D2, and D3) will be entered into the counter. Carry Out goes low on the terminal count, or when the counter is being preset.

This device is not designed for use with gated clocks. Control is via S1 and S2.

> PD = 625 mW typ/pkg (No Load) fcount = 150 MHz typ $t_{pd} = 3.3 \text{ ns typ (C-Q)}$ 7.0 ns typ (C-Cout)

5.0 ns typ (Cin-Cout)

FUNCTION TABLE

Cin	S1	S2	Operating Mode
φ	L	L	Preset (Program)
L	L	Н	Increment (Count Up)
Н	L	Н	Hold Count
L	Н	L	Decrement (Count Down)
Н	Н	L	Hold Count
φ	Н	Н	Hold (Stop Count)

MECL 10K SERIES

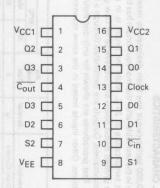
UNIVERSAL HEXADECIMAL COUNTER



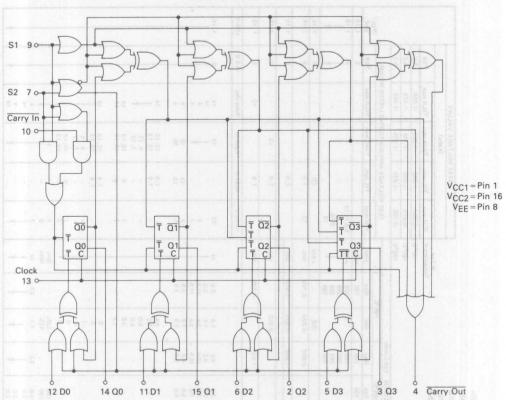
LSUFFIX CERAMIC PACKAGE CASE 620

P SUFFIX PLASTIC PACKAGE CASE 648





LOGIC DIAGRAM



SEQUENTIAL TRUTH TABLE*

			IN	INPUTS									
S1	S2			Carry	Clock **	Q0	Q1	Q2	Q3	Carry			
L	L	L	L	Н	Н	φ	Н	L	L	Н	Н	L	
L	H	φ	φ	φ	φ	L	H	Н	L	Н	H	H	
L	H	φ	φ	φ	φ	L	Н	L	Н	Н	Н	Н	
L	Н	φ	φ	φ	φ	L	Н	Н	Н	Н	Н	L	
L	н	φ	φ	φ	φ	Н	L	Н	Н	Н	Н	Н	
L	H	φ	φ	φ	φ	Н	H	Н	Н	Н	Н	H	
H	H	φ	φ	φ	φ	φ	Н	Н	Н	Н	Н	Н	
L	L	Н	Н	L	L	φ	Н	Н	Н	L	L	L	
Н	L	φ	φ	φ	φ	L	Н	L	Н	L	L	Н	
Н	L	φ	φ	φ	φ	L	Н	Н	L	L	L	Н	
Н	L	φ	φ	φ	φ	L	Н	L	L	L	L	L	
Н	L	φ	φ	φ	φ	L	Н	Н	Н	Н	Н	Н	

 $[\]phi = {\sf Don't}$ care. * Truth table shows logic states assuming inputs vary in sequence shown from top to bottom.

** A clock H is defined as a clock input transition from a low to a

high logic level.

Market 1		TEST	(Volts)	LUES	
@ Test Temperature	VIH max	V _{IL} min	VIHA min	VILA max	VEE
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

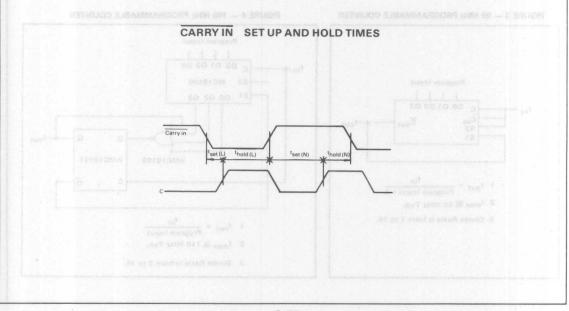
							69				+85°C	-0.700	-1.825	-1.035	-1.440	-5.2	
			Pin				MC10136	Test Limits				TEST	VOLTAGE A	PPLIED TO P	INS LISTED BI	ELOW	1 3 3 4 1
		1 4 五五	Under	-	°C		+25°C	1	+85				T		1	VEE	(Vcc)
Characte		Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	VIH max	V _{IL min}	V _{IHA} min	VILA max		Gnd
Power Supply Drain		1E	8		138	-	100	125	1	138	mAdc	(2) -1	-	-		8	1,16
Input Current		In H	5,6,11,12		350	-	431	220		220	μAdc	5,6,11,12	-		-	8	1,16
		-	9,10		425		- 5	265 245	The Trible	265 245		9.10	-	1 7	1	1 / 1	
		1 10 10	13		390 460		gl o-	290	Jan 1997	290	1	13		-			*
		l _{in L}	All	0.5	400	0.5		200	0.3	230	μAdc		①		1	8	1, 16
Logic "1"	1000		14②	-1.060	-0.890	-0.960	-93	-0.810	-0.890	-0.700	Vdc	12	7.9	-		8	1, 16
Output Voltage		VOH	140	-1.060	-0.890	-0.960	6	-0.810	-0.890	-0.700	Vac	12	7,9			1 1	1,10
Logic "O"	10136	Vol	14②.	-1.890	-1.675	-1.850	11.0	-1.650	-1.825	-1.615	Vdc		7,9		-	8	1, 16
Output Voltage	SE 34 SE S	1	_	E 14-15		-	-	-	-	_				-	Laborator St.		-
Logic "1"		VOHA	14 ②	-1.080	-1-15	-0.980		1	-0.910		Vdc		7,9	12	-	8	1, 16
Threshold Voltage					51.18			1500	29	- 97	TPS	6					
Logic "0" Threshold Voltage	e	VOLA	14②		-1.655		12	-1.630	- 1	-1.595	Vdc	-1-1	7.9	- 1	12	8	1, 16
Switching Times					W 13		50 0-		1			+1.11 V	+0.31 V	Pulse In	Pulse Out	-3.2 V	+2.0 \
(50-ohm Load)		le e z	2	Ja 21					Maria and			-	The second second		9	The same	
Propagation Delay					OIT JE							12		13	14	8	1, 16
	Clock Input	113+14+	14	0.8	4.8	1.0	3.3	4.5 4.5	1.4	5.0	ns	12		13	14	111	1,10
		t13+14-	4	2.0	10.9	2.5	7.0	10.5	2.4	11.5		7			4		
		t13+4-	4	2.0	10.9	2.5	7.0	10.5	2.4	11.5		7	-	1	4	4	(A)
Carry In To Carry C	Out	110 4	43	1.6	7.4	1.6	5.0	6.9	1.9	7.5		7	13	10	4		
	out e	t10+4+	4	1.6	7.4	1.6	5.0	6.9	1.9	7.5	453	7	13	10	4		
Set Up Time							6-17	h	LA PAT			C0		1	-		
3 4 5	Data Inputs	t12+13+	14	3.5		3.5	8	1000	3.5	-		100-1	7,9	12, 13	14		
		t12-13+	14	3.5		3.5	The second second	- 1/	3.5	- 1		-	7,9	12, 13			
	Select Inputs	t9+13+	14	6.0		6.0			6.0			-	-	9,13		1	
E 3 5 8 .	10 0 0 0	t7+13+	14	6.0	1 7 3	1	70.500	-	6.0	* *				7, 13		-	74
120-	Carry In Input	t10-13+	14	2.5		2.5	70	1 -	3.0		la de la constante de la const	7	9	10, 13	14	10-10	- 3
.0.3 2 8		t10+13+	14	1.5		1.5	0		1.5			1	9	10, 13	14		1
Hold Time	Data Inputs		14	0		0	100		0				7.9	12,13	14	land by	8-1
20 3 3 4		t13+12+ t13+12-	14	0		0	and the second	- protect	0		-	-	7,9	12,13	T	- 1	-
	Select Inputs	113+9+	14	- 100		-1.0	111111	The same	-1		11	7061		9.13			
	Select inputs	t13+9+	14	-1		-1.0			-1		10	BL		7,13	100		1
· ·	Carry In Input	t13+10-	14	0		0	- 0	_ =	0		1-1-1	7	9	10, 13	1 4 1 1	0 4 1	
	ourry in Imput	t ₁₃₊₁₀₊	14	0		0	Φ.		0		1	7	- 3	10, 13		5 L	100
Counting Frequency	,		14	125		125	150		125.	12 Defe	MHz	7		13	14	h	
Lounting Frequency		fcountdown	14	125		125	150		125		MHz	9		13			
Rise Time		100000000000000000000000000000000000000	4	0.9	3.3	1.1	2.0	3.3	1.1	3.5	ns	7		0	2 4		2 -
(20% to 80%)		114+	14	0.9	3.3	1	2.0	3.3	1.7	3.5	1 1	ĺ	_		14		107
Fall Time		14-	4				2.0				3				4 0		
(20% to 80%)		114-	14				2.0		1	*	1	1	_	1 1	14	*	V .

1 Individually apply VIL min to pin under test.

To preserve reliable performance, the MC10136 (plastic-packaged device only) is to be operated in ambient temperatures above $70^{\rm O}C$ only when 500 lfpm blown air or equivalent heat sinking is provided.

3 Before test set all Q outputs to a logic high.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C V_{in} V_{CC1} = V_{CC2} = +2.0 Vdc V_{out} 9 Coax Coax sulli cels nore: suprince eldemmorphia bricese A 00 0-0 C 01 0 DO Machine Input Pulse III on t+ = t- = 2.0 ns ± 0.2 ns Clock Input (0-0 (20 to 80%) D2 oresceler up ne the MCS 0 0 +1.11 V TPin TPout S1 Cout 52 +0 31 V - tc+0+ - tc+Q-1 0.1 μF - F 3 MUSCH ¥ 80% Q Output - 50% - 20% - tQ+ VEE = -3.2 Vdc to--+1,11 V C 50% thold H 50-ohm termination to ground located in each scope channel input. Dors 50% All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input t_{setup} L pin and TPout to output pin. Unused outputs are connected to a 50-ohm resistor to ground.



APPLICATIONS INFORMATION

To provide more than four bits of counting capability several MC10136 counters may be cascaded. The Carry In input overrides the clock when the counter is either in the increment mode or the decrement mode of operation. This input allows several devices to be cascaded in a fully synchronous multistage counter as illustrated in Figure 1. The carry is advanced between stages as shown with no external gating. The Carry In of the first device may be left open. The system clock is common to all devices.

The various operational modes of the counter make it useful for a wide variety of applications. If used with MECL III devices, prescalers with input toggle frequencies in excess of 300 MHz are possible. Figure 2 shows such a prescaler using the MC10136 and MC1670. Use of the MC10231 in place of the MC1670 permits 200 MHz operation.

The MC10136 may also be used as a programmable counter. The configuration of Figure 3 requires no additional gates, although maximum frequency is limited to about 50 MHz. The divider modulus is equal to the program input plus one (M = N + 1), therefore, the counter will divide by a modulus varying from 1 to 16.

A second programmable configuration is also illustrated in Figure 4. A pulse swallowing technique is used to speed the counter operation up to 110 MHz typically. The divider modulus for this figure is equal to the program input (M = N). The minimum modulus is 2 because of the pulse swallowing technique, and the modulus may vary from 2 to 15. This programmable configuration requires an additional gate, such as 1/2MC10109 and a flipflop such as 1/2MC10131.

FIGURE 1 — 12 BIT SYNCHRONOUS COUNTER

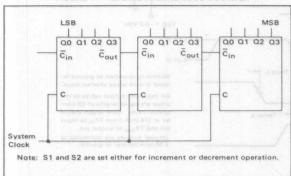


FIGURE 2 - 300 MHz PRESCALER

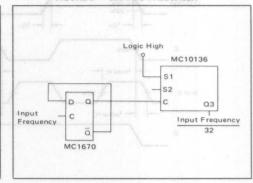


FIGURE 3 — 50 MHz PROGRAMMABLE COUNTER

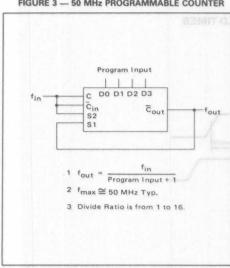
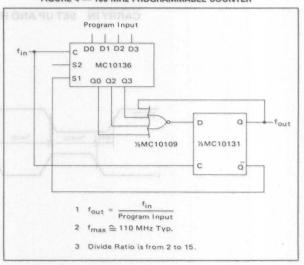


FIGURE 4 — 100 MHz PROGRAMMABLE COUNTER



UNIVERSAL DECADE COUNTER

The MC10137 is a high speed synchronous counter that can count up, down, preset, or stop count at frequencies exceeding 100 MHz. The flexibility of this device allows the designer to use one basic counter for most applications. The synchronous count feature makes the MC10137 suitable for either computers or instrumentation.

Three control lines (S1, S2, and Carry In) determine the operation mode of the counter. Lines S1 and S2 determine one of four operations; preset (program), increment (count up), decrement (count down), or hold (stop count). Note that in the preset mode a clock pulse is necessary to load the counter, and the information present on the data inputs (D0, D1, D2, and D3) will be entered into the counter. Carry Out goes low on the terminal count. The Carry Out on the MC10137 is partially decoded from Q1 and Q2 directly, so in the preset mode the condition of the Carry Out after the Clock's positive excursion will depend on the condition of Q1 and/or Q2. The counter changes state only on the positive going edge of the clock. Any other input may change at any time except during the positive transition of the clock. The sequence for counting out of improper states is as shown in the State Diagrams.

 $\begin{array}{l} P_D = 625 \text{ mW typ/pkg (No Load)} \\ f_{count} = 150 \text{ MHz typ} \\ t_{pd} = 3.3 \text{ ns typ (C-Q)} \\ = 7.0 \text{ ns typ (C-\overline{C}_{out})} \\ = 5.0 \text{ ns typ (\overline{C}_{in}-\overline{C}_{out})} \end{array}$

Preset (Program)

Hold (Stop Count)

Increment (Count Up)

Decrement (Count Down)

L

L

H

H

Н

L

H

MECL 10K SERIES

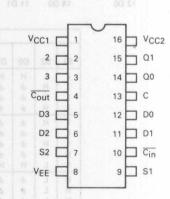
UNIVERSAL DECADE COUNTER

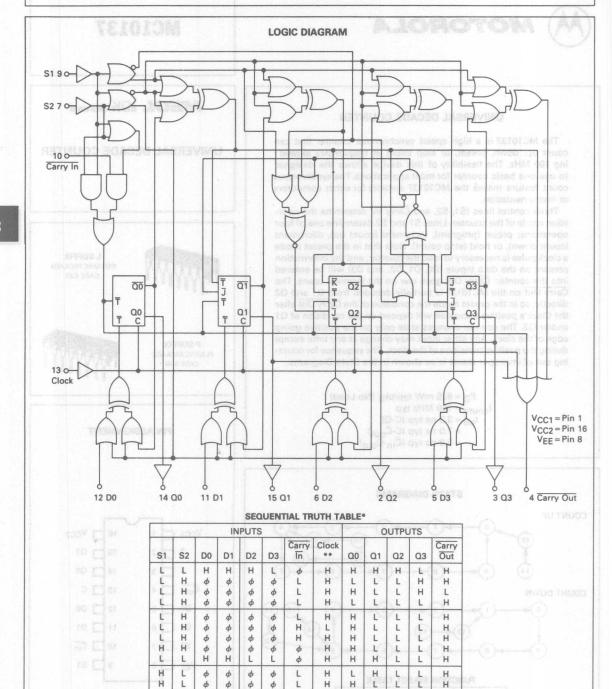


L SUFFIX CERAMIC PACKAGE CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648







 $\phi = Don't care.$

Н

Н

Truth table shows logic states assuming inputs vary in sequence shown from top to bottom.

^{**} A clock H is defined as a clock input transition from a low to a high logic level.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Test Procedures are shown only for selected inputs and outputs. Other inputs and outputs are tested in a similar manner.

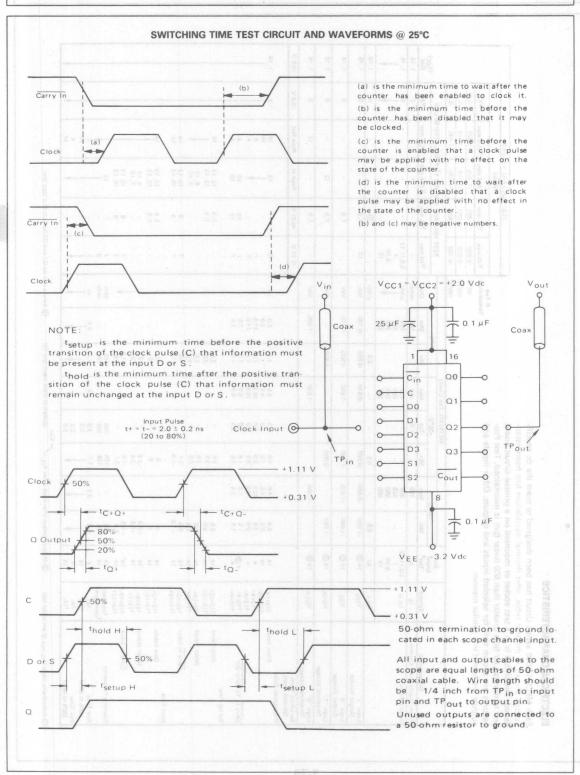
		TEST	OLTAGE VA	LUES	0 B E
		N 1	(Volts)	100	. 8 %
@ Test Temperature	VIH max	VIL min	VIHA min	VILA max	VEE
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

	T	1				MC101271	Test Limits			+85°C	-0.700	-1.825	-1.035	-1.440	-5.2	
		Pin	2	0°C		+25°C	rest Limits	+85	90	N 67	TEST	OLTAGE A	PPLIED TO PI	NS LISTED BE	ELOW	
Characteristic	Symbol	Under	Min	Max	Min	Typ	Max	Min +85	Max	Unit	VIH max	VIL min	VIHA min	VILA max	VEE	(VCC)
Power Supply Drain Current	m le -	8	-	165	F- 5	120	150	1 24	165	mAdc	-	16-21	5- 9	13.4	8	1,16
Input Current	I _{in} H	5,6,11,12 7 9,10 13		350 425 390 460		- - -	220 265 245 290		220 265 245 290	μAdc	5,6,11,12 7 9,10 13	(c) 5/100	ade to	Make He Fig. (1993) Distribution	8	1,16
	lin L	All	0.5	-	0.5	-	-	0.3	-	µAdc ,	-	1	m 9 1	- 4	8	1,16
Logic "1" Output Voltage	VOH	14 ②	-1.060	-0.890	-0.960	9	-0.810	-0.890	-0.700	Vdc	. 12	7,9	2 K- # C	2 t- a	8	1,16
Logic "0" Output Voltage	VOL	14 ②	-1.890	-1.675	-1.85C		-1.650	-1.825	-1.615	Vdc	0,=	7,9	-	-	8	1,16
Logic "1" Threshold Voltage	Vона	14 ②	-1.080	-	-0.980	-		-0.910		Vdc		7.9	12	-	8	1, 16
Logic "0" Threshold Voltage	VOLA	14②	-	-1.655	1		-1.630	-	-1.595	Vdc	1-	7,9	- 1	12	8	1, 16
Switching Times (50-ohm Load)				9	-	(9)	1	6 6		11	+1.11 V	+0.31 V	Pulse In	Pulse Out	-3.2 V	+2.0
Propagation Delay Clock Input Carry In To Carry Out	113+14+ 113+14- 113+4+ 113+4- 110-4- 110+4+	14 14 4 4 4 4 3	0.8 0.8 2.0 2.0 1.6	4.8 4.8 10.9 10.9 7.4 7.4	1.0 1.0 2.5 2.5 1.6	3.3 3.3 7.0 7.0 5.0 5.0	4.5 4.5 10.5 10.5 6.9 6.9	1.1 1.1 2.4 2.4 1.9	5.0 5.0 11.5 11.5 7.5 7.5	ns	12 7 7 7 7	- - 13 13	13 V 10 10	14 14 4 4 4	8	1, 16
Set Up Time Data Inputs Select Inputs	t12+13+ t12-13+ t9+13+	14 14 14	3.5 3.5 7.5		3.5 3.5 7.5 7.5	-	2 10 E	3.5 3.5 7.5				7, 9 7, 9	12, 13 12, 13 9, 13 7, 13	14		
Carry In Input	t7+13+ t10-13+ t13+10+	14 14 14	7.5 4.5 - 1.0		3.7	3 da 8 -8	19 6	7.5 4.5 - 1.0			7 7	9	10, 13	14 14		
Hold Time Data Inputs	t ₁₃₊₁₂₊ t ₁₃₊₁₂₋	14 14	0		0	0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	11	0				7, 9 7, 9	12, 13 12, 13	14		
Select Inputs	t13+9+ t13+7+	14 14	- 2.5 - 2.5		-2.5 -2.5	Ī	80, 91 JOSE	- 2.5 - 2.5		1		-	9, 13 7, 13			
Carry In Input	t13+10- t10+13+	14 14	-1.6 4.0		-1.6 3.1	-	9 0	-1.6 4.0		*	7 7	9	10, 13 10, 13			
Counting Frequency	fcountup fcountdown	14 14	125 125	-	125 125	150 150	3.1	125 125		MHz MHz	7 9	-	13	15		
(20% to 80%)	t4+ t14+	14	0.9	3.3	1.1	2.0 2.0	3.3	1.1	3.5	ns	7	N		4 14		
Fall Time (20% to 80%)	t4- t14-	4 14	-		1	2.0	1			1	1	15	1	4 14		1

① Individually apply VIL min to pin under test.

 $[\]ensuremath{ \bigcirc \!\!\! \bigcirc}$ Measure output after clock pulse $\ensuremath{ \mathrm{V_{IL}}}$ $\ensuremath{ \sqrt{ \ \ ^{\mathrm{V_{IH}}}}}$ appears at clock input (pin 13)

³ Before test set Q1 and Q2 outputs to a logic low.





BI-QUINARY COUNTER

The MC10138 is a four bit counter capable of divide by two, five, or ten functions. It is composed of four set-reset master-slave flip-flops. Clock inputs trigger on the positive going edge of the clock pulse.

Set or reset input override the clock, allowing asynchronous "set" or "clear." Individual set and common reset inputs are provided, as well as complementary outputs for the first and fourth bits.

P_D = 370 mW typ/pkg (No Load)

f_{tog} = 150 MHz typ

 t_r , $t_f = 2.5 \text{ ns typ } (20\%-80\%)$

LOGIC DIAGRAM S1 01 SO QO S2 02 S3 Q3 109 15 9 13 9 49 59 29 S D1 D1 Q D1 0 0 Q D2 D2 Q' Q C1 Q' Q' 12 \bar{a} ā ā ā C2 C2 C2 14 0 C2 V_{CC1} = Pin 1 V_{CC2} = Pin 16 V_{EE} = Pin 8

COUNTER TRUTH TABLES

BI-QUINARY	
(Clock connected to C	2
and O2 connected to C	11

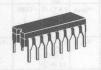
COUNT	Q1	Q2	03	00
			au	- 40
0	L	L	L	L
1	Н	L	1	L
2	L	H	L	L
3	Н	Н	L	L
4	L	L	Н	L
5	L	L	L	H
6	Н	L	L	H
7	L	Н	L	Н
8	Н	н	L	H
9	L	L	H	H

BCD (Clock connected to C1 and Q0 connected to C2)

COUNT	QO	Q1	Q2	03
0	L	L	L	L
1	Н	L	L	L
2 3	L	H	L	L
3	Н	Н	L	L
4	L	L	Н	L
5	Н	L	H	L
6	L	н	Н	L
7	Н	Н	Н	L
8	L	L	L	Н
9	H	L	L	Н

MECL 10K SERIES

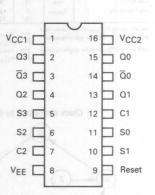
BI-QUINARY COUNTER



L SUFFIX CERAMIC PACKAGE CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648





3

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

		TEST	VOLTAGE	VALUES	
@ Test			(Volts		
Temperature	VIHmax	VILmin	VIHAmin	VILAmax	VEE
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

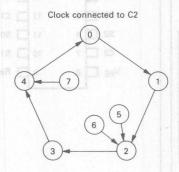
				4.3						+85°C	-0.700	-1.825	-1.035	-1.440	-5.2	
42.000					1	AC10138	Test Lim	ts		YMAL	HUEH	TEST VO	LTAGE A	PPLIED		
		Pin Under	-3	0°C		+25°C		+85	5°C	1341	MANAM	TO PINS	LISTED	BELOW		
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	V _{IHmax}	VILmin	VIHAmin	VILAmax	VEE	(V _{CC} Gnd
Power Supply Drain Current	B I E	8		97		70	88	n in e	97	mAdc	9	1861	8 es 8	EFUI DI	8	1.16
Input Current	I _{in} H	12		350			220	A Section 1	220	N. In	12	no el l	ensit	mult do	114.15	will.
	AU00	5,6,10,11		390		ivale-	245	16857	245	1 10 10	5,6,10,11	72.12		Total Control		545
		7	La Page	460		mit to	290	ming	290		7.3	But a	Bridge :	13013 -		V
		9		6501			410		410	Y	9		-	188	A Volce	
ANT YE LERES	lin L	All	0.5		0.5			0.3	-	μAdc	Late Late	-	and and	terons	8	1,16
Logic "1"	VOH	3,14②		-0.890	-0.960	BEET CHARLE	-0.810	-0.890	-0.700	Vdc	9	-	22	The state of	8	1,16
Output Voltage		2,4,13,15	-1.060	-0.890	-0.960	\$110 BI	-0.810	-0.890	-0.700	Vdc	5,6,10,11	10000	Material III	18910	8	1,16
Logic "O"	1	3,14 ①	-1.890	-1.675	-1.850	THE PERSON	-1.650	-1.825	-1.615	Vdc	5.0.40.44	THE R	17000-01	Timber 2	0	COTAC
Output Voltage	VOL	2,4,13,15		-1.675	-1.850		-1.650	-1.825	-1.615	Vdc	5,6,10,11				8	1,16
Obtput voltage		(2)	-1.030	-1.073	1.000		-1.050	-1.025	-1.015	VOC	3				0	1,16
Logic "1"	VOHA	2,4,13,15	-1.080		-0.980	-		-0.910		Vdc			5,6,10,11	1	8	1.16
Threshold Voltage	UHA	1		111		-						27.7	0,0,		li	1,10
	1974	3,14 ②	-		W		- 410	80 V 01	O pao	C .	MI STE	-	9			V
TOWNSHIP OF THE PERSON	18.3	13,15①					100	,		1			7,12			Y
Logic "0"	VOLA	2,4,13,15	2.33	-1.655		1-11-11	-1.630		-1.595	Vdc	LEAN FACT	- 1	071 -	5,6,10,11	8	1,16
Threshold Voltage		3,14(1)	11/180		12. 2			168	190	S) but	2.5, na	100 1	19	9		
		13,15(2)	181		100		A		-				177	7.12		A
Switching Times (50-ohm Load)													Pulse In	Pulse Out	-3.2 V	+2.0
Propagation Delay	4 5 1				-	-						-				-
Clock Delays		15	1.4	5.0	1.5	3.5	4.8	1.5	5.3	1	14.13	21.01	10		8	10.5
50 \ Loads	t12+15+		1.4	5.0	1.5	3.5	4.8	1.5	5.3	ns			12	15 14	8	1,16
30 11 20003	t7+13+	13		5.2		100	5.0		5.5	BARS	AHU SH	303	7	13		
	17+4+	4		1		0.4	1					-		4		
	17+2+	2		1							-	13 - 13		2		
	t7+3+	3		V		10			A			-/-	A	3		
	t12+15-	15		5.0	10	6.0	4.8	1.60	5.3		10	4.8	12	15	44	
	†12+14-	14		5.0	3.45	188	4.8	1 9	5.3			201	12	14		1
	17+13-	13	-	5.2	1 0	-	5.0.	-	5.5	-	-		7	13		
	t7+4-	4 2									-			4		
	t7+2-	3		V					-		111 1		-	3		
Set Delay	t7+3-	2.00%		5.2		10			100	64 1		2 7	V	The state of the state of	1 21	
Set Delay	t11+15+	15		5.2		189	14		130				11	15		
	t11+14-	14		5.2		10 -	13 -	1	10	0		0.75	11	14		-
					1		V	-	V	1		5	9	15	13	
Reset Delay	t9+14+	14	V	A											1 1 1	
	t9+15-	15	*	V	V	2.5	Post 1 100 11 11	1.1	E 0		- C 18	0.	11	14	la 1	
Rise Time	t9+15- t14+	15 14	1.1	4.7	1.1	2.5	4.5	1.1	5.0	ns		8	11	14	8.1	
Rise Time (20% to 80%)	t9+15- t14+ t15+	15 14 15	1.1	4.7	1.1 1.1	2.5	Post 1 100 11 11	1.1	5.0 5.0	ns		2	11	15		
Rise Time (20% to 80%) Fall Time	t9+15- t14+ t15+ t14-	15 14 15 14				2.5	4.5			ns		2	11 9	15 14	8	2
Rise Time (20% to 80%)	t9+15- t14+ t15+	15 14 15	1.1			2.5	4.5	1.1	5.0	ns W	-	2	11	15		

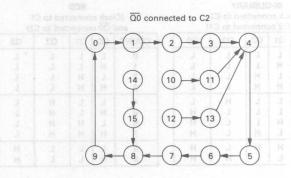
*Individually apply V_{ILmin} to pin under test.

① Set all four flip-flops by applying pulse

V_{ILmin}
V_{IHmax} to pins 5,6,10,11 prior to applying test voltage indicated.
V_{ILmin}
V_{IHmax} to pin 9 prior to applying test voltage indicated.

COUNTER STATE DIAGRAM — POSITIVE LOGIC



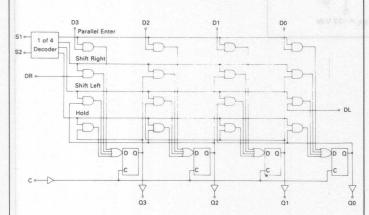


FOUR-BIT UNIVERSAL SHIFT REGISTER

The MC10141 is a four-bit universal shift register which performs shift left, or shift right, serial/parallel in, and serial/parallel out operations with no external gating. Inputs S1 and S2 control the four possible operations of the register without external gating of the clock. The flip-flops shift information on the positive edge of the clock. The four operations are stop shift, shift left, shift right, and parallel entry of data. The other six inputs are all data type inputs; four for parallel entry data, and one for shifting in from the left (DL) and one for shifting in from the right (DR).

> P_D = 425 mW typ/pkg (No Load) fShift = 200 MHz typ $t_r t_f = 2.0 \text{ ns typ } (20\%-80\%)$

LOGIC DIAGRAM



V_{CC1} = Pin 1 V_{CC2} = Pin 16 VEE = Pin 8

TRUTH TABLE

SEL	ECT			OUT	PUTS	
S1	S2	OPERATING MODE	Q0 _{n+1}	Q1 _{n+1}	Q2 _{n+1}	Q3 _{n+1}
L	L	Parallel Entry	D0	D1	D2	D3
L	Н	Shift Right*	Q1 _n	Q2 _n	Q3 _n	DR
Н	L	Shift Left*	DL	Q0 _n	Q1 _n	Q2 _n
Н	Н	Stop Shift	Q0 _n	Q1 _n	Q2 _n	Q3 _n

*Outputs as exist after pulse appears at "C" input with input conditions as shown. (Pulse = Positive transition of clock input).

MC10141

MECL 10K SERIES

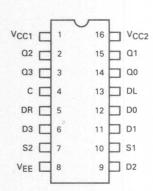
FOUR-BIT UNIVERSAL SHIFT REGISTER

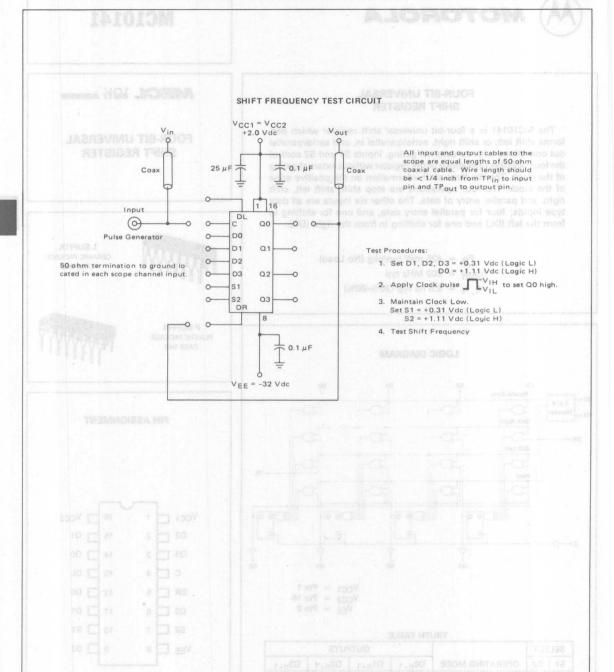


L SUFFIX. CERAMIC PACKAGE CASE 620

P SUFFIX PLASTIC PACKAGE **CASE 648**



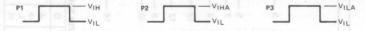




Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established in an ambient temperature of 25°C, while the circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs tested in the same manner.

	-				
		TEST	VOLTAGE	VALUES	
		Photo.	(Volts)		122
@ Test Temperature	VIH max	VIL min	VIHA min	VILA max	VEE
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

										+85-C	-0.700	-1.825	-1.035	-1.440	-5.2			9	
		Pin			MC	10141	Test Lin	nits		5	TEST VO	I TAGE A	PRI IED TO	PINS LISTED	BELOW:				
		Under	-30	o°C		+25°C		+8	5°C		TEST VC	TAGEA	THE TO	TINS LISTED	BELOW.				(VC
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	VIH max	VIL min	VIHA min	VILA max	VEE	P1	P2	P3	Gn
Power Supply Drain Current	1E	8	-	112	-	82	102	-	112	mAdc	-		-	-	8	-	-	-	1,1
Input Current	lin H	5	-	350	-	-	220	-	220	μAdc	5		-	-	8	-		-	1,1
	1	6	-	350	-	-	220	-	220		6		-	-	1	-	-	-	1
		7	-	390	-	-	245	-	245		7	-	-	-	1	-	-	-	
	-	4	-	425	-	_	265	-	265		4	-	-	0 15 -5 10	40 VT 5		-		
	lin L	12	0.5	-	0.5	-	-	0.3	-	μAdc	4,5,6,7,9, 10,11,13	12	-	日日日日	8	-	-	-	1,1
Logic "1" Output Voltage	Vон	3	-1.060	-0.890	-0.960	_	-0.810	-0.890	-0.700	Vdc	6	-	_	1838	8	4	-	-	1,1
Logic "0" Output Voltage	VOL	3	-1.890	-1.675	-1.850	_	-1.650	-1.825	-1.615	Vdc		- 8	-	2 日 2 日	8	4	_		1,1
Logic "1"	VOHA	3	-1.080	-8	-0.980	_	-	-0.910		Vdc	-	- 2	6	A WAR E	8	4	-	-3	1,1
Threshold Voltage	1	NI	1	-/	17	X		1	-	1	6	(4)	- 9	7	E 13	4	-	-	
	0			4		-			-		6	4	_ 0	6-0 3		-	4	-	
				-		-	-		-		- 8	-	- 9	7 00 -6 00	D 12	-	-	4	1
Logic "O"	VOLA	3	-	-1.655	-8	11 -	-1.630	-	-1.595	Vdc	-	= 0	- 67	6	8	4	-	- 1	1,1
Threshold Voltage	①		-			-	140	-			-	(5)	- 27	7	- 10 3	4	-	-	1
			or Trees		-	-		+			- 1	(5)	- 1	R 2-1 5	0		4	-	
16		N.	-	No.		-		-		4	6	- 8	- 8	B	S 4	-	-	4	
Switching Times (50 \Omega Load)	in the second		-		-	4	(0)		1000	100	1	70.0	100	10000			50		+2.0
Propagation Delay	t4+3+	3	1.7	3.9	1.8	2.9	3.8	2.0	4.2	ns	2		- 6	2 5-6 2	-3.2 V	-	-	-	_
Setup Time (tsetup)	t12+4+	14	2.5		2.5	-	_	2.5	_	1	- 5	1 -	- 5	医男子 加	8	-	0 -	-	1,1
	t10+4+	14	5.5	1	5.0	-	62	5.5	-		- 8	32 9	_ =====================================	9-5		-	D-	-	
Hold Time (thold)	t4+12+	14	1.5	1	1.5	-	-	1.5	-	77	- 1	12 00	- 5	1. 图 题 商	3 10 0	-	-	- 1	
Rise Time (20% to 80%)	t3+	3	1.0	3.4	1.1	2.0	3.3	1.1	3.6		2	- 1	- 10	S 20 -2 3	3 5 5	-	0 -	-	
Fall Time (20% to 80%)	t3-	3	1.0	3.4	1.1	2.0	3.3	1.1	3.6		2	-	- 5	B 17 14 B	5 8	-	-	-	
Shift Frequency	fShift	- 3	150	- 1	150	200	-	150	-	MHz	@@	8-9	- 6	2 2 4 2	(b) V (c)	-	-	-	1



These tests to be performed in sequence as shown.
 See switching time test circuit for test procedures.
 See shift frequency test circuit for test procedures.
 Reset to zero before performing test.
 Reset to one before performing test.



QUAD LATCH

The MC10153 is a high speed, low power, MECL quad latch consisting of four bistable latch circuits with D type inputs and gated Qoutputs. Open emitters allow a large number of outputs to be wire-ORed together. Latch outputs are gated, allowing direct wiring to a bus. When the clock is low, outputs will follow D inputs. Information is latched on positive going transition of the clock. The MC10153 provides the same logic function as the MC10133, except for inversion of the clock.

PD = 310 mW typ/pkg (No Load)

 $t_{pd} = 4.0 \text{ ns typ}$

 t_r , $t_f = 2.0 \text{ ns typ } (20\%-80\%)$

MECL 10K SERIES

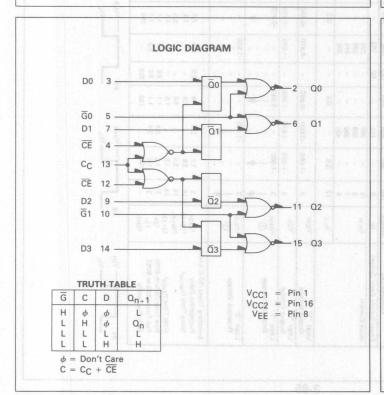
QUAD LATCH

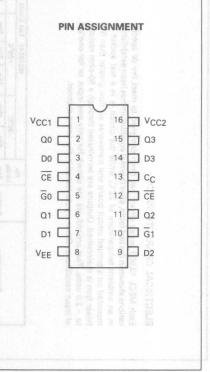


LSUFFIX CERAMIC PACKAGE CASE 620

P SUFFIX PLASTIC PACKAGE CASE 648







ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to $-2.0\ volts$. Test procedures are shown for only selected inputs and outputs. Other inputs and outputs are tested in a similar manner.

	W.	TEST	OLTAGE VA	LUES	49.7
		P	(Volts)		257
@ Test Temperature	VIH max	V _{IL min}	VIHA min	VILA max	VEE
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

	1 1/2 (2)	130 60	1 20 -		200	240452	Test Limit		10 5 70	T00 C	-0.700	-1.025	-1.035	-1.440	-3.2	
9 0	(n cn	Pin		оос	IVI	+25°C	Test Limit	1	5°C		TEST	OLTAGE A	PPLIED TO F	INS LISTED	BELOW:	
Characteristic	Symbol	Under	Min	Max	Min	Typ	Max	Min	Max	Unit	VIH max	VIL min	VIHA min	VILA max	VEE	(VCC) Gnd
Power Supply Drain Current	1 _E	8	-	83	-	-	75	-	83	mAdc		13	-		8	1,16
Input Current	linH	3	-	390	-	_	245	_	245	μAdc	3	-	-		8	1,16
		4	-	390	-	_	245	-	245		4	-	-	-		1
	-	5	-	560 460		-	350 290	-5	350 290		5 13	-		=		
	1	3	0.5	460	0.5	- 10	290	0.3	290	μAdc	- 13	3	_		8	1.16
Logic "1"	linL	-	-				-				-				-	-
Output Voltage	VOH	2	-1.060 -1.060	-0.890 -0.890	-0.960 -0.960	- 10	-0.810	-0.890 -0.890	-0.700 -0.700	Vdc Vdc	3 3	4 13	9T8 9	18 . 19	8	1,16 1,16
Cotput voitage	TATE	2	-1.000	-0.030	-0.300		-0.610	-0.830	-0.700	Vac	3	13	700	計畫手	0	1,10
Logic "0"	VOL	2	-1.890	-1.675	-1.850	10	-1.650	-1.825	-1.615	Vdc	-	3,13	1 1 1 1 1 m	W 15-9	8	1,16
Output Voltage	1 1 2 2	2		1		-	1	1	1		3,5	13	5-11 5	F 2-2		1
		2		V	V	-	V		V	V	-	3,4	5-2 3	25 943	1	
Logic "1"	VOHA	2	-1.080	- 7	-0.980	-	-	-0.910	-	Vdc	3	4	B E-2 S	5 5	8	1,16
Threshold Voltage	=	2 2		- T-1		-			-		3	4 4	3	B 9-8		100 P
		21							I I		3	3 4	# 8 2 9	W W_0		
		2††	1 13	- 1	0	-0.3	-		- 3		0.93	5-	8 3-5 8	13 d_8 -		
	1- 1- 1- 1-	2††	W 2	-		17	-	2 10	-		- h	5-	6 E-0 a	0-6-6	20	
	La La Sala	2		-					-52		3	E 65-	2 1-6 2	4		
		2	18	-			-		-12	V		1 2 7	E 2711 a	13	32 V 1	,
Logic "0" Threshold Voltage	VOLA	2 2	P -	-1.655			-1.630	-53	-1.595	Vdc	3	4	5	3	8	1,16
Threshold voltage	10 14 14	2	I I			Ξ	-	5			5 70	4	W 978-8	3	8 - 1	19.73
	S to by 14	2†			_	_					-	-	B 8_3 6	0.0	-6	
		2††	-		-		m				3	-	B 6-R 6	3-6-7		
		2††	-	V		-			Y		3	-	S C- 15	13		V
Switching Times (50 Ω Load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t3+2+	2	1.0	5.6	1.0	4.0	5.4	1.1	5.9	ns	4	- 6-	3	2	8	1,16
	t4-2+	2	1.0	5.6	1.0	4.0	5.6	1.2	6.2		3 *	-	4 4	2		
	t5-2+	2	1.0	3.2	1.0	2.0	3.1	1.0	3.4	M- 1	-	-	5	2		
	^t Setup ^t Hold	3	2.5	E	2.5 1.5	0.7	-	2.5	-			_	3	2 2		
Rise Time (20% to 80%)	t ₂₊	2	1.0	3.6	1.1	2.0	3.5	1.1	3.8	1 4	_		3	2	1	
Fall Time (20% to 80%)	t ₂ _	2	1.0	3.6	1.1	2.0	3.5	1.1	3.8			_	3	2		
	2-			-10			0.0	440	5.0		1			10 KB 10	,	

[†]Output level to be measured after a clock pulse has been applied to the clock input (Pin 4).

VIH max

^{*}Latch set to zero state before test.

^{††}Data input at proper high/low level while clock pulse is low so that device latches at proper high/low level for test. Levels are measured after device has latched.

3

BINARY COUNTER

The MC10154 is a four-bit counter capable of divide-by-two, divide-by-four, divide-by-eight or a divide-by-sixteen function.

Clock inputs trigger on the positive going edge of the clock pulse. Set and Reset inputs override the clock, allowing asynchronous "set" or "clear." Individual Set and common Reset inputs are provided, as well as complementary outputs for the first and fourth bits. True outputs are available at all bits.

> PD = 370 mW typ./pkg. (No Load)

tpd

= 150 m Hz (typ.) ftoggle = 3.5 ns typ. (C to Q_0) = 11 ns typ. (C to Q₃) tpd

MECL 10K SERIES

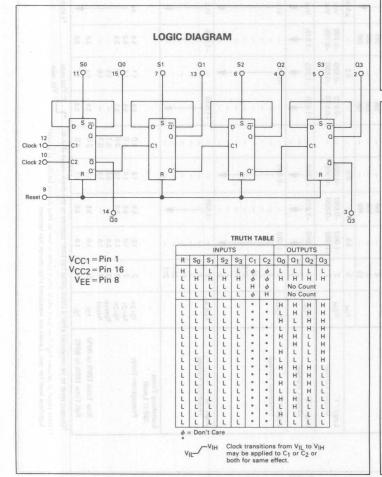
BINARY COUNTER



L SUFFIX CERAMIC PACKAGE CASE 620

P SUFFIX PLASTIC PACKAGE CASE 648





VCC1 [1	16	□ V _{CC2}
O3 [2 8	15	□ 00
<u>03</u> [<u> </u>
Q2 [4	14	1 01
S3 [15	12	Clock 1
S2 [6 7	12	□ S0
S1 [7	10	Clock 2
VEE [8	9	Reset
	18	1 1 8	

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only selected inputs and outputs. Other inputs and outputs tested in the same manner.

		TEST V	OLTAGE	/ALUES	
			(Volts)	1 1/2	13
@ Test Temperature	VIHmax	VILmin	VIHAmin	VILAmax	VEE
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

										+85-C	-0.700	-1.825	-1.035	-1.440	-5.2	
		Pin	-	o°C	ANC	+25°C	fest Limit		5°C	1	-		LTAGE AF	PPLIED TO)	
		Under								1	1					(VCC)
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	VIHmax	VILmin	VIHAmin	VILAmax	VEE	Gnd
Power Supply Drain Current	1E	8	-13	97	-		88		97	mAdc	9	-	-	5 2 5	8	1,16
Input Current	linH	12 11 9	=	390 350 650		=	245 220 410	-	245 220 410	μAdc μAdc μAdc	12 11 9	_	-	of a to	8 8 8	1,16 1,16 1,16
	linL		0.5	-	0.5	-	-0	0.3	-	μAdc	-			5 - 5	8	1,16
Logic "1" Output Voltage	Voн	14 15	-1.060 -1.060	-0.890 -0.890	-0.960 -0.960	-	-0.810 -0.810	-0.890 -0.890	-0.700 -0.700	Vdc Vdc	9	- 8	- 5	841	8	1,16 1,16
Logic "0" Output Voltage	VOL	14 15	-1.890 -1.890	-1.675 -1.675	-1.850 -1.850	=	-1.650 -1.650	-1.825 -1.825	-1.615 -1.615	Vdc Vdc	11 9	100	- 8	THE RESIDENCE OF THE PERSON OF	8	1,16 1,16
Logic "1" Threshold Voltage	VOHA	3 14 15	-1.080 -1.080 -1.080	-	-0.980 -0.980 -0.980		Ī	-0.910 -0.910 -0.910		Vdc Vdc Vdc		2 to 100	5 11 9	050 101 B	8 8 8	1,16 1,16 1,16
Logic "0" Threshold Voltage	VOLA	3 14 15	d	-1.655 -1.655 -1.655	17	-	-1.630 -1.630 -1.630	7=	-1.595 -1.595 -1.595	Vdc Vdc Vdc	1 2	2 4 4 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8	- 016	5 11 9	8 8 8	1,16 1,16 1,16
Switching Times	TIT	TT	TT	1	TX		KTT	T		5 1	1 8	889	Pulse In	Pulse Out	-3.2 Vdc	+2.0 Vd
Clock Input Propagation Delay	t12+15+ t12-13- t12+4- t12-3+	15 13 4 3	1.4 1.9 2.9 3.9	5.0 9.4 12.3 14.9	1.5 2.0 3.0 4.0	3.5 6.0 8.5 11	4.8 9.2 12 14.5	1.5 2.0 3.0 4.0	5.3 9.8 12.8 15.5	ns	73	200	12	15 13 4 3	8	1,16
Rise Time (20 to 80%)	t15+	15	1.1	4.7	1.1	2.5	4.5	1.1	5.0		===	12-8	1	15		
Fall Time (20 to 80%)	t15-	15	1.1	4.7	1.1	2.5	4.5	1.1	5.0		45	-	- 50	15	- 5	
Set Input	t11-15+	15	1.4	5.2	1.5	-	5.0	1.5	5.5	ns	-	-	11 0	15	8	1,16
Reset Input	t9-15+	15	1.4	5.2	1.5	-	5.0	1.5	5.5	ns	11 -	-	9	15	8	1,16
Counting Frequency	fcount	15	125	_0	125	150	0 - 8	125	E -	MHz	-	-	12	15	8	1,16

^{*}Individually test each input applying VIL to input under test.

MECL 10K SERIES

QUAD 2-INPUT MULTIPLEXER

(NON-INVERTING)

QUAD 2-INPUT MULTIPLEXER (NON-INVERTING)

The MC10158 is a quad two channel multiplexer. A common select input determines which data inputs are enabled. A high (H) level enables data inputs D00, D10, D20, and D30 and a low (L) level enables data inputs D01, D11, D21, and D31.

 $P_D = 197 \text{ mW typ/pkg (No Load)}$

t_{pd} = 2.5 ns typ (Data to Q) 3.2 ns typ (Select to Q)

 t_r , $t_f = 2.5 \text{ ns typ } (20\%-80\%)$

3



LSUFFIX CERAMIC PACKAGE CASE 620

P SUFFIX PLASTIC PACKAGE CASE 648



LOGIC DIAGRAM Select 9 -D00 6 -D21 12 D20 13 D31 10 14 Q3 D30 11 TRUTH TABLE VCC = Pin 16 Select DO D1 0 VEE = Pin 8 φ L L φ H H Н L L φ Н Н φ H $\phi = Don't care$

Q0	П	1	16		VCC
Q1			15	b	Q2
D11		3	14		Q3
D10		4	13	\vdash	D20
D01		5	12		D21
D00			11		D30
NC	口		10		D31
VEE		8	9	3	Select

3-91

233		TEST V	OLTAGE VAL	LUES	
@ Test	Service No.		(Volts)	100	
Temperature	VIH max	VIL min	VIHA min	VILA max	VEE
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

						-5.				+85°C	-0.700	-1.825	-1.035	-1.440	-5.2	
		Pin			MC	10158	TEST LIM	ITS .			TEST	OL TACE ADD	LIED TO BIA	IS LISTED BI	EL OW.	
		Under	-3	0°C		+25°C		+8	5°C		I EST VI	JL TAGE APP	LIED TO PIN	IS LISTED BI	ELOW:	(VCC)
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	VIH max	VIL min	VIHA min	VILA max	VEE	Gnd
Power Supply Drain Current	1E	8	-	53		38	48	-	53	mAdc		-			8	16
Input Current	linH	9 5	-	360 400	-	12	225 250	- 8	225 250	μAdc μAdc	9 5	-		12 1 1	8	16 16
1.1	linL	5	0.5	7	0.5		-	0.3	-	μAdc	14	5	- 0.5		8	16
Logic "1" Output Voltage	VOH	1	-1.060	-0.890	-0.960	皮	-0.810	-0.890	-0.700	Vdc	5	5_E	- 1	2 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	8	16
Logic "0" Output Voltage	VOL	1	-1.890	-1.675	-1.850	(=)	-1.650	-1.825	-1.615	Vdc	Ha	2 5 3	- Land	1 10 10 10 10 10 10 10 10 10 10 10 10 10	8	16
Logic "1" Threshold Voltage	VOHA	1	-1.080	J.	-0.980	FE		-0.910	- 1	Vdc	113	2 1- 1	5	913	8	16
Logic "0" Threshold Voltage	VOLA	1	7	-1.655	1:0	17	-1.630	1	-1.595	Vdc	l Te	555	10.00	5	8	16
Switching Times (50 Ω Load)	TT I	ET.	10.7	W	E	7 8		m	7	ns	+1.11 Vdc	+0.31 Vdc	Pulse In	Pulse Out	-3.2 Vdc	+2.0 Vdc
Propagation Delay Data Input	†5-1-	1	1.3	3.1	1.2	2.5	3.0	1.3	3.2			868	5	1	8	16
Select Input	t9+1+	1	2.5	4.8	2.4	3.2	4.5	2.5	4.8		6	2_4	9	1 1	13	
Rise Time (20% to 80%)	t ₁₊	1	1.6	3.4	1.5	2.5	3.3	1.6	3.4		112	된-다	5	1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		
Fall Time (20% to 80%)	t ₁₋	1	1.6	3.4	1.5	2.5	3.3	1.6	3.4		-		5	100	5	1

3

QUAD 2-INPUT MULTIPLEXER (INVERTING)

The MC10159 is a quad two channel multiplexer with enable. It incorporates common enable and common data select inputs. The select input determines which data inputs are enabled. A high (H) level enables data inputs D00, D10, D20, and D30. A low (L) level enables data inputs D01, D11, D21, and D31. Any change on the data inputs will be reflected at the outputs while the enable is low. Input levels are inverted at the output.

PD = 218 mW typ/pkg (No Load)

tpd = 2.5 ns typ (Data to Q) 3.2 ns typ (Select to Q)

 t_r , $t_f = 2.5 \text{ ns typ } (20\%-80\%)$

MECL 10K SERIES

QUAD 2-INPUT MULTIPLEXER (INVERTING)



L SUFFIX CERAMIC PACKAGE CASE 620

P SUFFIX PLASTIC PACKAGE CASE 648



LOGIC DIAGRAM Select 9 D00 6 D113 2 01 D10 4 Enable 7 D21 12 D20 13 D31 10 D30 11 -TRUTH TABLE VCC = Pin 16 Enable Select D0 D1 Q VEE = Pin 8 L L φ Н L L φ H L L H L φ H Н L Н H φ φ φ

 $\phi = Don't Care$

PIN ASSIGNMENT QO 16 VCC Q2 D11 3 14 Q3 D10 13 D20 D01 12 D21 D00 11 D30 Enable 10 D31 9 Select VEE [

5 8	200	TEST V	OLTAGE VAI	LUES	1654
@ Test			(Volts)		
Temperature	VIH max	VIL min	VIHA min	VILA max	VEE
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

		Pin			М	C10159	Test Limi	ts			. TECT 1/	OL TACE ADD	LIED TO BIA	IC LICTED BI	EL OW.	
		Under	-3	0°C		+25°C		+8	5°C		TEST VI	ULTAGE APP	LIED TO PIN	IS LISTED BI	ELOW.	(Vcc)
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	V _{IH} max	VIL min	VIHA min	VILA max	VEE	Gnd
Power Supply Drain Current	ΙE	8		58	-	42	53	It	58	mAdc			atuo	09 09	8	16
Input Current	linH	9 5		360 400	-	=	225 250		225 250	μAdc μAdc	9 5	=	11.0	2 - 和	8	16 16
	linL	5	0.5		0.5		-	0.3	-	μAdc	-	5	张 是 报 3	0 - 52	8	16
Logic "1" Output Voltage	Voн	1	-1.060	-0.890	-0.960	-	-0.810	-0.890	-0.700	Vdc	-	-	华夏 1	8-8	8	16
Logic "0" Output Voltage	VOL	1	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615	Vdc	5	2	100	M - M	8	16
Logic "1" Threshold Voltage	VOHA	1/	-1.080	- /	-0.980	-		-0.910	-	Vdc	9	1	253	6	8	16
Logic "0" Threshold Voltage	VOLA	1	-	-1.655	4-	-	-1.630		-1.595	Vdc	9 9	auth	6	o gy	8	16
Switching Times (50 Ω Load) Propagation Delay Data Input Select Input Enable Input Rise Time (20% to 80%) Fall Time	t5 + 1- t9 + 1- t7+1- t1+	1 1 1 1 1	1.1 1.5 1.4 1.0	3.8 5.3 5.3 3.7	1.2 1.5 1.5 1.1	2.5 3.2 2.5 2.5	3.3 5.0 5.0 3.5	1.1 1.5 1.4 1.0	3.8 5.3 5.3 3.7	ns	+1.11 Vdc	+0.31 Vdc	Pulse In 5 9 7 5 5	Pulse Out	-3.2 Vdc	16
(20% to 80%)	t1_	1	1.0	3.7	1.1	2.5	3.5	1.0	3.7		9	_	9 9	- 8 - 7		1

MOTOROLA

12-BIT PARITY GENERATOR-CHECKER

The MC10160 consists of nine EXCLUSIVE-OR gates in a single package, internally connected to provide odd parity checking or generation. Output goes high when an odd number of inputs are high. Unconnected inputs are pulled to low logic levels allowing parity detection and generation for less than 12 bits.

 $P_D = 320 \text{ mW typ/pkg (No Load)}$

 $t_{pd} = 5.0 \text{ ns typ}$

 t_r , $t_f = 2.0 \text{ ns typ } (20\%-80\%)$

MECL 10K SERIES

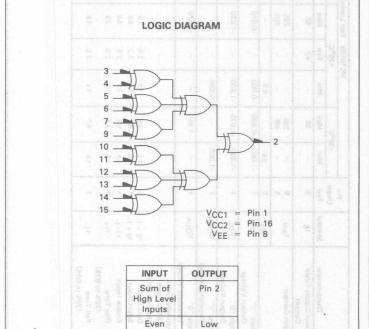
12-BIT PARITY **GENERATOR-CHECKER**



L SUFFIX CERAMIC PACKAGE CASE 620

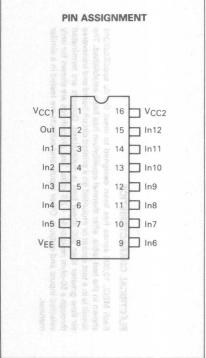
P SUFFIX PLASTIC PACKAGE CASE 648





Odd

High



ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for one set of conditions. Complete testing according to truth table.

	100	TEST VOI	LTAGE VALUI	ES	negt.	
@ Test	6292	>-50 ·	(Volts)		- (3	
Temperature	VIHmax	VILmin	VIHAmin	VILAmax	VEE	
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2	
+25°C	-0.810	-1.850	-1.105 `	-1.475	-5.2	
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2	

Pin	LISTED BELO	ow:	
Under -30°C +25°C +85°C	LISTED BELL	JVV:	
Characteristic Symbol Test Min Max Min Typ Max Min Max Unit VIHmax VILmin VIHAmin			(VC
	VILAmax	VEE	Gn
Power Supply Drain I _E 8 - 86 - 62 78 - 86 mAdc 4,5,9,10,13,14 Current	-	8	1,16
Input Current InH* 3 - 425 265 - 265 µAdc 3 350 220 - 220 µAdc 4	X 14 8	8 8	1,10
I _{inL} 3 0.5 - 0.5 0.3 - μAdc - 3 -	10 4 8	8	1,16
Logic "1" VOH 2 -1.060 -0.890 -0.9600.810 -0.890 -0.700 Vdc 3 4.5,6,7,9,10, -11,12,13,14,15	100	8	1,16
Logic "0" Output Voltage 2 -1.890 -1.675 -1.8501.650 -1.825 -1.615 Vdc - 3,4,5,6,7,9,10, -1,1,12,13,14,15	X 60 10 10 10 10 10 10 10 10 10 10 10 10 10	8	1,16
Logic "1" VOHA 2 -1.0800.9800.910 - Vdc - 4,5,6,7,9,10,11, 3 12,13,14,15		8	1,10
Logic "O" Threshold Voltage 21.6551.6301.595 Vdc - 3,5,6,7,9,10,11 - 12,13,14,15	4	8	1,16
Switching Times (50 Ω Load)	2335		2.8
Propagation Delay +1,11 V Pulse In	Pulse Out	-3.2 V	+2.0
t ₃₊₂₊ 2 1.8 8.1 2.0 5.0 7.5 2.0 8.0 ns 3 5 t ₃₊₂₊ t ₃₊₂₋	2	8	1,16
13-2+	E BE B	18 18	
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	10 mm	0 0	III S
14-2- 14-2+ 3 - 3 -	2 6 E	0 1	186
Rise Time (20% to 80%) 12+ 1.1 3.5 1.1 2.0 3.3 1.0 3.5 3.3	STATES OF THE PARTY OF THE PART		N Gill
Fall Time (20% to 80%) t2_ 1.1 3.5 1.1 2.0 3.3 1.0 3.5 V 3			

*Pins 3, 6, 7, 11, 12, 15 are similar Pins 4, 5, 9, 10, 13, 14 are similar

BINARY TO 1-8 DECODER (LOW)

The MC10161 is designed to decode a three bit input word to a one of eight line output. The selected output will be low while all other outputs will be high. The enable inputs, when either or both are high, force all outputs high.

The MC10161 is a true parallel decoder. No series gating is used internally, eliminating unequal delay times found in other decoders. This design provides the identical 4 ns delay from any address or enable input to any output.

A complete mux/demux operation on 16 bits for data distribution is illustrated in Figure 1. This system, using the MC10136 control counters, has the capability of incrementing, decrementing or holding data channels. When both S0 and S1 are low, the index counters reset, thus initializing both the mux and demux units. The four binary outputs of the counter are buffered by the MC10101s to send twisted-pair select data to the multiplexer/demultiplexer units.

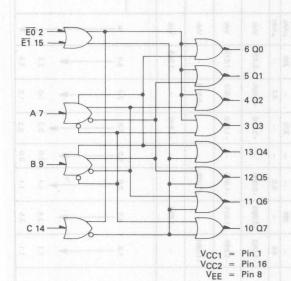
P_D = 315 mW typ/pkg (No Load)

 $t_{pd} = 4.0 \text{ ns type}$

3

 $t_r, t_f = 2.0 \text{ ns typ } (20\%-80\%)$

LOGIC DIAGRAM



TRUTH TABLE

	BLE	IN	PU'	TS	OUTPUTS												
E1	ĒΘ	С	В	A	QO	Q1	Q2	Q3	Q4	Q5	Q6	Q7					
L	L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н					
L	L	L	L	Н	· H	L	Н	Н	H	Н	Н	Н					
L	L	L	Н	L	Н	Н	L	Н	Н	Н	Н	Н					
L	L	L	Н	Н	Н	H	Н	L	H	Н	Н	H					
L	L	H	L	L	Н	Н	Н	H	L	Н	Н	Н					
L	L	Н	L	Н	Н	H	Н	Н	Н	L	Н	H					
L	L	Н	Н	L	H	H	Н	н	Н	Н	L	H					
L	L	Н	Н	Н	Н	Н	Н	H	Н	Н	Н	L					
H	φ	φ	φ	φ	Н	Н	H	Н	Н	Н	Н	Н					
φ	H	φ	φ	φ	Н	Н	Н	Н	Н	Н	Н	Н					

MC10161

MECL 10K SERIES

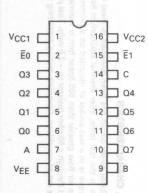
BINARY TO 1–8 DECODER (LOW)



L SUFFIX CERAMIC PACKAGE CASE 620

P SUFFIX PLASTIC PACKAGE CASE 648

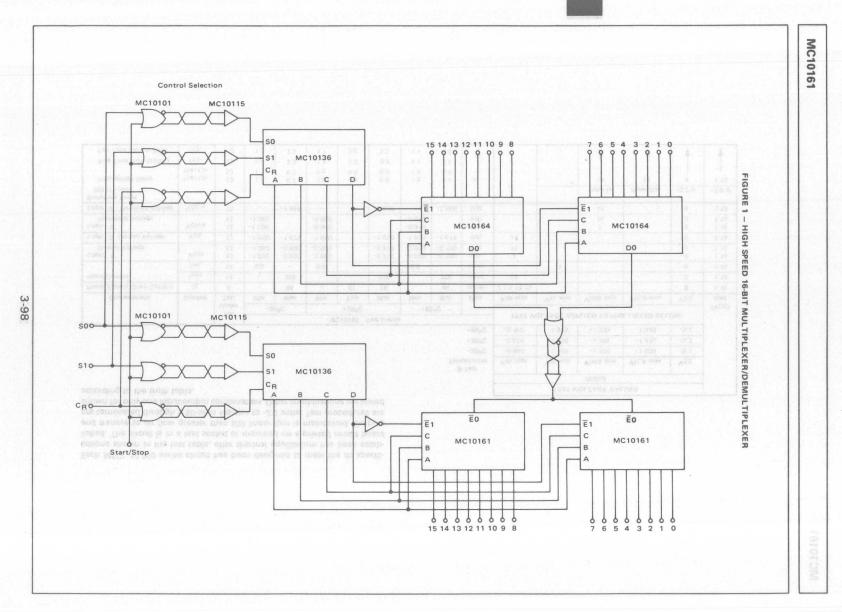




3-97

		TEST V	OLTAGE VAL	LUES	
		1	(Volts)		
@ Test Temperature	VIH max	VIL min	VIHA min	VILA max	VEE
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

										+85-6	-0.700	-1.025	-1.035	-1.440	-3.2	
LI I METOTO		ecial)	6	Mary Trans	M	C10161	Test Limits	5			TEST VI	OLTAGE AR	PLIED TO PIN	S LISTED BEL	OW-	
		Pin Under	-3	0°C		+25°C		+8	5°C	-	TEST	JETAGE AFT	EIED TOTTIN	S EISTED BEE		(Vcc)
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	VIH max	VIL min	VIHA min	VILA max	VEE	Gnd
Power Supply Drain Current	1E	8		84	-	61	76	1 -	84	mAdc	2,7,9,14,15	-	LILE STORY	-	8	1,16
Input Current	linH	14	-	350	- 900		220	Library.	220	μAdc	14			Market M.	8	1,16
	linL	14	0.5	-	0.5	7		0.3		μAdc		14	-		8	1,16
Logic "1" Output Voltage	VOH	13 13	-1.060 -1.060	-0.890 -0.890	-0.960 -0.960	-	-0.810 -0.810	-0.890 -0.890	-0.700 -0.700	Vdc Vdc	2 15			00 -	8	1,16 1,16
Logic "0" Output Voltage	VOL	13	-1.890	-1.675	-1.850	-	-1.650	-1.825	-1.615	Vdc	14		-		8	1,16
Logic "1" Threshold Voltage	VOHA	13 13	-1.080 -1.080	-51	-0.980 -0.980	1		-0.910 -0.910	- 14	Vdc Vdc			2 15	10104	8	1,16 1,16
Logic '0" Threshold Voltage	VOLA	13	-	-1.655		4000	-1.630		-1.595	Vdc		4	14	1 7-1 7	8	1,16
Switching Times (50 12 Load)	K_X	11>	1							TE	TT		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t14+13- t14-13+	13 13	1.5 1.5	6.2	1.5	4.0 4.0	6.0 6.0	1.5	6.4	ns			14	13	8	1,16
Rise Time (20% to 80%)	t13+	13	1.0	3.3	1.1	2.0	3.3	1.1	3.5				. 1			
Fall Time (20% to 80%)	112	13	1.0	3.3	1.1	2.0	3.3	1.1	3.5	0 7 0	0.0		0 1 6	00 10		



BINARY TO 1-8 DECODER (HIGH)

The MC10162 is designed to convert three lines of input data to a one-of-eight output. The selected output will be high while all other outputs are low. The enable inputs, when either or both are high, force all outputs low.

The MC10162 is a true parallel decoder. No series gating is used internally, eliminating unequal delay times found in other decoders.

This device is ideally suited for demultiplexer applications. One of the two enable inputs is used as the data input, while the other is used as a data enable input.

A complete mux/demux operation on 16 bits for data distribution is illustrated in Figure 1 of the MC10161 data sheet.

 $P_D = 315 \text{ ns typ/pkg (No Load)}$

 $t_{pd} = 4.0 \text{ ns typ}$

 t_r , $t_f = 2.0 \text{ ns typ } (20\%-80\%)$

E0 2 E1 15 O 6 Q0 A 7 O 3 Q3 B 9 O 12 Q5 O 11 Q6 C 14 VCC1 = Pin 1 VCC2 = Pin 16 VEE = Pin 8 INPUTS O UTPUTS E0 E1 C B A Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7

	11	NPUT	S					OUT	PUTS	18		
ĒΟ	Ē1	С	В	Α	Q0	Q1	Q2	Q3	04	Q5	Q6	0.7
L	L	L	L	L	H	L	L	L	L	L	L	L
L	L	L	L	Н	L	Н	- L	L	L	L	L	L
L	L	E8	Н	L	·L	L	Н	L	L	L	L	L
L	L	L	Н	H	L	L	L	H	L	L	L	L
L	L	H	L	L	L	L	L	L	Н	L	L	L
L	L	H	L	Н	L	L	L	L	L	Н	L	L
L	L	Н	Н	L	L	L	L	L	L	L	Н	L
L	L	Н	Н	Н	L	L	L	L	L	L	L	Н
H.	φ	φ	φ	φ	L	L	L	L	L	L	L	L
φ	Н	φ	φ	φ	L	L	L	L	L	L	L	L

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MECL 10K SERIES

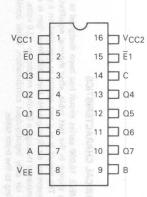
BINARY TO 1-8 DECODER

(HIGH)

L SUFFIX CERAMIC PACKAGE

P SUFFIX
PLASTIC PACKAGE
CASE 648





Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to $-2.0\ volts$. Test procedures are shown for only input/output combination. Other combinations are tested according to the truth table.

		TEST V	OLTAGE VA	UES	
@Test			(Volts)		
	VIH max	VIL min	VIHA min	VILA max	VEE
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic Sym	2 2 2	5,0				MC1016	2 Test Lin	nits				. 0	2983		>=	
	-50, -50 -12	Pin Under	-30	o°C	+25°C			+8	5°C		TEST VOLTAGE APPLIED TO PINS LISTED BELOW:					(VCC)
	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	VIH max	VIL min	VIHA min	VILA max	VEE	Gnd
Power Supply Drain Current	1 _E	8	-	84	- 1	61	76	-	84	mAdc	15	2.5	7 5-50	# (2,	8	1,16
Input Current	linH	14	- A	350	- 3	-5	220	1 -	220	μAdc	14		0- 10 B	2	8	1,16
	linL	14	0.5	5 - 75	0.5	2	7-	0.3	- 1	μAdc	Ge-	14	S 2- 00 9	3.8	8	1,16
Logic "1" Output Voltage	VOH	13	-1.060	-0.890	-0.960	1-1	-0.810	-0.890	-0.700	Vdc	14	8.5	B & B &	1.8	8	1,16
Logic "0" Output Voltage	VOL	13 13	-1.890 -1.890	-1.675 -1.675	-1.850 -1.850	-	-1.650 -1.650	-1.825 -1.825	-1.615 -1.615	Vdc Vdc	2 15	23	B its	100	8 8	1,16 1,16
Logic "1" Threshold Voltage	VOHA	13	-1.080	1-1	-0.980	-	-	-0.910	6	Vdc	9 8	900	14	B 573	8	1,16
Logic "O" Threshold Voltage	VOLA	13 13	- I	-1.655 -1.655	-		-1.630 -1.630	-	-1.595 -1.595	Vdc Vdc	1 1	8.5	2 15	2 8	8 8	1,16
Switching Times - (50-ohm load)									85	S. S.	3 2	9 5 6	Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t14+13+	13	1.5	6.2	1.5	4.0	6.0	1.5	6.4	ns	112	恒星五	14	13	8	1,16
K-X-X-D	t14-13-	13	1.5	6.2	1.5	4.0	6.0	1.5	6.4	1	-	분명 등	를 끄 큰 형	5 5	6	51
Rise Time (20% to 80%)	t+	13	1.0	3.3	1.1	2.0	3.3	1.1	3.5	1	7.0	14 PK	图 图 3	0 10	8	
Fall Time (20% to 80%)	t-	13	1.0	3.3	1.1	2.0	3.3	1.1	3.5		-	Party Party Barry	0 1	100	*	*

3-100



ERROR DETECTION- CORRECTION CIRCUIT

The MC10163 and the MC10193 are error detection and correction circuits. They are building blocks designed for use with memory systems. They offer economy in the design of error detection/correction subsystems for mainframe and add-on memory systems. For example, using eight MC10163s together with eight 12-bit parity checkers (MC10160), single-bit error detection/correction and double-bit error detection can be done on a word of 64-bit length. Only eight check bits (B0–B7) need be added to the word. A useful feature of this building block is that the MC10193 option generates the parity of all inputs to the block. Thus, if the MC10193 is applied in a byte sequence, individual byte parity is automatically available.

MECL 10K SERIES

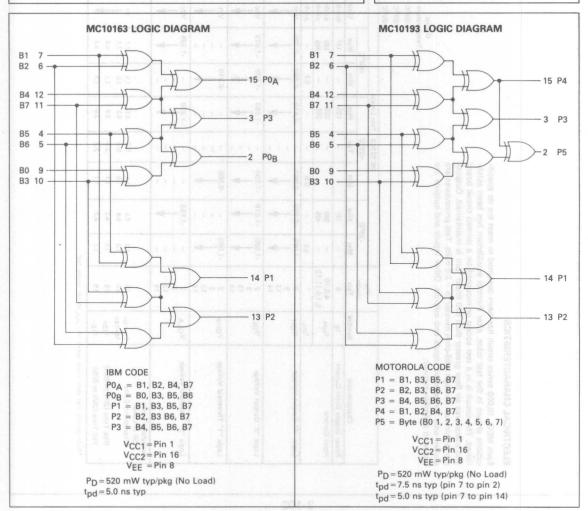
ERROR DETECTION — CORRECTION CIRCUIT



P SUFFIX PLASTIC PACKAGE CASE 648



L SUFFIX
CERAMIC PACKAGE
CASE 620



Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to $-2.0\ volts$. Test procedures are shown only for selected inputs and outputs. Other inputs and outputs are tested in a similar manner.

	31	TEST VO	LTAGE V	ALUES	198
	XX =		(Volts)	19	
@ Test Temperature	VIHmax	VILmin	VIHAmin	VILAmax	VEE
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

										100 0	-0.700	-1.025	-1.033	-1.440	-0.2	A COLUMN
		Pin			M	C10163	Test Limit	s		100	TE	ST VOLT	AGE APPI	LIED TO		1
		Under	-3	0°C		+25°C		+8!	5°C			PINS LI	STED BEL	.ow:		(Vcc
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	VIHmax	VILmin	VIHAmin	VILAmax	VEE	Gnd
Power Supply Drain Current	1E	8		137	-	-	125	-	137	mAdc	-	-	-	-	8	1,16
Input Current	linH	4,6,10 5,7,9,11,12	-	350 425	5.0	-0.0	220 265	- 1	220 265	μAdc μAdc	4,6,10 5,7,9,11,12	100	五五 8	75.0	8	1,16 1,16
	linL	•	0.5	-	0.5	-	- "	0.3	-	μAdc	B = 03	198	4 5 16	2.8	8	1,16
Logic ''1'' Output Voltage	Voн	2 3 13	-1.060	-0.890	-0.960	=	-0.810	-0.890	-0.700	Vdc	4 4 11	15 Tal.	Mary And And And And And And And And And And	Division of the control of the contr	8	1,16
	13	14				- E	- P			V	_11	8 0- 1	3 5 6	6 8	N.	A
Logic ''0'' Output Voltage	VOL	3 13	-1.890	-1.675	-1.850	10 - 10 -	-1.650	-1.825	-1.615	Vdc	Mary Mary Mary Mary Mary Mary Mary Mary	4 11 11	POST POST Strong	de la la la la la la la la la la la la la	8	1,16
		14		V		-					84.5	11	2 - 5	a -	V .	
Logic "1" Threshold Voltage	VOHA	2 3	-1.080	Ξ	-0.980	-	-	-0.910	-	Vdc	多事品		5 11	3 =	8	1,16
	1 4	13 14	*	_	•	人_	人	1	- 1	4	111	日本市	5 4	8 =	+	•
Logic "0" Threshold Voltage	VOLA	2 3	-	-1.655	_	-	-1.630	7=7	-1.595	Vdc	2 1 2		111	5 11	8	1,10
	1	13 14	7-	*	-	-	+				314	450	0 = 0	5 4	1	
Switching Times	1				1	1	1	Not	3 9		+1.11 V	4 6 2	Pulse In	Pulse Out	-3.2 V	+2.0
(50 Ω Load) Propagation Delay	[†] 7+15+ [†] 4+14+	15 14	1.3 1.3	6.8 6.8	1.5 1.5	5.0 5.0	6.5 6.5	1.5 1.5	7.1 7.1	ns	100	STORY OF	7 4	15 14	8	1,10
Rise Time (20% to 80%)	t ₁₅₊	15	1.1	4.2	1.1	2.0	3.9	1.1	4.4		1 4 4 5	222	7	15		1 1
Fall Time (20% to 80%)	t15-	15	1.1	4.2	1.1	2.0	3.9	1.1	4.4	4	1 2 2 3	E 9	7	15	5 V	

^{*}Individually test each input, apply VILmin to pin under test.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to $-2.0\,\mathrm{volts}$. Test procedures are shown only for selected inputs and outputs. Other inputs and outputs are tested in a similar manner.

		TEST	VOLTAGE	VALUES									
	(Volts)												
@ Test Temperature	VIHmax	VILmin	VIHAmin	VILAmax	VEE								
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2								
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2								
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2								
	La car a car	1 11000	100000										

			1			and the state of	San Brook			+85°C	-0.700	-1.825	-1.035	-1.440	-5.2	0 3 5
25554	es es le	Pin	-31	0°C	M	+25°C	Test Limit		5°C			TEST VO	(Vcc)			
Characteristic	Symbol	Under Test	Min	Max	Min	Тур	Max	Min	Max	Unit	VIHmax	VILmin	The same of the sa	VILAmax	VEE	Gnd
Power Supply Drain Current	ΙE	8	12-	137	- *	F _ K	125	-	137	mAdc	100-	15-8-	S e2-00	5 JL 6 9	8	1,16
Input Current	linH	4,6,10 5,7,9,11,12		350 425	3	13.5	220 265		220 265	μAdc μAdc	4,6,10 5,7,9,11,12	5-3	3 12 23	E .	8	1,16 1,16
	linL		0.5		0.5	- B	·	0.3	1 ml-	μAdc	0 2 7		N	F = 50	8	1,16
Logic "1" Output Voltage	Vон	2 3 13	-1.060	-0,890	-0.960	-	-0.810	-0.890	-0.700	Vdc	4 4	- 471	(2.10)	781	8	1,16
	20 10 15	14		*	*	-		*		*	11	I	_	_		
Logic "0" Output Voltage	VOL	2 3 13	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615	Vdc		4 11 11	8 2-8	£ \$ 2	8	1,16
	10 II I	14	1		*			♥	*		8 5 8 8 9	11	1 15 1	- 1- B	*	A Ve
Logic "1" Threshold Voltage	VOHA	2 3	-1.080	-	-0.980	15		-0.910	15-	Vdc		25-0	5 11	1 - 0	8	1,16
	19 9	13 14		_			I SE						5 4	1 五章	10	
Logic "0" Threshold Voltage	VOLA	2 3	1 1	-1.655		-	-1.630	-	-1.595	Vdc	58 2 53	3-E	4 1	5 11	8	1,16
	2 1 1	13 14	-		-	- 1		_				8E-3		5 4	3 8	
Switching Times							2.			5 4	+1.11 V	23	Pulse In	Pulse Out	-3.2 V	+2.0 V
(50 Ω Load) Propagation Delay	t7+15+ t4+14+ t7+2+	15 14 2 2	1.3 1.3 1.8 1.8	6.8 6.8 8.9 8.9	1.5 1.5 2.0 2.0	5.0 5.0 7.5 7.5	6.5 6.5 8.5 8.5	1.5 1.5 2.0 2.0	7.1 7.1 9.2 9.2	ns		12 e	7 4 7 4	15 14 2 2	8	1,16
Rise Time (20% to 80%)	t ₄₊₂₊	15	1.1	4.2	1.1	2.5	3.9	1.1	4.4	9 15		1 8 8 5 6 8	7	15	4 8	
Fall Time (20% to 80%)	^t 15-	- 15	1.1	4.2	1.1	2.5	3.9	1.1	4.4		1 2 2 5	2-2	7	15	10	3 V S

^{*}Individually test each input, apply $V_{\mbox{\scriptsize ILmin}}$ to pin under test.

The MC10163 is a building block for generating the modified Hamming single-error-correction, double-error-detection (SEC-DED) code used in the IBM 370/145 memory. While the MC10163 can also be used for generating other patterns, it is optimized for generating the pattern shown in the H matrix of Figure 1.

When writing into a memory, the MC10163 is used to generate the eight check bits (C0-C32, CT) which are stored with the 65 data bits (B0-B63). These check bits are generated by taking the parity of all data bits marked with an X in the appropriate row of the H matrix. (C0, C1, C32, CT, are even parity; C2, C4, C8, C17, are odd parity.) To generate these check bits with the building blocks, eight MC10163s and eight MC10160 parity checkers are used. One MC10163 is connected to each byte of data and the outputs of these building blocks are connected to the eight MC10160 parity checkers, one for each check bit. Figure 2 shows which connections are required (i.e., C0 is the even parity of output P0A of the MC10163 on the "zero" byte of data, output POB of the "zero" byte, POA of the "one" byte, -, POB of the "three" byte and data bit 32.)

During the memory read operation, the fetched check bits previously generated (as described) are exclusive-ORed with newly generated C0-C32 to generate syndrome bits S0-S32. Syndrome ST is a special case where ST is the even parity of all eight fetched check bits and all 64 fetched data bits. For determining the type and location of an error:

- If all syndromes (S0–S32 and ST) are false, there is no error.
- 2. If ST is true and S0–S32 are false, the CT is in error.
- 3. If ST is false and one or more of S0–S32 is true, an uncorrectable error has occurred.
- If ST is true and one or more of S0–S32 is true, simply add the S1–S32 bits to get the binary location of the error (S1 has weight, 1, S2 weight 2, S4 weight 4, etc.)

Data bits B0 and B32 are special cases of this location technique: B0 is in error if ST, S0, and S32 are true; B32 is in error if ST, S0, S1, and S32 are true.

FIGURE 1 - 370/145 PATTERN

		вч	TE	0		_	8	100	BYT	TE 1				8	TYE	E 2	1000				В	TE	3	1			В	YTE	4	18	100		В	Y TE	5			8	YT	E 6				В	BYT	E 7			
1	2	3	3 4	5	6	7	8 9	3 10) 11	121	3 14	4 15	16 1	7 18	19 3	20 2	1 2	2 23	24	25	26 2	7 2	8 29	30	31	32 33	34	35 3	6 3 7	38	39 4	0 41	42 4	3 44	45 4	6 47	48 4	9 50	51 5	52 53	54	55 5	6 57	58	59 6	0 6	1 62	63	3 E
×			x	×	×	×	×	(×	×	× :	x x	×	x :	x x	×	× 2	K X	×	×	×	× 1	× ×	×	×	×	×																							(
×		ж		×		×	3	e -	×		ĸ	×		K	×	>		×		×	2		×		×	××		×	×		×	×			x	×	×		×	×		×	×		×	×		×	
	2	×			×	×		×	×		×	×		×	×		×	×			X 1			×	×		×	×		x	x		x >		20	x		×	×		х	x		x	×		×	×	(
			×	×	×																																			x x							×		
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													X I	x x	×	× ×	c x	×	×	X	X I	c x	×	×	×												x x	×	x :	x x	x	x x	×	x	X)				
																										x x	×	X 3	×	×	x x	x	X X	×	×	×	x x	×	X :	x x	X	x x	×	×	x)		×		
×	Ж		×			×	X		×	1	t x		×		×	3	< ×			×	X	×			×	×	×				××		>		X :		×		×	×	×		×	×		K		×	C

FIGURE 2 — 370/145 PATTERN GENERATION

C0 = P0A0	POBO	POA1	POB1	POA2	POB2	PO _{A3}	PO _{B3}	B(32)
C1 = P10	P11	P12	P13	P14	P15	P16	P17	B(32)
C2 = P20	P21	P22	P23	P24	P25	P26	P27	
C4 = P30	P31	P32	P33	P34	P35	P36	P37	
C8 = P0 _{A1}	POB1	POA3	POB3	PO _{A5}	POB5	POA7	POB7	
C16 = P0A2	POA2	PO _{A3}	POB3	POA6	POB6	POA7	POB7	
$C32 = P0_{A4}$	POB4	POA5	PO _{B5}	POA6	POB6	POA7	POB7	B(0)
CT = POAO	POB1	POB2	PO _{A3}	POA4	PO _{B5}	P086	POA7	B(0)
Where for PNN	1: N = MC	10163 Ou	tput					

MC10193 APPLICATIONS INFORMATION

70 71 69 EXAMPLE PATTERN MOTOROLA FIGURE 3

The MC10193 is a building block for generating modified Hamming SEC-DED codes. It can be used for any length data word and for a variety of codes. The MC10193 is optimized for codes organized on a byte repetitive basis and has the advantage of automatically supplying whole byte parity (P5 output). While it is possible to use a number of criteria for choosing a pattern, the pattern of Figure 3 was chosen on the basis of speed and ease of error location decode. As can be seen in the H matrix of Figure 3, the pattern is repetitive by byte with the various rows generated by only five combinations of bit parities within the bytes. For the 64 bit data word in the example of Figure 3, the eight check bits (B64 to B71) are generated by the odd parity of all data bits indicated by an -X in the appropriate row. The syndromes S1 to S8 are generated by including the fetched check bits in the same generator that originally generated the check bits.

The pattern of Figure 3 is easily generated by using eight MC10193 devices, one for each data byte and eight MC10160 parity checkers, one for each syndrome/check bit. The connections of building blocks and parity checkers are shown in tabular form in Figure 4 and in schematic form in Figure 6.

Once the syndrome bits (S1 to S8) have been formed from fetched data (B0 to B63) and fetched check bits (B64 to B71), the determination of type and location of error is simply done:

- 1. If all syndromes are false, there is no error.
- If one syndrome is true, the corresponding check bit is in error.
- If more than one syndrome is true, and the parity of all syndromes is even, a multiple (uncorrectable) error has occurred.
- If more than one syndrome is true, and the parity of all syndromes is odd, a single error has occurred and is easily located by the circuit of Figure 5.

Figure 5 gives the error location circuit for the example pattern. The outputs EB0 to EB7 are a one-of-eight-high code giving the byte in error. Outputs EC0 to EC3 give the binary location of the bit in error within the located byte. Since this location process can occur simultaneously with the determination of error type described, the entire error correction sequence (using a toggling fetched data latch) takes less than 20 ns. This is because an error occurrence detector is a simple ORing of S1 to S8. The error locator has simultaneously located the error which is then corrected as though the error was a single (and therefore correctable) error. The parity of syndromes then determines if the error was indeed single, and interrupts the CPU if the error was an uncorrectable (multiple) error. Since uncorrectable data is unusable without special handling, the CPU would be interrupted anyway; therefore this automatic correction of any error as if it were single does not create any problems. This fast error correction technique allows single error correction on a noninterrupt basis with only a 20 ns memory system access time penalty.

These techniques can, of course, be extended to large or smaller data words.

each syndromizationed

length data word and for a variety of ordes. The MC19193 is optimized for codes organized or a byte repetitive S1 = P10 P11 P12 P13 P54 P55 P56 B(64) S2 = P20 P21 P22 P23 PSS B(65) S3 = P30 P31 P32 P33 P56 ne to sees box box S4 = P40 P41 P42 P43 P55 P56 S5 = P14 P15 P16 S6 = P24 S7 = P34 P36 P37 S7 = P34 S8 = P44 P46 P51

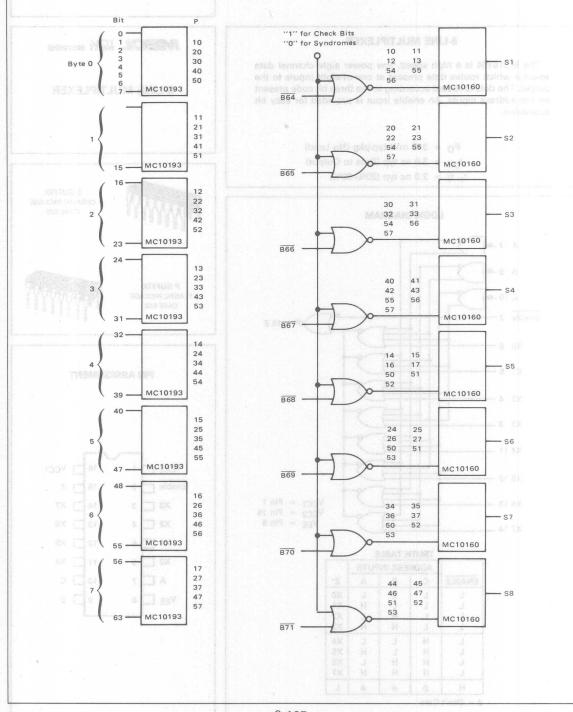
Where for P_{NM}: N = MC10193 Output M = Byte Number

FIGURE 5 — M2 PATTERN CORRECTION MATRIX

 $\overline{S5} \overline{S6} \overline{\overline{S7}} \overline{\overline{S8}} \longrightarrow EB0$ $\overline{S5} \overline{\overline{S6}} \overline{\overline{S7}} \overline{\overline{S8}} \longrightarrow EB1$ $\overline{S5} \overline{\overline{S6}} \overline{\overline{57}} \overline{\overline{58}} \longrightarrow EB2$ $\overline{S5} \overline{\overline{56}} \overline{\overline{57}} \overline{\overline{58}} \longrightarrow EB3$ $\overline{S1} \overline{\overline{S2}} \overline{\overline{\overline{S3}}} \overline{\overline{54}} \longrightarrow EB4$ $\overline{S1} \overline{\overline{S2}} \overline{\overline{S3}} \overline{\overline{54}} \longrightarrow EB5$ $\overline{S1} \overline{S2} \overline{\overline{S3}} \overline{\overline{54}} \longrightarrow EB6$ $\overline{S1} \overline{\overline{S2}} \overline{\overline{S3}} \overline{\overline{54}} \longrightarrow EB6$

2. If one systemms is true, the corresponding check b.

\$1 — EC0 \$2 — EC1 \$3 — EC2 \$5 — EC0 \$6 — EC1 \$7 — EC2



MC10164

8-LINE MULTIPLEXER

The MC10164 is a high speed, low power eight-channel data selector which routes data present at one-of-eight inputs to the output. The data is routed according to the three bit code present on the address inputs. An enable input is provided for easy bit expansion.

PD = 310 mW typ/pkg (No Load)

tpd = 3.0 ns typ (Data to Output)

 t_r , $t_f = 2.0 \text{ ns typ } (20\%-80\%)$

MECL 10K SERIES

8-LINE MULTIPLEXER

LSUFFIX CERAMIC PACKAGE CASE 620 P SUFFIX PLASTIC PACKAGE CASE 648

V _{CC2}	Н	1	V	16	Ь	V _{CC1}
Enable		2		15	Б	z
ХЗ		3		14		X7
X2		4		13	b	X6
X1		5		12		X5
X0		6		11	þ	X4
A		7		10	Þ	С
VEE	d	8		9	Þ	В
	SM		ole 7		ı	

LOGIC DIAGRAM C 10 -Enable 2 X0 6 X1 5 X2 4 X3 3 X4 11 -X5 12 V_{CC1} = Pin 1 X6 13 V_{CC2} = Pin 16 V_{EE} = Pin 8 X7 14 -TRUTH TABLE ADDRESS INPUTS ENABLE Z X0 H X1 L 1 X2 L Н H X3 X4 X5 H L H L L H X6 H H X7 Н $\phi = Don't Care$

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established in an ambient temperature of $25^{\circ}\mathrm{C}$, while the circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs tested in the same manner.

		TEST V	OLTAGE VA	LUES	
07	3		(Volts)		
@Test Temperature	VIH max	VIL min	VIHA min	VILA max	VEE
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

		Pin			M		Test Limi				TEST VI	I TAGE APE	I IED TO PIN	IS LISTED BE	LOW	
		Under	-30	o _C	and the same of th	+25°C		+8!	5°C		1531 VC	LIAGE AFF	LIED TO FIN	S LISTED BE	LOW	(Vcc)
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	V _{IH} max	VIL min	VIHA min	VILA max	VEE	Gnd
Power Supply Drain Current	1E	8	-	83	-	60	75	-	83	mAdc	-	E	-	-	8	1,16
Input Current	lin H	2	=	425	1816	3 E3 II	265	-	265	μAdc	4	-	77	_	8	1,16
	lin L	4	0.5	-	0.5		-	0.3		μAdc		4		-	8	1,16
Logic "1" Output Voltage	VOH	15	-1.060	-0.890	-0.960	- 75	-0.810	-0.890	-0.700	Vdc	4,9		2	155	8	1,16
Logic "0" Output Voltage	VOL	15	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615	Vdc	9		-5	1 1 8	8	1,16
Logic "1" Threshold Voltage	VOHA	15	-1.080	-	-0.980	-	-]	-0.910	-	Vdc	4,9	-	20	2	8 -	1,16
Logic "0" Threshold Voltage	VOLA	15	-	-1.655	-	-60	-1.630	-	-1.595	Vdc	9	-	-	2	8	1,16
Switching Times (50 Ω Load)		10 to 10 to									+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay Rise Time (20% to 80%) Fall Time (20% to 80%)	t4+15+ t4+15- t7+15+ t7-15- t2+15- t2-15+ t+	15 15 15 15 15 15 15	1.5 1.5 1.9 1.9 0.9	4.9 4.9 6.5 6.5 3.5	1.5 1.5 2.0 2.0 1.0 1.0 1.1	3.0 3.0 4.0 4.0 2.0	4.7 4.7 6.2 6.2 3.1 3.1 3.3	1.6 1.6 2.2 2.2 1.0 1.0 1.2	5.0 5.0 6.7 6.7 3.3 3.3 3.6	ns	9 9 5 5 7,5 7,5 7,5 9		4 4 7 7 2 2 4	TIS THE BOOK OF TH	8	1,16

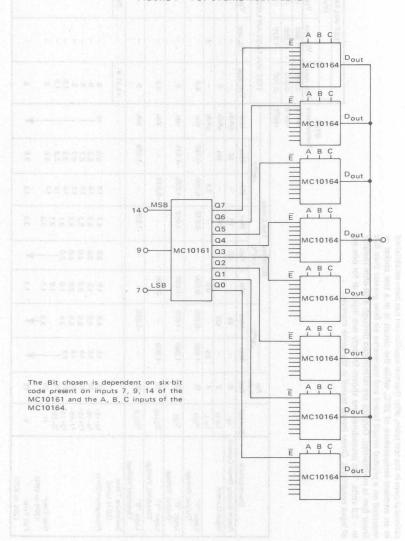
0

The MC10164 can be used wherever data multiplexing or parallel to serial conversion is desirable. Full parallel gating permits equal delays through any data path. The output of the MC10164 incorporates a buffer gate with

eight data inputs and an enable. A high level on the enable forces the output low. The MC10164 can be connected directly to a data bus, due to its open emitter output and output enable.

Figure one illustrates how a 1-of-64 line multiplexer can be built with eight MC10164's wire ORed at their outputs and one MC10161 to drive the enables on each multiplexer, without speed degradation over a single MC10164 being experienced.

FIGURE 1 - 1-OF-64 LINE MULTIPLEXER



3



8-INPUT PRIORITY ENCODER

The MC10165 is a device designed to encode eight inputs to a binary coded output. The output code is that of the highest order input. Any input of lower priority is ignored. Each output incorporates a latch allowing synchronous operation. When the clock is low the outputs follow the inputs and latch when the clock goes high. This device is very useful for a variety of applications in checking system status in control processors, peripheral controllers, and testing systems.

The input is active when high, (e.g., the three binary outputs are low when input D0 is high). The Q3 output is high when any input is high. This allows direct extension into another priority encoder when more than eight inputs are necessary. The MC10165 can also be used to develop binary codes from random logic inputs, for addressing ROMs, RAMs, or for multiplexing data.

PD = 545 mW typ/pkg (No Load)

tpd = 4.5 ns typ (Data to Output)

 t_r , $t_f = 2.0 \text{ ns typ } (2\%-80\%)$

MECL 10K SERIES

8-INPUT PRIORITY ENCODER MC10165



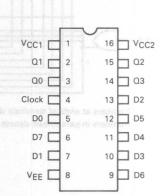
L SUFFIX CERAMIC PACKAGE CASE 620

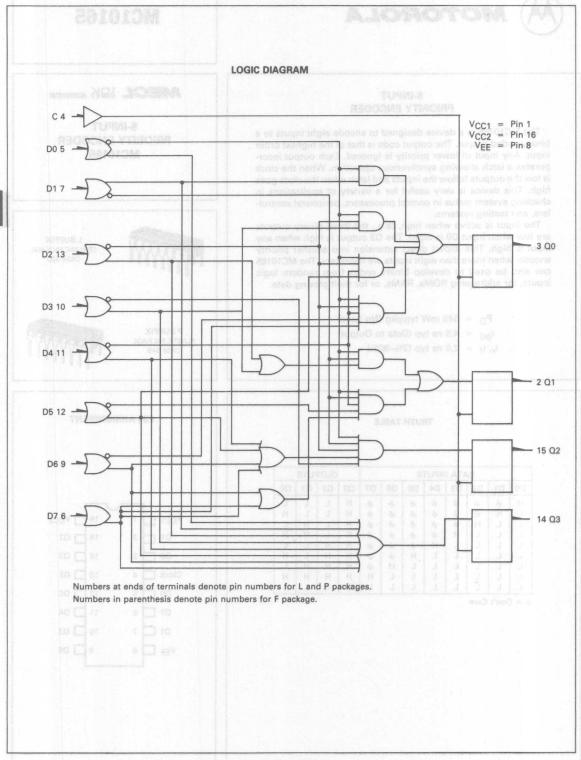
P SUFFIX
PLASTIC PACKAGE
CASE 648



TRUTH TABLE

		D	ATA I	NPU	TS				OUT	PUTS	
D0	D1	D2	D3	D4	D5	D6	D7	Q3	Q2	Q1	QO
Н	φ	φ	φ	φ	φ	φ	φ	Н	L	L	L
L	Н	φ	φ	φ	φ	φ	φ	Н	L	L	Н
L	L	Н	φ	φ	φ	φ	φ	Н	L	Н	L
L	L	L	Н	φ	φ	φ	φ	Н	L	Н	Н
L	L	L	L	H	φ	φ	φ	Н	Н	L	L
L	L	L	.L	L	Н	φ	φ	Н	Н	L	Н
L	L	L	L	L	L	Н	φ	Н	Н	Н	L
L	L	L	L	L	L	L	Н	Н	Н	Н	Н
L	L	L	L	L	L	L	L	L	OL I	LJ	L





Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established in an ambient temperature of 25°C, while the circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs tested in the same manner.

	50 3	TEST \	OLTAGE V	ALUES	
	1115	2	(Volts)	3.,	1 34
@ Test Temperature	VIH max	V _{IL min}	VIHA min	VILA max	VEE
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

					M	C10165	Test Lim	its								5 0
		Pin Under	-30	o°C		+25°C	1031 2		5°C	-	TEST VO	LTAGE AP	PLIED TO P	INS LISTED	BELOW:	(Vcc)
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	VIH max	VIL min	VIHA min	VILA max	VEE	Gnd
Power Supply Drain Current	1E	8	-	144	-	105	131	-	144	mAdc		-	-	- #	8	1,16
Input Current	lin H	4 5		390 350		-	245 220		245 220	μAdc μAdc	4 5 ①	-	-	- 50	8 8	1,16 1,16
	lin L	4 5	0.5 0.5	-	0.5 0.5		-	0.3 0.3		μAdc μAdc	1=13	4 5①	-	- 8	8	1,16 1,16
Logic "1" Output Voltage	V _{OH}	2 3 14 15	-1.060 -1.060 -1.060 -1.060	-0.890 -0.890 -0.890 -0.890	-0.960 -0.960 -0.960 -0.960	-	-0.810 -0.810 -0.810 -0.810	-0.890 -0.890 -0.890 -0.890	-0.700 -0.700 -0.700 -0.700	Vdc	6	88 4 4 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5		1 1 1	8	1,16
Logic "0" Output Voltage	VOL	2 3 14 15	-1.890 -1.890 -1.890 -1.890	-1.675 -1.675 -1.675 -1.675	-1.850 -1.850 -1.850 -1.850	E	-1.650 -1.650 -1.650 -1.650	-1.825 -1.825 -1.825 -1.825	-1.615 -1.615 -1.615 -1.615	Vdc		4	=	onghi	8	1,16
Logic "1" Threshold Voltage	VOHA	2 3 14 15	-1.080 -1.080 -1.080 -1.080		-0.980 -0.980 -0.980 -0.980	Ē	-	-0.910 -0.910 -0.910 -0.910	-	Vdc		4	6	-	8	1,16
Logic "0" Threshold Voltage	VOLA	2 3 14 15		-1.655 -1.655 -1.655 -1.655	1111	<u> </u>	-1.630 -1.630 -1.630 -1.630		-1.595 -1.595 -1.595 -1.595	Vdc		4	=	6	8	1,16
Switching Times (50-ohm Load)				17.17					11000	Unit	+1.11 V	+0.31 V	Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay Data Input	t5+14+ t5-14- t7+3+ t11+15+ t13+2+	14 14 3 15 2	2.0	7.0	3.0		7.0	2.0	8.0	ns		# 4 M	5 5 7 11 13	14 14 3 15 2	8	1,16
Clock Input	t4-3+ t4-3- t4-14+	3 ② 3 ③ 14②	1.5	4.5	2.0	E	4.0	1.5	4.5	H	7 - 7	1	1	3 3 14		1
Setup Time	t _{setup} H t _{setup} L	143	6.0 6.0	METO.	6.0 6.0	3.4 3.0	0 0	6.0 6.0	inic	10165 1 D D	(A)	-	4,7	14 3		
Hold Time	thold H	16	1.0	ő – I	1.0	-2.3 -2.7	9-16	1.0	1 3	- 6			₩	(6)	0.00	
Rise Time (20% to 80%) Fall Time (20% to 80%)	t3+ t3-	1	5 1.1 1.1	3.5 3.5	1.1	2.0	3.3 3.3	1.1	3.5 3.5		-	4	7	97.37		

① The same limit applies for all D type input pins. To test input currents for other D inputs,

individually apply proper voltage to pin under test.

② Output latched to low state prior to test.

③ Output latched to high state prior to test.

^{*} To preserve reliable performance, the MC10165P (plastic-packaged device only) is to be operated in ambient temperatures above 70°C only when 500 lfpm blown air or equivalent heat sinking is provided.

APPLICATION INFORMATION

A typical application of the MC10165 is the decoding of system status on a priority basis. A 64 line priority encoder is shown in the figure below. System status lines are con-

nected to this encoder such that, when a given condition exists, the respective input will be at a logic high level. This scheme will select the one of 64 different system conditions, as represented at the encoder inputs, which has priority in determining the next system operation to be performed. The binary code showing the address of the highest priority input present will appear at the encoder outputs to control other system logic functions.

64-LINE PRIORITY ENCODER Z MC10164 MC10164 MC10164 Six bit output word yielding 1/2 MC10101 highest priority Clock channel present at input 00 MC10165 DO 01 Highest Priority 02 00 Input 03 DO 01 0 02 0.0 MC10165 DO 01 02 03 Q0 Q1 Q2 Q3 WC10165 Q1 Q2 Q3 DO MC10165 00 03 DO C DO D7 00 01 02 00 MC10165 DO 01 02 03 Q0 Q1 Q2 Q3 DO Lowest Input

5-BIT MAGNITUDE COMPARATOR

The MC10166 is a high speed expandable 5-bit comparator for comparing the magnitude of two binary words. Two outputs are provided: $A < B \ \text{and} \ A > B. \ A = B \ \text{can} \ \text{be obtained by NORing}$ the two outputs with an additional gate. A high level on the enable function forces both outputs low. Multiple MC10166s may be used for larger word comparisons.

 $P_D = 440 \text{ mW typ/pkg (No Load)}$

 t_{pd} = Data to output 6.0 ns typ

Ē to output 2.5 ns typ

 t_r , $t_f = 2.0 \text{ ns typ } (20\%-80\%)$

LOGIC DIAGRAM A4 9 B4 10 A3 12 B3 11 A2 13 B2 14 A1 6 B1 7 A0 5 B0 4 E 15 TRUTH TABLE Inputs Outputs

	5 20 5	INOTH TAI	JLL	1 21 3
	Inputs		Out	puts
Ē	Α	В	A < B	A > B
Н	X	X	L	L
L	Word A =	Word B	L	L
L	Word A >	Word B	L	Н
L	Word A <	Word B	Н	L

MECL 10K SERIES

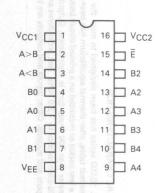
5-BIT MAGNITUDE COMPARATOR



L SUFFIX CERAMIC PACKAGE CASE 620

P SUFFIX PLASTIC PACKAGE CASE 648





Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to $-2.0\,$ volts. Test procedures are shown for only selected inputs and outputs. Other inputs and outputs are tested in a similar manner.

		TEST V	DLTAGE V	ALUES		
			Volts			
@ Test Temperature	VIHmax	VILmin	VIHAmin	VILAmax	VEE	
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2	
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2	
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2	

						240400	w			100 0	-0.700	-1.025	-1.000	-1.440	-5.2	
		Pin	-	-0-	IVIC		Test Limit		-0-		VOLTA	GE APPLIED	TO PINS	LISTED BE	LOW:	
		Under		0°C		+25°C			5°C	514						(Vcc
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	VIHmax	VILmin	VIHAmin	VILAmax	VEE	Gnd
Power Supply Drain Current	1E	8	(1/3	117	-	85	106	-	117	mAdc	-	4,7,10,11,14	5- 8	2) of 14	8	1,16
Input Current	linH	5	100	350	- /	-	220	-	220	μAdc	5	-	32 0	安臣音	8	1,16
	linL	5	0.5	-)	0.5	-	-	0.3		μAdc	-	5	4-5	《 产 页	8	1,16
Logic "1" Output Voltage	VOH	2 3	-1.060 -1.060	-0.890 -0.890	-0.960 -0.960	_	-0.810 -0.810	-0.890 -0.890	-0.700 -0.700	Vdc Vdc	5 4	8 I	計高	X 4 8	8	1,16
Logic "0" Output Voltage	VOL	2 3	-1.890 -1.890	-1.675 -1.675	-1.850 -1.850	=	-1.650 -1.650	-1.825 -1.825	-1.615 -1.615	Vdc Vdc	5,15 4,15	E	となっ		8	1,16
Logic "1" Threshold Voltage	VOHA	2 3	-1.080 -1.080	OE !	-0.980 -0.980	_	-	-0.910 -0.910	_	Vdc Vdc	5 4	9-	वृद्ध	15 15	8	1,16
Logic "0" Threshold Voltage	VOLA	2 3	_	-1.655 -1.655			-1.630 -1.630	-	-1.595 -1.595	Vdc Vdc	5 4	ğ I	15 15	1 2 5	8	1,16
Switching Times (50 Ω Load) Propagation Delay Data to Output	†9+2+ †9-2- †11-2+ †11+2-	2 2 2 2 2	1.0	8.0	1.0	6.0	7.6	1.0	8.4	ns	+1.11 V	4450 BLASS DA	9 9 11 11	Pulse Out	-3.2 V	+2.0
Enable to Output Rise Time (20% to 80%)	t7+3+ t7-3- t15-3+ t15+3- t2+	3 3 3 3		3.8 3.8 3.6	¥ 1.1	2.5 2.5 2.0	3.6 3.6 3.5	1.1	4.0 4.0 3.8		6 6 10 10	9:	7 7 15 15 9	3 3 3 3 2		
Fall Time (20% to 80%)	t2-	2		3.6	1.1	2.0	3.5	1.1	3.8		-		9	2		Y

APPLICATION INFORMATION FIGURE 1 — 9-BIT MAGNITUDE COMPARATOR A080 A181 A282 A383 A484 A585A686A787A888 В4 B24 ___ 0 A1 A2 A3 A4 B0 B1 B2 B3 B4 0 A1 A2 A3 A4 B0 B1 B2 B3 B4 A24-A4 B23 --- B3 A23-A3 A< MC10166 MC10166 B22 - B2 A22 -A2 A > B A < BB21 -B1 A>E A21-A1 B20 - B0 A20-AO B19 - B4 A 19 -A4 B18 -В3 A18-A3 A<B A>B A<B A = B B17 - B2 For 9-Bit Word A17-A2 B16 - B1 A>B A16-A1 B15 - B0 A15 -AO В4 B14_ B4 A14_ A4 A4 B13 - B3 В3 A13 -A3 A<F A3A<R B12 ___ B2 B2 A2 A2 B11-B1 A>B A11 A1 B0 A1 B0 A10 -AO AO B9 _ B4 A9 -A4 R8 --B3 A3 A<B The MC10166 compares the magnitude of two 5-bit B7 -B2 words. Two outputs are provided which give a high level A2 B6-B1 A>E for A > B and A < B. The A = B function can be obtained A6 -A1 B0 by wire-ORing these outputs (a low level indicates A = B) B5or by NORing the outputs (a high level indicates A = B). A5-AO For longer word lengths, the MC10166 can be serially B4 -84 expanded or cascaded. Figure 1 shows two devices in a A4-A4 serial expansion for a 9-bit word length. The A > B and в3. B3 A < B outputs are fed to the A0 and B0 inputs respectively A3-A3 A < B B2 -B2 of the next device. The connection for an A = B output is A2-A2 also shown. The worst case delay time of serial expansion B1 -B1 A>E is equal to the number of comparators times the data-to-B0 -B0 output delay. A0 -AO For shorter delay times than possible with serial expansion, devices can be cascaded. Figure 2 shows a 25-bit FIGURE 2 - 25-BIT MAGNITUDE COMPARATOR cascaded comparator whose worst case delay is two datato-output delays. The cascaded scheme can be extended to longer word lengths.



MC10168

QUAD LATCH

The MC10168 is a Quad Latch with common clocking to all four latches. Separate output enabling gates are provided for each latch, allowing direct wiring to a bus. When the clock is high, outputs will follow the D inputs. Information is latched on the negative-going transition of the clock.

PD = 310 mW typ/pkg (No Load)

 $t_{pd} = \overline{G} \text{ to } Q = 2 \text{ ns typ}$ D to Q = 3 ns typ

C to Q = 4 ns typ

 t_r , $t_f = 2.0 \text{ ns typ } (20\%-80\%)$

MECL 10K SERIES

QUAD LATCH

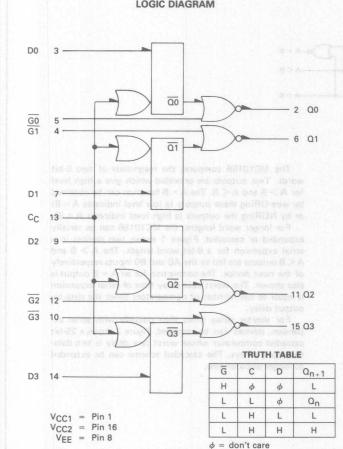


LSUFFIX CERAMIC PACKAGE CASE 620

P SUFFIX PLASTIC PACKAGE CASE 648



LOGIC DIAGRAM





Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to $-2.0\,\text{volts}$. Test procedures are shown for only selected inputs and outputs. The other inputs and outputs are tested in the same manner.

		TEST	(Volts)	VALUES	- 6
@ Test Temperature	V _{IHmax}	VILmin	VIHAmin	VILAmax	VEE
-30°C	-1.890	-1.890	-1.205	-1.500	-5.2
+25°C	-1.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

				hard to be a second						+85 C	-0.700	-1.825	-1.035	-1.440	-5.2	
		Pin		1.3	M	C10168	Test Limit	s		1818	TES	ST VOLT	AGE APPI	IED TO PI	NS	k Kine
	1	Under	-30	0°C		+25°C		+85	5°C		100	LIS	STED BEL	OW:		(Vcc
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	VIHmax	VILmin	VIHAmin	VILAmax	VEE	Gnd
Power Supply Drain Current -	1 _E	8	-	82	-	60	75		82	mAdc	-2	0-4	5-3-	14-	8	1,16
Input Current	linH	3,7,9,14 4,5,10,12 13	-	390 425 460	-	-	245 265 290	-	245 265 290	μAdc ▼	13	1 8-61 1 8-81 8-8		Special Specia	8	1,16
	linL		0.5	-	0.5		3-2	0.3	相景与	μAdc	- (0	4.6.4	3-7	- No.	8	1,16
Logic "1" Output Voltage	VOH	6	-1.060 -1.060	-0.890 -0.890	-0.960 -0.960	-	-0.810 -0.810	-0.890 -0.890	-0.700 -0.700	Vdc Vdc	3,13 7,13	18-A	2.8	#- 3- a	8	1,16 1,16
Logic ''0'' Output Voltage	VOL	2 6	-1.890 -1.890	-1.675 -1.675	-1.850 -1.850	=	-1.650 -1.650	-1.825 -1.825	-1.615 -1.615	Vdc Vdc	3,5 4,7	6-17 0-13	T.	12-1	8	1,16 1,16
Logic "1" Threshold Voltage	VOHA	2 6	-1.080 -1.080		-0.980 -0.980	3 -	-	-0.910 -0.910		Vdc Vdc	13 13	BC8	3 7	8	8 8	1,16 1,16
Logic "0" Threshold Voltage	VOLA	2 6	-	-1.655 -1.655	-	-	-1.630 -1.630	- 4	-1.595 -1.595	Vdc Vdc	13 13	10.0	9-8 9-4	3 7	8 8	1,16 1,16
Switching Times (50 \Omega Load)									3 5 5	3	+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay: Data Gate Clock	t3+2+ t5-2+ t13+2+	2 2 2 2	1.0	5.6 3.2 5.8	1.0	3.0 2.0 4.0	5.4 3.1 5.6	1.1 1.0 1.2	5.9 3.4 6.2	ns	8-16 5-16 15-16		3 5 13	2 2 2	8	1,16
Setup Time Hold Time	t3+13+ t13+3+	2	2.5	L-	2.5 1.0	_	1	2.5 1.0	- 1	6	313	13.8	2 3 25	5 m		
Rise Time (20% to 80%)	t ₂₊	2	1 1	3.6	1.1	2.0	3.5	1.1	3.8	(a)	32 234 3	4 5	3	2		
Fall Time (20% to 80%)	t ₂₋	2	A	3.6	1.1	2.0	3.5	1.1	3.8	-	57-9 1	3-9	3	2	\	

^{*}Individually test each input applying VIH or VIL to input under test.

MC10170

9 + 2-BIT PARITY GENERATOR-CHECKER

The MC10170 is a 11-bit parity circuit, which is segmented into 9 data bits and 2 control bits.

Output A generates odd parity on 9 bits; that is, Output A goes high for an odd number of high logic levels on the bit inputs in only 2 gate delays.

The Control Inputs can be used to expand parity to larger numbers of bits with minimal delay or can be used to generate even parity. To expand parity to larger words, the MC10170 can be used with the MC10160 or other MC10170's. The MC10170 can generate both even and odd parity.

P_D = 300 mW typ/pkg (No Load)

 $t_{pd} = 2.5 \text{ ns typ (Control Inputs to B Output)}$

4.0 ns typ (Data Inputs to A Output)

6.0 ns typ (Data Inputs to B Output)

 $t_{r,tf} = 2.0 \text{ ns typ } (20\%-80\%)$

MECL 10K SERIES

9 + 2-BIT PARITY GENERATOR-CHECKER



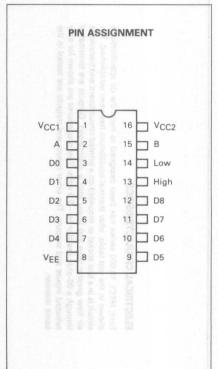
L SUFFIX CERAMIC PACKAGE CASE 620

P SUFFIX PLASTIC PACKAGE CASE 648



LOGIC DIAGRAM 13 High Control 15 B Inputs 14 Low Even Parity D0 3 D1 4 D2 5 D3 6 D4 D5 9 Odd Parity D6 10 D7 11 D8 12 - $V_{CC1} = Pin 1$ V_{CC2} = Pin 16 V_{EE} = Pin 8

INPUTS	OUT	PUTS
Sum of D Inputs	Odd Parity	Even Parity
at High Level	Output A	Output B
Even	Low	High
Odd	High	Low



		TEST V	OLTAGE VA	ALUES	6500
@ Test	1936		(Volts)		
Temperature	V _{IHmax}	VILmin	VIHAmin	VILAmax	VEE
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

										.00 C	-0.700	1.020	1.000	-1.440	0.2	
		Pin			MC	10170 Te	st Limits				TEST VOL	TAGE APP	LIED TO PI	NS LISTED E	BELOW:	
	- January	Under	-30	o°C		+25°C		+8	5°C					16 1		(VCC)
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	V _{IHmax}	VILmin	VIHAmin	V _{ILAmax}	VEE	Gnd'
Power Supply Drain Current	1E	8	-	78	1-	57	71	-	78	mAdc	-	-	- 8	2 =	-	1,16
Input Current	linH	3 5		350 350	- 85 - 79		200	- 6	22',	μAdc μAdc	3 5	-	- 8	3 2	8	1,16 1,16
	linL	3	0.5		0.5	-	0 - 1	0.3	- 8	μAdc	F	3	- 8	CO. To	8	1,16
Logic "1" Output Voltage	Vон	2 15	-1.060 -1.060	-0.890 -0.890	-0.960 -0.960	-	-0.810 -0.810	-0.890 -0.890	-0.700 -0.700	Vdc Vdc	3,4,5 14	- E	- 1	7.5	8	1,16 1,16
Logic "0" Output Voltage	VOL	2 15	-1.890 -1.890	-1.675 -1.675	-1.850 -1.850	-	-1.650 -1.650	-1.825 -1.825	-1.615 -1.615	Vdc Vdc	4,5 13,14	- E	_ 3	5 5	8	1,16 1,16
Logic "1" Threshold Voltage	Vона	2 15	-1.080 -1.080		-0.980 -0.980	-	1-1	-0.910 -0.910		Vdc Vdc		1 - 6	5 13	が見	8	1,16 1,16
Logic "0" Threshold Voltage	VOLA	2 15	-	-1.655 -1.655	- 1	-	-1.630 -1.630	-	-1.595 -1.595	Vdc Vdc		北北京	-3.0	5 13	8	1,16 1,16
Switching Times (50-ohm Load) Propagation Delay	0.17.75									- 6		0.00	Pulse In	Pulse Out	-3.2 V	+2.0 V
-=====================================	t13+15+ t14-15-	15 15	1.5	4.2	1.5	2.5	4.0	1.5	4.4	ns			13 14 3	15 15 2	-8	1,16
	t3+2- t3-15+	2 15	2.0 4.0	6.6 9.5	2.0 4.0	6.0	6.0 8.8	2.0 4.0	6.6 9.5	V	L FI 3	123	3	15	. 1	*
Rise Time (20% to 80%)	t ₂₊	2	1.5	4.3	1.5	2.0	3.9	1.5	4.3	ns	-	_	3	2	8	1,16
Fall Time (20% to 80%)	t ₂₋	2	1.5	4.3	1.5	2.0	3.9	1.5	4.3	ns		_	3_	2	8	1,16

MC10171

BINARY TO 1-4-DECODER (LOW)

The MC10171 is a binary coded 2 line to dual 4 line decoder with selected outputs low. With either E0 or E1 high, the corresponding selected 4 outputs are high. The common enable E, when high, forces all outputs high.

 $P_D = 325 \text{ mW typ/pkg (No Load)}$

 $t_{pd} = 4.0 \text{ ns typ}$

3

 t_r , $t_f = 2.0 \text{ ns typ } (20\%-80\%)$

MECL 10K SERIES

BINARY TO 1-4-DECODER (LOW)

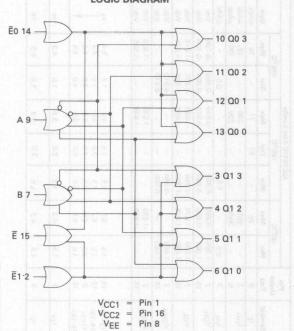


LSUFFIX CERAMIC PACKAGE CASE 620

P SUFFIX PLASTIC PACKAGE CASE 648

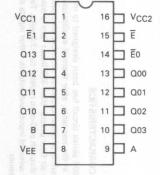


LOGIC DIAGRAM



TRUTH TABLE

ENA	BLE IN	PUTS	INP	UTS				OUT	PUTS			
Ē	ĒΟ	E1	A	В	Q10	Q11	Q12	Q13	000	Q01	Q02	Q03
L	L	L	L	L	L	Н	Н	Н	L	Н	Н	Н
L	L	L	L	Н	Н	L	Н	Н	Н	L	Н	Н
L	L	L	Н	L	Н	н	.L	Н	H	Н	L	Н
L	L	L	H	H	Н	Н	Н	L	Н	Н	Н	L
L	L	Н	L	L	Н	Н	Н	Н	L	Н	Н	Н
L	Н	L	L	L	L	Н	Н	Н	Н	Н	Н	Н
Н	φ	φ	φ	φ	Н	Н	Н	Н	Н	Н	Н	Н



Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to $-2.0\ volts$. Test Procedures are shown only for selected inputs and outputs. Other inputs and outputs are tested in a similar manner.

		TEST V	OLTAGE VAI	UES	199
@ Test			(Volts)	61.00 61.00	738
Temperature -30°C	VIHmax	VILmin	VIHAmin	VILAmax	VEE
+25°C	-0.890	-1.890	-1.205	-1.500	-5.2
+85°C	-0.810	-1.850	-1.105	-1.475	-5.2
T05 C	-0.700	-1.825	-1.035	-1.440	-5.2

											-0.700	-1.825	-1.035	-1.440	-5.2	
		Pin			N	1C1017	1 Test Li	imits			TEST VC	I TAGE APPI	IED TO PIN	S LISTED BE	LOW:	
		Under	-30	o°C		+25°C		+85	5°C		120, 10	ETAGE ATT		1 & 7		(VCC)
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	VIHmax	VILmin	VIHAmin	VILAmax	VEE	Gnd
Power Supply Drain Current	1E	8		85		65	77	E	85	mAdc	2,7,9,14,15	-	-	N X	8	1,16
Input Current	linH	14	100	350		-	220	4 - 5	220	μAdc	14	-	7.15		8	1,16
	linL	14	0.5	0 -	0.5	-	09 -	0.3	6	μAdc		14	- 1	10.0	8	1,16
Logic "1" Output Voltage	VOH	6	-1.060 -1.060	-0.890 -0.890	-0.960 -0.960	-	-0.810 -0.810	-0.890 -0.890	-0.700 -0.700	Vdc Vdc	15 15		5.5	유민	8	1,16 1,16
Logic "0" Output Voltage	VOL	13	-1.890	-1.675	-1.850	-	-1.650	-1.825	-1.615	Vdc	P - 10	2,7,9,14,15	- 1	LUL =	8	1,16
Logic "1" Threshold Voltage	VOHA	6 13	-1.080 -1.080	1/	-0.980 -0.980	=	L F	-0.910 -0.910	I I	Vdc Vdc	Ξ	7- 4	15 15	0 9	8	1,16 1,16
Logic "0" Threshold Voltage	VOLA	6	1.1.	-1.655 -1.655	1	-	-1.630 -1.630	1-1	-1.595 -1.595	Vdc Vdc	4.1	2,9,14,15 2,7,14,15	1	7 9	8	1,16 1,16
Switching Times (50 Ω Load)	1	13										+0.31 V	Pulse In	Pulse Out	-3.2 V	+2.0
Propagation Delay	t7+6+ t7-6-	6	1.5	6.2	1.5	4.0	6.0	1.5	6.4	ns	- B	2,9,14,15	7	6	8	1,16
	t7+13+ t7-13-	13 13	*	*	V	1		*	*		8 -	V		13 13	19	
Rise Time (20% to 80%) Fall Time (20% to 80%)	t6+ t13+ t6- t13-	6 13 6 13	1.0	3.3	1.1	2.0	3.3	1.1	3.4		-	2.5	a Villandia	6 13 6 13	15 AVA	

MC10172

DUAL BINARY TO 1-4-DECODER (HIGH)

The MC10172 is a binary-coded 2 line to dual 4 line decoder with selected outputs high. With either E0 or E1 low, the corresponding selected 4 outputs are low. The common enable E, when high, forces all outputs low.

PD = 325 mW typ/pkg (No Load)

 $t_{pd} = 4.0 \text{ ns typ}$

 t_r , $t_f = 2.0 \text{ ns typ } (20\%-80\%)$

MECL 10K SERIES

DUAL **BINARY TO 1-4-DECODER** (HIGH)

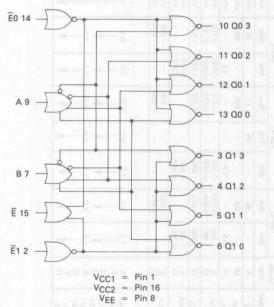
PLASTIC PACKAGE CASE 648

P SUFFIX



CERAMIC PACKAGE CASE 620

LOGIC DIAGRAM

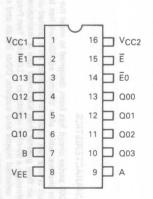


TRUTH TABLE

Ē	Ē1	Ē0	Α	В	Q1 0	Q1 1	Q1 2	Q13	Q0 0	Q0 1	Q0 2	Q0 3
L	Н	Н	L	L	Н	L	L	L	H	L	L	L
L	Н	Н	L	H	L	Н	BL 3	L.	L	Н	L	L
L	Н	Н	Н	L	L	L	Н	L	L	aL.	Н	L
L	Н	Н	H	н	L	L	L	H	L	L	L	Н
L	L	Н	L	L	L	L	L	L	Н	L	L	L
L	Н	L	L	L	н	L	L	L	L	E	L	L
Н	φ	φ	φ	φ	L	L	L	L	L	L	L	L

 $\phi = Don't Care$

3



Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to $-2.0\ volts$. Test procedures are shown only for selected inputs and outputs. Other inputs and outputs are tested in a similar manner.

		TEST V	OLTAGE VAI	LUES	1555
			(Volts)		1000
@ Test Temperature	VIHmax	VILmin	VIHAmin	VILAmax	VEE
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

	100	Pin			Mo	10172	Test Limit	s			TEST VI	OLTAGE APP	LIED TO PIN	SIISTED BE	OW:	
		Under	-30	o°C		+25°C		+8!	5°C		TEST VC	DETAGE AFF	LIED TO FIN	3 LISTED BE	LOW.	(VCC)
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	VIHmax	VILmin	VIHAmin	VILAmax	VEE	Gnd
Power Supply Drain Current	1E	8	-	85	-	62	77	-	85	mAdc	-	840	8.0-3.6	2 2 -	8	1,16
Input Current	linH	14	- 20	350	-	-	220		220	μAdc	14	3 5 5	8 8 -0 -	ā a-	8	1,16
	linL	14	0.5	-	0.5	-	8-	0.3		μAdc		14	23-5	2. 是-	8	1,16
Logic "1" Output Voltage	VOH	6 13	-1.060 -1.060	-0.890 -0.890	-0.960 -0.960	_	-0.810 -0.810	-0.890 -0.890	-0.700 -0.700	Vdc Vdc	2 14	133	2 5 3 8	1 5	8	1,16 1,16
Logic "0" Output Voltage	VOL	13	-1.890	-1.675	-1.850	-	-1.650	-1.825	-1.615	Vdc	15	2,7,9,14	0 2-03	9-9-	8	1,16
Logic "1" Threshold Voltage	VOHA	6 13	-1.080 -1.080	-	-0.980 -0.980			-0.910 -0.910	-	Vdc Vdc	=	8 2 3	2 14	图 图	8	1,16 1,16
Logic "0" Threshold Voltage	VOLA	6 13	1	-1.655 -1.655	-	=	-1.630 -1.630	_	-1.595 -1.595	Vdc Vdc		2,9,14 2,7,14	1235	7 9	8	1,16 1,16
Switching Times (50 Ω Load)	TT			H		TT	TI		100	1 98	+1.11 V	+0.31 V	Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t7+6- t7-6+	6	1.5	6.2	1.5	4.0	6.0	1.5	6.4	ns	2 2	9,14 9,14	§ 67-3 5	6	8	1,16
Rise Time (20% to 80%)	t7+13- t7-13+ t6+ t13+ t6-	13 13 6 13 6	1.0	3.3	1.1	2.0	3.3	1.1	3.4	A = 31	14 14 2 14 2	2,9 2,9 9,14 2,9	sinw een 662 shug 600 asuqi	13 13 6 13	815	
Fall Time (20% to 80%)	t13-	13		*	*	1	V		\ \		14	9,14	3 5 7 3	13		

QUAD 2-INPUT **MULTIPLEXER/LATCH**

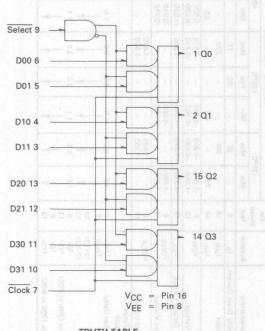
The MC10173 is a quad two channel multiplexer with latch. It incorporates common clock and common data select inputs. The select input determines which data input is enabled. A high (H) level enables data inputs D00, D10, D20, and D30 and a low (L) level enables data inputs D01, D11, D21, D31. Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information.

PD = 275 mW typ/pkg (No Load)

 $t_{pd} = 2.5 \text{ ns typ}$

 t_r , $t_f = 2.0 \text{ ns typ } (20\%-80\%)$

LOGIC DIAGRAM



TRUTH TABLE

	SELECT	CLOCK	Q0 _{n+1}
1	Н	L	D00
	L	L	D01
1	φ	Н	Q0 _n

 $\phi = Don't Care$

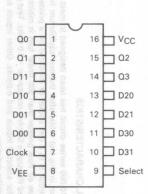
MECL 10K SERIES

QUAD 2-INPUT MULTIPLEXER/LATCH

> P SUFFIX PLASTIC PACKAGE **CASE 648**



CERAMIC PACKAGE CASE 620



Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

		TEST V	OLTAGE VA	LUES	
	100		(Volts)	lan.	(1) ·
@ Test Temperature	V _{IH} max	V _{IL min}	V _{IHA} min	VILA max	VEE
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

	TITLE	TTO		print.		- 4			5 M	.00	-0.700	1.025	1.000	1.440	36	
South Bank	had but	Pin	1-2 1-		٨		Test Lim		18 6		VOL1	AGE APPLI	ED TO PINS I	ISTED BELO	W:	1
	8 8	Under	-	0°C		+25°C		-	5°C					35	1	(Vcc
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	V _{IH} max	V _{IL} min	VIHA min	VILA max	VEE	Gnd
Power Supply Drain Current	1E	8	-	73	7 F		66	- 1	73	mAdc			-	S/cX	8	16
Input Current	linH	5	1	470			295	T "	295	μAdc	5				8	16
		6 7		470		-	295		295		6	manual la			-	-
		9		400			250 250		250 250	-	7 9		and the second		-	1
Input Leakage Current	linL	All	0.5	400	0.5		250	0.3	250	µAdc					8	16
	,,,,		0.0				Particular 1	0.0	Salar		Little Bill		II. I sum sin in			
Logic "1"	VOH	1	-1.060	-0.890	-0.960	-	-0.810	-0.890	-0.700	Vdc	6,9	7		8 8 8	8	16
Output Voltage		2	-1.060	-0.890	-0.960	10-	-0.810	-0.890	-0.700	Vdc	5	7	1000	9 9 8	8	16
Logic "0" Output Voltage	VOL	1 2	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615	Vdc	9	7		* 2 g	8	16 16
			-1.890	-1.675	-1.850	3.3	-1.650	-1.825	-1.615	Vdc		7		2 0 %	8	-
Logic "1" Threshold Voltage	VOHA	1 2	-1.080 -1.080	_	-0.980 -0.980		12	-0.910 -0.910		Vdc Vdc	9	7 7	6 5	0 2	8	16 16
Logic "O"	VOLA	1	- 2	-1.655		-	-1.630		-1.595	Vdc	9	7		6	8	16
Threshold Voltage		2	17	-1.655	-		-1.630	- 1	-1,595	Vdc		7	Production of the	5	- 8	16
Switching Times Propagation Delay								-	-		+1.11 Vdc	+0.31 Vdc	Pulse In	Pulse Out	-3.2 Vdc	+2.0 V
Data Input	t ₆₊₁₊	1	0.8	3.7	1.0	2.5	3.5	1.1	5.3	ns	9	7	6		8	16
Heleful Helef	t6-1-	1 =		-11		1	1			1	9	1 34 8	6	P # P	28 3	1
	t5+1+		1			-	1	0 4.0	1	0	8 1	1 0	5		311	
	t5-1-		1		7	Y		1		1	- E	0.0	5		San I	
Clock Input	t7-1+		1.6	7.2	1.6	4.5 4.5	6.8	1.4	6.8			5 5	5,7			
	t7-1-	1837	1.6	7.2	1.6		6.8	1.4	6.8	MIN THE	8 1	8 8			201	
Select Input	t9+1+	181	1.1	6.2	1.3	3.5	5.7	1.2	6.7		6 5	51 or	9	2 0 0	6	
	t9+1- t9-1+		10 4	44-4	+64-4		1				5	19 00	6 4 6	4 8 8	X 11	
	t9-1-	FIL									6	5 B	R 22		50	
Setup Time			V			A					-	200	+ 3	7 3 5	See 1	
Data Input	t _{setup}		2.0	1 - 1	2.0	1.5	300	2.0				- E-4	5,7	5.5.0	為一生	
Select Input	tsetup		3.0		3.0	2.5		3.0			6		7.9	n A 3	6	
Hold Time Data Input			2.5	11 1	2.5	0.0	hope of	2.5	4 1				6.7 8	5 8 5		
Select Input	thold thold		1.5	1 1	1.5	-0.5	1.5	1.5	k - 4		6		5,7 7,9	5 4 5		
Rise Time (20 to 80%)	t+	G.	1.2	4.0	1.5	2.0	3.5	1.4	4.0	(1)	5		7			
Fall Time (20 to 80%)	t-	+	1.2	4.0	1.5	2.0	3.5	1.4	4.0	*			7	t	+	+

^{*}VILmin applied to each input pin, one at a time.

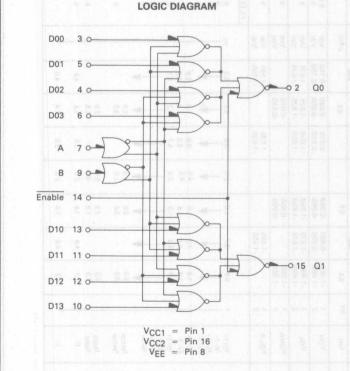
DUAL 4 TO 1 MULTIPLEXER

The MC10174 is a high speed dual channel multiplexer with output enable capability. The select inputs determine one of four active data inputs for each multiplexer. An output enable forces both outputs low when in the high state.

 $P_D = 305 \text{ mW typ/pkg (No Load)}$

tpd = 3.5 ns typ (Data to output)

 t_{r} , $t_{f} = 2.0 \text{ ns typ } (20\%-80\%)$



TRUTH TABLE

ENABLE	ADDRESS	SINPUTS	OUT	PUTS
Ē	В	Α	QO	01
Н	φ	φ	L	L
L	L	L	D00	D10
L	L	Н	D01	D11
L	Н	L	D02	D12
L	Н	Н	D03	D13

 $\phi = Don't Care$

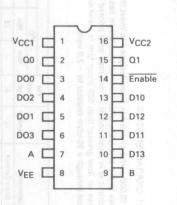
MECL 10K SERIES

DUAL 4 TO 1 MULTIPLEXER

P SUFFIX PLASTIC PACKAGE CASE 648



L SUFFIX CERAMIC PACKAGE CASE 620



Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established in an ambient temperature of 25° C, while the circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs tested in the same manner.

No. of the last		TEST V	OLTAGE VAL	LUES	
			(Volts)		. 3
@Test Temperature	V _{IH max}	VIL min	VIHA min	VILA max	VEE
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

											.00 0	-0.700	-1.023	-1.035	-1.440	-0.2	
Γ			n:			N	AC10174	Test Lin	nits						O LIOTED DE		
1		-	Pin Under	-30	o°C		+25°C		+85	5°C	1.1	TEST VC	DETAGE APP	LIED TO PIN	IS LISTED BE	LOW	(VCC)
	Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	VIH max	VIL min	VIHA min	VILA max	VEE	Gnd
1	Power Supply Drain Current	1E	8	-	80	-	58	73	80		mAdc	-	40, 41	5 (3-8	35-9 5	8	1,16
1	Input Current	lin H	4	-	350	-	-	220	-	220	μAdc	4	8	A B-6	53-18	8	1,16
1			14	_	525	-	-	330	-	330		14	-1	0_0_0	F E 3 F	8	1,16
1		Tin L	4	0.5	-	0.5	-	-	0.3	-47	μAdc	-	4	5-5	2 7-2 7-	8	1,16
	Logic ''1" Output Voltage	VOH	15	-1.060	-0.890	-0.960	-	-0.810	-0.890	-0.700	Vdc	13	33	3 3 6	2 5 3 5	8	1,16
-	Logic "0" Output Voltage	VOL	15	-1.890	-1.675	-1.850	-	-1.650	-1.825	-1.615	Vdc	14	- 音图	1 1 1	B # 8 B	8	1,16
	Logic ''1'' Threshold Voltage	Vона	15	-1.080	- 17	-0.980		61	-0.910		Vdc	8 8	48	13	8 - 2 - 5	8	1,16
-	Logic ''0'' Threshold Voltage	VOLA	15	0 0	-1.655	-		-1.630	133-	-1.595	Vdc	9-6	- 50	14	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	8	1,16
-	Switching Times (50 Ω Load)									T E	12	+1.11 V	1 8	Pulse In	Pulse Out	-3.2 V	+2.0 V
	Propagation Delay	t13+15+	15	1.4	5.0	1.5	3.5	4.7	1.4	5.0	ns	3 4	2.3	13	15	8	1,16
1		t13-15-	15	1.4	5.0	1.5	3.5	4.7	1.4	5.0	110	0 E	70 10	13	w 12 5	1	1
		t7+15-	15	1.9	6.6	2.0	5.0	6.2	2.1	6.6	1 100	11	-8	7	图 古 图 道		1.
1		t7-15+	.15	1.9	6.6	2.0	5.0	6.2	2.1	6.6		11	- 4 3	7	3 - 3 -	0 3	
I		t14+15-	15	1.0	3.3	1.0	2.0	3.1	0.9	3.4		13	-6 %	. 14	as 98 122 JF		
1	* * 31	t14-15+	15		3.3	1.0	2.0	3.1	0.9	3.4	1 %	E 9.	25, 12	14			3
1	Rise Time	t+	15		3.4	1.1	2.0	3.3	1.1	3.6	1 2	-		14	F 2 6 6		
1	(20% to 80%)	-10.00		- 100		69		103					# 2 8	H 90 5	R B B &		
1	Fall Time	t-	15		3.4	1.1	2.0	3.3	1.1	3.6			12 4 5	14	5 3V2 9		
1	(20% to 80%)	20181	2	- 52		. 32		17					233	8 5 5	3 2 2 3		

MC10175

QUINT LATCH

The MC10175 is a high speed, low power quint latch. It features five D type latches with common reset and a common two-input clock. Data is transferred on the negative edge of the clock and latched on the positive edge. The two clock inputs are "OR"ed together.

Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information. The reset input is enabled only when the clock is in the high state.

 $P_D = 400 \text{ mW typ/pkg (No Load)}$

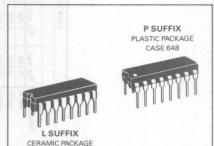
tpd = 2.5 ns typ (Data to Output)

 t_r , $t_f = 2.0 \text{ ns typ } (20\%-80\%)$

LOGIC DIAGRAM D0 10 -0 - 14 Q0 D1 12 -D 0 - 15 Q1 D2 13 -D 0 R D 0 D4 5. CO 6 -C1 VCC1 = Pin 1 Reset 11 -VCC2 = Pin 16 VEE = Pin 8 TRUTH TABLE CO D C1 Reset Q_{n+1} L L L φ L Н H L L φ Н φ L Qn H φ L Qn H H L 6 φ H L $\phi = Don't Care$

MECL 10K SERIES

QUINT LATCH



CASE 620

PIN ASSIGNMENT VCC1 1 16 VCC2 02 7 2 15 01 14 Q0 03 7 3 04 4 13 D2 12 D1 C0 6 11 Reset 10 D0 C1 7 9 D3

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown only for selected inputs and outputs. Other inputs and outputs are tested in a similar manner.

		TEST V	OLTAGE VA	LUES	1000
	10		(Volts)	74 E	1
@ Test Temperature	VIH max	VIL min	VIHA min	VILA max	VEE
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

	F	0:			N	1C10175	L Test Lim	its	0	This is			D TO BING I	ICTED DELC	MAI.	
		Pin	-30	о°С		+25°C		+8	5°C		VOLI	AGE APPLIE	DIOPINS	ISTED BELC	PVV:	
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	V _{IH max}	VIL min	VIHA min	VILA max	VEE	Gnd
Power Supply Drain Current	1E	8	-	107	-	78	97	_	107	mAdc	-	-	_	-	8	1,16
Input Current *	linH	6 7 10 11	-	460 460 460 1000		=	290 290 290 650		290 290 290 650	μAdc	6 7 10 11	=	1 1907 1 1 1007 1 1 1007	1000	1	1
Input Leakage Current	linL	All	0.5	-	0.5	-	-	0.3		μAdc	-	1	0.4	8 4-6	8	1,16
Logic "1" Output Voltage	VOH	14 15	-1.060 -1.060	-0.890 -0.890	-0.960 -0.960	_	-0.810 -0.810	-0.890 -0.890	-0.700 -0.700	Vdc Vdc	10 12	6			8	1,16 1,16
Logic "0" Output Voltage	VOL	14 15	-1.890 -1.890	-1.675 -1.675	-1.850 -1.850	_	-1.650 -1.650	-1.825 -1.825	-1.615 -1.615	Vdc Vdc	- 8	6,10 6,12	建重角		8	1,16 1,16
Logic "1" Threshold Voltage	VOHA	14 15	-1.080 -1.080	12	-0.980 -0.980	=	_	-0.910 -0.910		Vdc Vdc	安三 よ	6	10 12	613	8	1,16 1,16
Logic "0" Threshold Voltage	VOLA	14 15	_	-1.655 -1.655	-	_	-1.630 -1.630	-	-1.595 -1.595	Vdc Vdc	F= 4	6	1938	10 12	8	1,16 1,16
Switching Times				113					-34.3		+1.11 Vdc	+0.31 Vdc	Pulse In	Pulse Out	-3.2 Vdc	+2.0 Vdc
Data Input Clock Input	t10+14+ t10-14- t6-14+ t6-14-	14	1.0	3.6 3.6 4.7 4.7	1.0		3.5 3.5 4.3 4.3	1.0	3.6 3.6 4.4 4.4	ns	8-1-1	6.7 6,7 7 7	10 10 10,6 10,6	14	8	1,16
Reset Input	t11+4- t11+14-	4 14	1.0	4.0 4.0	1.0 1.0	=	3.9 3.9	1.0	4.2 4.2	ns †	5	6	7,11 7,11	4 ② 14 ②	8	1,16 1,16
Setup Time Hold Time	t _{setup}	14 14	2.5 1.5	E	2.5 1.5	_	L.	2.5 1.5	= 1	ns	1 1 2 4 9	7 7	6,10 6,10	14	8	1,16
Rise Time (20 to 80%)	t+	14	1.0	3.6	1.1	-	3.5	1.1	3.7		1 7 4 9	6,7	10	2 2 5	16	
Fall Time (20 to 80%)	t-	14	1.0	3.6	1.1	-	3.5	1.1	3.7	+	1 2 2	6,7	10	E 55 6	*	+

¹ Individually test each input; apply VIL min to pin under test.

² Output latched to high logic state prior to test.

HEX "D" MASTER-SLAVE FLIP-FLOP

The MC10176 contains six high-speed, master slave type "D" flip-flops. Clocking is common to all six flip-flops. Data is entered into the master when the clock is low. Master to slave data transfer takes place on the positive-going Clock transition. Thus, outputs may change only on a positive-going Clock transition. A change in the information present at the data (D) input will not affect the output information any other time due to the master-slave construction of this device.

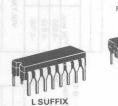
PD = 460 mW typ/pkg (No Load)

f_{toggle} = 150 MHz (typ)

 t_r , $t_f = 2.0 \text{ ns typ } (20\%-80\%)$

MECL 10K SERIES

HEX "D" MASTER-SLAVE FLIP-FLOP



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

LOGIC DIAGRAM D1 6 3 Q1 4 02 D3 10 13 Q3 D4 11 14 Q4 D5 12 15 Q5 **CLOCKED TRUTH TABLE** $V_{CC1} = Pin 1$ C D Q_{n+1} VCC2 = Pin 16 φ Q_n VEE = Pin 8 H* L H* H H $\phi = Don't Care$ *A clock H is a clock transition from a low to a high state.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one data input, and the clock input, and for one output. Other inputs and outputs tested in the same manner.

		TEST V	OLTAGE VA	LUES	61
	The second second second	151	(Volts)	20	100
@Test Temperature	VIHmax	VILmin	VIHAmin	V _{ILA max}	VEE
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

шш	HU	Pin	J U	ш	MC10176	Test Li	mits				TEST VO	LTAGE APPI	LIED TO PIN	S LISTED BE	LOW:	
	E &	Under		o°C		+25°C			5°C				1	5		(Vcc
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	VIHmax	VILmin	VIHAmin	VILAmax	VEE	Gnd
Power Supply Drain Current	1E	8	-	121	-	88	110	-	121	mAdc	-	-		-	8	1,16
Input Current	linH	5	-	350	-	-	220	-	220	μAdc	5		-		8	1,16
		9	-	495	-	-	310	-	310		9	-	-	-	8	1,16
Input Leakage Current	rinL	5	0.5	_	0.5	_	111	0.3		μAdc		5	-	-	8	1,16
		9	0.5	-	0.5	-	1-1-	0.3	-	μAdc	-	9	1898		8	1,16
Logic "1"	VOH	2†	-1.060	-0.890	-0.960	1 2 6	-0.810	-0.890	-0.700	Vdc	5	9 2 3	3 3.3	2 3 3	8	1,16
Output Voltage	011	15†	-1.060	-0.890	-0.960	-	-0.810	-0.890	-0.700	Vdc	12	3 2 5	1 1 1 - 5	9 5 3-	8	1,16
Logic "0"	VOL	2†	-1.890	-1.675	-1.850	_	-1.650	-1.825	-1.615	Vdc		5	1 2 0 0		8	1,16
Output Voltage		151	-1.890	-1.675	-1.850	-	-1.650	-1.825	-1.615	Vdc	- 1	12	# R-E		8	1,16
Logic "1"	VOHA	2†	-1.080	_	-0.980		1 -8	-0.910	8 8	Vdc	- 3	9 2 7	5	4 2 2	8	1,16
Threshold Voltage	A A	15t	-1.080	1	-0.980	-	- 3	-0.910	5 5	Vdc	-	見 み きょ	12	m 01 SF	8	1,16
Logic "0"	VOLA	2†	- /	-1.655	0	8-	-1.630	3-5	-1.595	Vdc		9 5 6 1	22.5	5	8	1,16
Threshold Voltage		15†	- 4	-1.655		50-	-1.630	12- 2	-1.595	Vdc	9	E = 9	1 2 2 4	12	8	1,16
Switching Times						1	1 3	8 4	7 8	5 9	+1.11 Vdc	+0.31 Vdc	Pulse In	Pulse Out	-3.2 Vdc	+2.
Clock Input ** Progagation Delay						12	11 3	- 0	w 6	- A- A	9 1	5 8 8	5.9	2	8	1,16
1 Togagation Delay	t9+2+	2 2	1.6 1.6	4.6	1.6	2	4.5	1.6	5.0	ns	8 7 8	46.	5,9	9 9 7	°	17"
Rise Time (20 to 80%)	t9+2- t2+	2	1.0	4.6	1.6 1.1	9	4.5	1.6	5.0	18 2	77	8 5 0	0 8 9	3 9 3	8 3	11
Fall Time (20 to 80%)	t2-	2	1.0	4.1	1.1	-	4.0	1.1	4.4	1 m	6 1		1 8 8 8	5 5 8	24	
7 all 1 line (20 to 00%)	12-	-	1.0	4.1	1.1		4.0	1.1	3	1315	2 0	3 8 8 4	1	- 21	1	1
Setup Time	t _{setup}	2	2.5	DF 534	2.5	-	1-3	2.5	34	ns	- 3	2 2 3	5.9	2	8	1,1
Hold Time	thold	2	1.5	-	1.5	-	1-	1.5	0 3	ns	5 - 9	State of the state	5,9	2 2	8	1,1
Toggle Frequency	f _{tog}	2	125	_	125	150	_	125	_	MHz	- 0	1	1 1 2 3	2 6 4	8	1,1

 $[\]uparrow$ Output level to be measured after a clock pulse has been applied to C input (pin 9) \hfill VIH max VIL min

TRIPLE MECL TO **NMOS TRANSLATOR**

The MC10177 consists of three MECL to MOS translators which convert MECL 10,000 logic levels to NMOS levels. It is designed for use in N-channel memory systems as a Read/Write, Data/Address driver. It may also be used as a high fanout (30) MECL to TTL translator, or in other applications requiring the capability to drive high capacitive loads. A separate lead from each of the three translators is brought out of the package. These leads may be connected to VSS or to an external capacitor (0.01 to 0.05 μF to ground), for waveform improvement, and short circuit protection. When connection is made to an external capacitor, VSS line fluctuations due to transient currents are also reduced.

Max Load: 350 pF

3

 $P_D = 1.0 \text{ W typ/pkg} @ 5.0 \text{ MHz}$ Operating rate: 5.0 MHz typ.

(all 3 translators in use simultaneously)

INPUT: MECL 10,000 (differential) OUTPUT: NMOS + 0.5 V VOLmax + 3.0 V VOHmin*

 t_r , $t_f = 6.0 \text{ ns typ } (20\%-80\%)$

*May be raised by increasing VSS.

MECL 10K SERIES

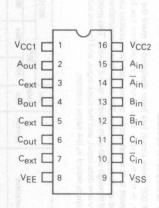
TRIPLE MECL TO **NMOS TRANSLATOR**



P SUFFIX PLASTIC PACKAGE CASE 648



PIN ASSIGNMENT



LOGIC DIAGRAM

V_{CC} = Gnd = Pins 1, 16

 $V_{EE} = Pin 8 = -5.2 Vdc \pm 5\%$

 $V_{SS} = Pin 9 (+5.0 Vdc or +6.0 Vdc \pm 10\%)$

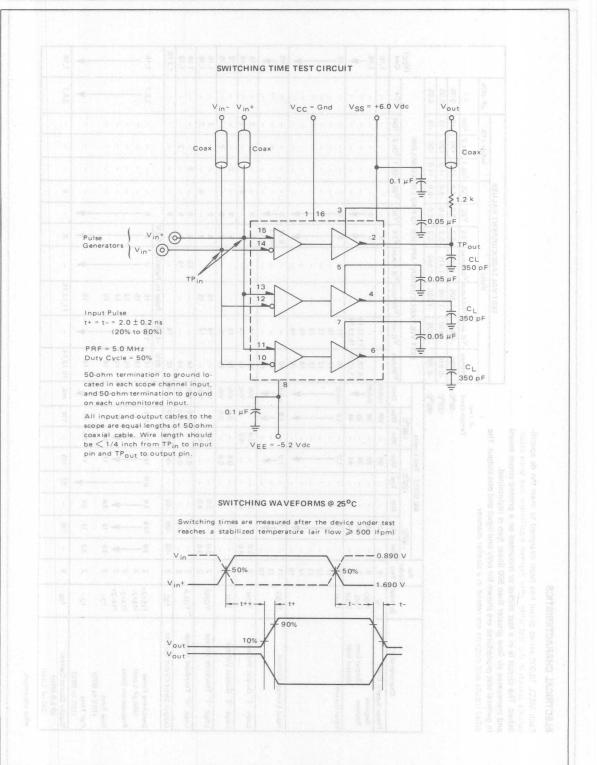
Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. In general test procedures are shown for only one input and one output. The other inputs and outputs are tested in a similar manner.

TEST VOLTAGE/CURRENT VALUES μF ±5% Volts mAdc ±1% @ Test VIHmax VSC VSS IOL1 IOL2 IOH C# V_{ILmin} VIHAmin VILAmax VEE Temperature -30°C -0.890 -1.890 -1.205 -1.500 -5.2 +5.0 +6.0 +1.0 +20 0.05 +25°C -0.810 -1.850 -1.105 -1.475 | -5.2 | +5.0 | +6.0 | +1.0 | +20 0.05

	المراكب سا	Like '		of Line					+8	35°C	-0.700	-1.825	-1.035	-1.440	-5.2	+5.0	+6.0	+1.0	+20	-15	0.05	
		Pin			MC1	0177	Test L	-			TE	STVOLT	AGE/CUR	RENT APP	LIED	TOPIN	VS LIS	TED B	ELOW			
	1.0	Under		0°C		+25°C		-	5°C												2	(Vcc
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	VIHmax	VILmin	VIHAmin	VILAmax	VEE	V _{SC}	VSS	OL1	IOL2	IOH	C#	Gnd
Power Supply Drain	1E	8	o-	106	-	-	96	-	106	mAdo	T = 11			-	8	-	-	-		-	W -	1,16
Negative	Isso	9	-	88	-	-	88	-	88	mAdo		-	L Fa	(8	9	-	-	-	-	y =	1,16
Positive Output Low	ISSL	9	1	88	-	-	88	-	88	1		11,13,15	- 7	4			-	-	-	-	N -	
Output High	ISSH	9	-	44	- 3	-	44	-	44		11,13,15	10,12,14	12	3 /	V	V	-	-	-	-	4 -	
Input Current	linH	10	-	1.6	-	-	1.0	-	1.0	mAdc	10	11	1 - 1	/	8	9.	-	-	-			1,16
		11	-	3	-2	-		-			11	10	-	-50			-		-	-	(g. =)	133
	100	12	1-	100	- 20	-		-			12	13	-	- 7		11 1		-	1/2	-	0 -	18
	1000	13	-	2 5	-	-		W -			13	12	-	1		1	-	-	-	=0	Jr - J	1 25
		14	-	-	1	-	-	2-	1		14	15	- 75		1		-	-	V-	-	3 -	V
		15	11-		-	-	,	0-		V	15	14	1-1	- /		1	-	-	-	-	K -	٧.
Input Leakage Current	CBO	11	-	1.5	71	-	1.0	7-	1.0	μAdc	10	V -	/ - N	-7	8,11	9	-	-	-	-		1,16
		13	-	1	-	-	1	-	1		12		0-1	- "10	8,13	I	-	-	7	-	-1	
		15	-	V	28	-		-	V		14	2 -	De m	- 1	8,15				1	-	-	65 V
Logic "1" Output Voltage	VOH	2	3.0	-	3.0	-	-	3.0	-	Vdc	15	14			8	9	-		1	2	2 -	1,16
	- 9	2	4.0	-	4.0	-	-	4.0	-2	Vdc	15	14		- 1	8	- "	9	-	-	2	1 - 1	1,16
Logic "0" Output Voltage	VOL	2	-	0.5	-	-	0.5	-	0.5	Vdc	14	15	1-	7-2-3	8	9	-	2	-	-	131-13	1,16
		2	-	0.6	-	-	0.6	-	0.6	Vdc	14	15	-		8	9	-	1-0	2	-9	8 -	1,16
Logic "1" Threshold Voltage	VOHA	2	3.0	2-3	3.0	-	-	3.0	-	Vdc	-	14	15	# 1	8	9	-	-	+	2	A-11	1,16
		2	4.0	5-3	4.0	-	-	4.0	-	Vdc	- I	14	15	100	8	-	9	-	-	2	-	1,16
Logic "O" Threshold Voltage	VOLA	2	1-	0.5	-	-	0.5		0.5	Vdc	14	-		15	8	9	-	2	-	-	-	1,16
		2	-	0.6	-	-	0.6	-1	0.6	Vdc	14	-	-	15	8	9	-	-	2	-		1,16
Output Short-Circuit Current	1sc	2	-50	-90	-50	-	-90	-50	-90	mAdo	15	14	-	- /	8	9	-	-	-	-	-	1,2,16
							- 6		13	100	-1.29 V	-1.69 V	Pulse In	Pulse Out	-5.2 V	,						
Switching Times	t15+2+	2	2.0	12.5	2.0	6.0	12.5	2.0	12.5	ns	14	11,13	15	2	8	9	-		_	_	3.5.7	1,16
(350 pF Load)	t15-2-	2	11	1	1	1			1	1	14	1.5	15	1 9		1	-	-	_	-	1	1
Propagation Delay	t14+2-	2				17	15	3 8		B 1 8	15	1 6	14	-	-		1	-	-	-		
· · · · · · · · · · · · · · · · · · ·	t14-2+	2	4	-	-		4	-	W	8 1 1	15	P. 10.	14				-		_	_		1 1
Rise Time	1 2 2	2	3.0	12	3.0		11	3.0	11		14		15						-	_		1 1
(10% to 90%)	t ₂₊	2	3.0	12	3.0		112	3.0	-		14		15		8			_	-			
Fall Time (10% to 90%)	t ₂₋	2	3.0	12	3.0	*	11	3.0	11		14	¥ 22	15	*	V	*	-	-	-		*	*
Supply Source Current (@ 5.0 MHz) (350 pF Load)	ISS	9	-	110	-	83	110	-	110	mA	10,12,14	-	11,13,15	-	8	-	9	-	-	1-1	3,5,7	1,16

#See test circuit.





MOTOROLA

BINARY COUNTER

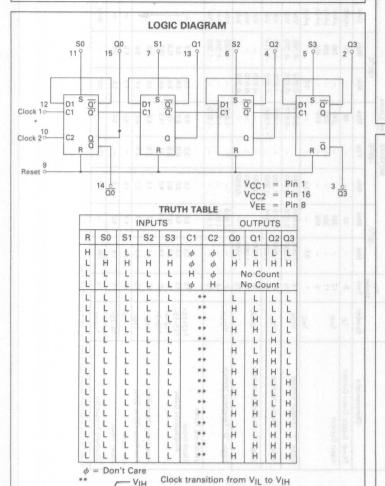
The MC10178 is a four-bit counter capable of divide-by-two, divide-by-four, divide-by-eight or a divide-by-sixteen function.

Clock inputs trigger on the positive going edge of the clock pulse. Set and Reset inputs override the clock, allowing asynchronous "set" or "clear." Individual Set and common Reset inputs are provided, as well as complementary outputs for the first and fourth bits. True outputs are available at all bits.

PD = 370 mW typ/pkg (No Load)

f_{toggle} = 150 MHz (typ)

 t_r , $t_f = 2.7$ ns typ (20%–80%)



MECL 10K SERIES

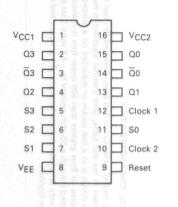
BINARY COUNTER

P SUFFIX PLASTIC PACKAGE CASE 648



L SUFFIX CERAMIC PACKAGE CASE 620 CASE 048

PIN ASSIGNMENT



3-137

may be applied to C1 or C2 or both

for same effect.

VIL-

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to $-2.0\ volts$. Test procedures are shown for only selected inputs and outputs. Other inputs and outputs tested in the same manner.

		TEST V	OLTAGE	/ALUES	
			(Volts)		14
@ Test Temperature	VIHmax	VILmin	VIHAmin	VILAmax	VEE
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Market State Company of the Company										+85°C	-0.700	-1.825	-1.035	-1.440	-5.2	. 3 7
		Pin		0-	M	C10178	Test Limit		-0-				LTAGE AP)	HL
		Under	-30	o°C		+25°C		+85	5°C			PINS	LISTED BE	LOW:		(VCC)
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	VIHmax	VILmin	VIHAmin	VILAmax	VEE	Gnd
Power Supply Drain Current	1E	8	-	97	017	_	88	-	97	mAdc	9	-	-	-	8	1,16
Input Current	linH	12 11	-	390 350		-1	245 220	70 -	245 220	μAdc	12	-	8 8	1 5	8	1,16 1,16
		9		650		_	410	-1	410	μAdc	9	4		8 8 8	8	1,16
	linL		0.5	- 3	0.5	-		0.3	100	μAdc			8.8	0 2 3	8	1,16
Logic "1" Output Voltage	VOH	14	-1.060	-0.890	-0.960	-	-0.810	-0.890	-0.700	Vdc	9	-	9.0	g. 4.3	8	1,16
the second of th		15	-1.060	-0.890	-0.960	-	-0.810	-0.890	-0.700	Vdc	- 11	-	5.5	353	8	1,16
Logic "0" Output Voltage	VOL	14	-1.890	-1.675	-1.850	_	-1.650	-1.825	-1.615	Vdc	11	-	B B B	10 - 15	8	1,16
	OL.	15	-1.890	-1.675	-1.850	-	-1.650	-1.825	-1.615	Vdc	9	9 -	6.3	P & D	- 8	1,16
Logic "1" Threshold Voltage	VOHA	- 3	-1.080		-0.980			-0.910	-	Vdc	意-	0 -	5	新华夏	8	1,16
		14	-1.080	-	-0.980	-	-cald	-0.910	-	Vdc	65-	75	11	2 -	8	1,16
the same of a comment of the comment of the	T 4 T	15	-1.080	17-1	-0.980	- 5	-	-0.910		Vdc		-	9	6 5 0	8	1,16
Logic "0" Threshold Voltage	VOLA	3	- 1	-1.655	- 1	-	-1.630		-1.595	Vdc	·	2 -	0 = X	5	8	1,16
		14	a ē 18	-1.655			-1.630		-1.595	Vdc	16-6	5 -	D 5.00	11	8	1,16
		15	- 13	-1.655		-	-1.630		-1.595	Vdc	7 -10	2 -	京 田 田	9	8	1,16
Switching Times	4 4 4 5	100-								150	15 4	150	Pulse In	Pulse Out	-3.2 Vdc	
Clock Input	t12+15+	15	1.4	5.0	1.5	3.5	4.8	1.5	5.3	ns	8-2	3 -	12	15	8	1,16
Propagation Delay	t12-13-	13	1.9	9.4	2.0	6.0	9.2	2.0	9.8	100	- 50	Q -	7 3 2	13		
	t12+4-	4	2.9	12.3	3.0	8.5	12	3.0	12.8		- 10	100 -	是自己	4	2 5	
	t12-3+	3	3.9	14.9	4.0	11	14.5	4.0	15.5	18 11 1	-	-	5 1	3	7 8	
Rise Time (20 to 80%)	t 15+	15	■ 1.1	4.7	1.1	2.5	4.5	1.1	5.0	-	- "	-		15	S V 8	
Fall Time (20 to 80%)	t15-	15	1.1	4.7	1.1	2.5	4.5	1.1	5.0	V	7	P '	70 10 0	15		
Set Input	t11-15+	15	1.4	5.2	1.5	-	5.0	1.5	5.5	ns	-	-	9 11	15	8	1,16
Reset Input	t9-15+	15	1.4	5.2	1.5	-5.	5.0	1.5	5.5	ns	-200	-	9	15	8	1,16
Counting Frequency	fcount	15	125		125	150		125	-	MHz	-	-	12	15	8	1,16

^{*}Individually test each input applying VIL to input under test.



MOTOROLA

LOOK-AHEAD CARRY BLOCK

The MC10179 is a high speed, low power, standard MECL complex function that is designed to perform the look-ahead carry function. This device can be used with the MC10181 4-bit ALU directly, or with the MC10180 dual arithmetic unit in any computer, instrumentation or digital communication application requiring high speed arithmetic operation on long words.

When used with the MC10181, the MC10179 performs a second order or higher look-ahead. Figure 2 shows a 16-bit look-ahead carry arithmetic unit. Second order carry is valuable for longer binary words. As an example, addition of two 32-bit words is improved from 30 nanoseconds with ripple-carry techniques. A block diagram of a 32-bit ALU is shown in Figure 1. The MC10179 may also be used in many other applications. It can, for example, reduce system package count when used to generate functions of several variables.

PD = 300 mW typ/pkg (No Load)

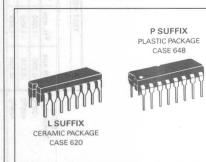
tpd = 3.0 ns typ (Carry, Propogate)

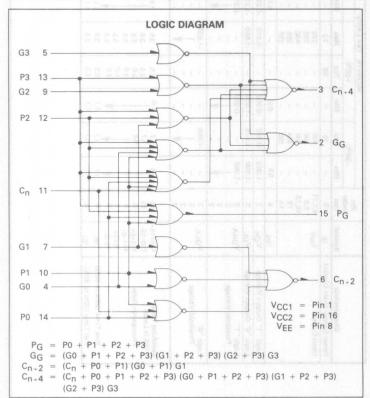
4.0 ns typ (Generate)

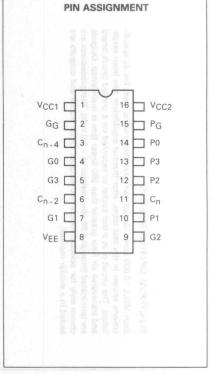
 t_r , $t_f = 2.3$ ns typ (20%–80%)

MECL 10K SERIES

LOOK-AHEAD CARRY BLOCK





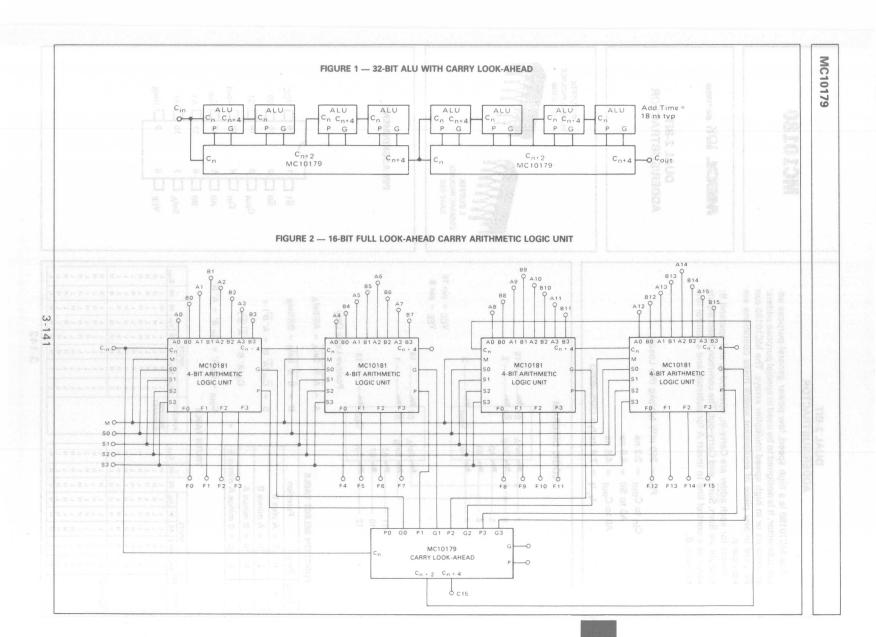


Each MECL 10,000 series device has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to $-2.0\,$ volts. Test procedures are shown only for selected inputs and outputs. Other inputs and outputs are tested in a similar manner.

	1000	TEST V	OLTAGE VA	LUES	1 13
	000		(Volts)	52	19
@ Test Temperature	VIH max	VIL min	VIHA min	VILA max	VEE
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

		Pin			N	1C10179	Test Limi	ts			TEST VO	TAGE API	PLIED TO PIN	IS LISTED BE	LOW:	
	170	Under	-3	0°C	7	+25°C		+85	5°C		1201 10	LIAUL AII	EIED IOIII			(Vcc)
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	VIH max	VIL min	VIHA min	VILA max	VEE	Gnd
Power Supply Drain Current	1E	8	-	79	-	58	72	-	79	mAdc	-5 9	75-	W =	1853	8	1,16
Input Current	linH	4,7,11 5,9 10,13 12 14	-	430 360 700 630 565			270 225 440 395 355	=	270 225 440 395 355	μAdc	4,7,11 5,9 10,13 12 14	ns pucho Parafipis na mosq	Hotel spirit	o pasks	8	1,16
	linL	4	0.5	-	0.5		-	0.3	-	иAdc	-3.9	4	- 6 2 9	525	8	1,16
Logic "1" Output Voltage	VOH	2	-1.060	-0.890	-0.960	-	-0.810	-0.890	-0.700	Vdc	4,5,7,9	4 4 6	15 7 00	8 2 2	8	1,16
Logic "0" Output Voltage	VOL	3	-1.890	-1.675	-1.850	-	-1.650	-1.825	-1.615	Vdc	10 12	E 1- 5	0 5 5	9.29	8	1,16
Logic "1" Threshold Voltage	VOHA	2 2 2 2	-1.080	-	-0.980	-		-0.910	Columbia Columbia	Vdc	13 5,12 5,9 5	Hales	5 9 12 13	Age 191	8	1,16
Logic "0" Threshold Voltage	VOLA	2 2 2 2	1	-1.655	=	=	-1.630	-	-1.595	Vdc	13 5 5 5,9		Burnel Burnel	5 13 9	8	1,16
8							1 8	114	do ter do	100	+1.11 V	二 8 增。	Pulse In	Pulse Out	-3.2 V	+2.0 V
Switching Times (50 Ω Load) Propagation Delay Rise Time (20% to 80%)	t10+15+ t10-15- t11+6+ t11-6- t5+2+ t5-2- t6+	15 15 6 6 2 2 6	1.0	3.7 3.7 5.8	1.0	2.5 2.5 3.0 3.0 4.0 4.0	3.5 3.5 5.5 5.5 5.5 5.5 5.5	1.0 	3.9 3.9 6.1	ns Q	4.7 4.7 4.7 4.7 4.7,9 4.7,9	nisona na aA lab adobada 105 Irodo A 160-538 a to ma	10 10 11 11 5 5	15 15 6 6 2 2	8	1,16
Fall Time (20% to 80%)	t6-	6	1.1	3.7	1.1	2.5	3.5	1.1	3.9		4,7	를 무용	11 🖂	6		

3-140



Inputs for each adder are Carry-in, operand A, and operand B; outputs are Sum, Sum, and Carry-out. The common Select inputs serve as a control line to invert A for subtract, and a control line to invert B.

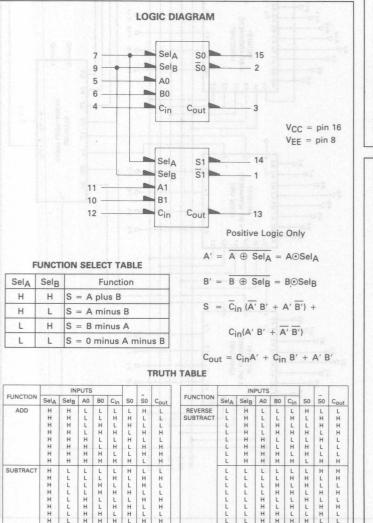
P_D = 360 mW typ/pkg (No Load)

 C_{in} to $C_{out} = 2.2$ ns

A0 to S0 = 4.5 ns

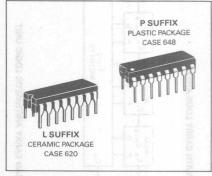
A0 to $C_{out} = 4.5 \text{ ns}$

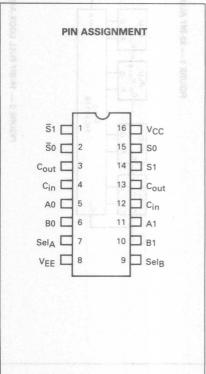
 $t_r t_f = 2.4 \text{ ns typ } (20\%-80\%)$



MECL 10K SERIES

DUAL 2-BIT ADDER/SUBTRACTOR





LHLHLL

Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

		750711	01 7405 1/4	· COED	_
		IESI V	OLTAGE VA Volts	LUES	- 6
@ Test Temperature	V _{IH} max	V _{IL min}	VIHA min	VILA max	VEE
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

		Pin			M	C10180	Test Limit	ts			TEST VO	L TAGE APP	LIED TO PIN	S LISTED BE	LOW:	
		Under	-30	o°C		+25°C		+85	5°C	7500				100		(VCC)
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	V _{IH} max	VIL min	VIHA min	VILA max	VEE	Gnd
Power Supply Drain Current	IE	- 8		95		70	86	1 + 1	95	mAdc			- 1	-	8	16
Input Current	linH	4		590		1121	370	-	370	μAdc	4	-	-	-	8	16
		5	-	350	1	_	220		220		5	200		_		
		6		350	-		220	1 1	220		6			2 20		
	100	7	1 to 4	460	-	-	290		290		7					
		9		460	-		290	I	290	2010	9	No. of the same	Car to a	on The sale		
		10	-	350	- T	-	220	1 1	220		10	3.2	3 2 9	B 5 9		
فالدخالة سيفاسيا المفاكر المسا		11		350			220	-	220		11 7	E 2 3	4 7 2	20 m 10		
		12	-	590	-	100	370	+ -	370	1	12	1. 4. 8.	3 2 3	729	1	1
	linL	All	0.5	의왕점	0.5	-	-	0.3	-	μAdc	-9 bi	7 2 3	0 4 1	6 8 8	8	16
Logic "1"	Vон	2	-1.060	-0.890	-0.960	-	-0.810	-0.890	-0.700	Vdc	7.9	100		- 4 O	8	16
Output Voltage	1 5 4	3	-1.060	-0.890	-0.960	_	-0.810	-0.890	-0.700		4,5,7,9	E 77 1	5 2 0	16 基 出		-11
	1-851	15	-1.060	-0.890	-0.960	_	-0.810	-0.890	-0.700	*	4,7,9	- 7 1	1 2 2 5	8 9 2	*	*
Logic "0"	VOL	2	-1.890	-1.675	-1.850	_	-1.650	-1.825	-1.615	Vdc	5,7,9	11 12 12 13	1 4 5	220	8	16
Output Voltage	1	3	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615	8	7,9	12 8 9		S 4 8	900	1
11411 1111	1 531	15	-1.890	-1.675	-1.850	-	-1.650	-1.825	-1.615	*	7,9	2 2 2	5 5 7	822	1	*
Logic "1"	VOHA	2	-1.080	17 4 1	-0.980	-	-	-0.910	100 miles	Vdc	7,9	2- 0 P	TW S S	4	8	16
Threshold Voltage		3	-1.080	-	-0.980		- 23	-0.910	_		4,7,9	2 3 4	5	07 4 6		
REAL REPORTS		15	-1.080	h	-0.980	-	- 5	-0.910	307	1	7,9	E 3 8	4		1	
Logic "0"	VOLA	2	0 Po	-1.655	2 2 0	TE S	-1.630	11 1 7	-1.595	Vdc	7,9	- 1 3 B	4	A - 2	8	16
Threshold Voltage		3	20, 701	-1.655		-	-1.630	14 4 22	-1.595		7.9	0.0	1 0 8	4	1 400	100
		15	-	-1.655	- 86	d	-1.630	1 + 34	-1.595	V	4,7,9	2.2.1	5	F F 5	1 5	
Switching Times Propagation Delay	100					·		1 6	551	125	+1.11 V	4 2 9	Pulse In	Pulse Out	-3.2 V	+2.0 \
Operand Input	t5+15+	15	1.3	5.8	1.3	16	5.4	1.1	5.8	ns	7.9	259	5	15	8	16
oparano mpar	t6+15+	15	1.3	5.8	1.3		5.4	1.1	5.8		7.9	EL mi	6	15	1	I
a atual frag	1000000	15	1.0	3.4	100000000000000000000000000000000000000	P 4 7 .		D- 00.			7,9	E 2 :	2 2 3	15	11 11	1.6
Carry-in Input	t4+15+	3	1.0	3.4	1.0	1 -	3.3	0.9	3.6	Seed 1		7-25	4	3	1 10	7
	t4+3+	201	1000	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1000	1 1	3.3	0.9	10000	基 岛	5,7,9	15 70 8	3 4 5	W. Herning	A 40	
Select Input	t7+15+	15	1.3	5.8	1.3	1 1	5.4	1.1	5.8	27 30	4,9	L. I 97 9	378	15	100	1
	t9+15+	15	1.3	5.8	1.3	57.0	5.4	1.1	5.8		7,4	医肝造成	9	2 9 T C	79	
Rise Time (20 to 80%)	t ₁₅₊	15	1.0	3.8	1.1	-	3.7	1.1	3.9		7,9	THE ST	5	2 2 3		
Fall Time	t15-	15	1.0	3.8	1.1	_	3.7	1.1	3.9	V	7.9	3 4 5 4	5	7 10	V .	V
	,15-		1.0	0.0	15.7		0.7	100	0.0	,	1,0			27.2	,	

^{*}Individually apply VIL min to pin under test.

MC10181

3

4-BIT ARITHMETIC LOGIC UNIT/FUNCTION GENERATOR

The MC10181 is a high-speed arithmetic logic unit capable of performing 16 logic operations and 16 arithmetic operations on two four-bit words. Full internal carry is incorporated for ripple through operation.

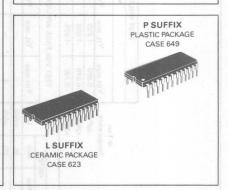
Arithmetic logic operations are selected by applying the appropriate binary word to the select inputs (S0 through S3) as indicated in the tables of arithmetic/logic functions. Group carry propagate (PG) and carry generate (GG) are provided to allow fast operations on very long words using a second order look ahead. The internal carry is enabled by applying a low level voltage to the mode control input (M).

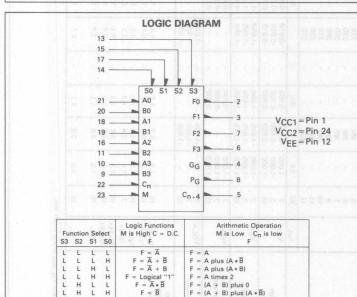
When used with the MC10179, full-carry look-ahead, as a second order look ahead block, the MC10181 provides high speed arithmetic operations on very long words.

> $P_D = 600 \text{ mW typ/pkg (No Load)}$ t_{pd} (typ): A1 to F = 6.5 ns C_n to $C_{n+4} = 3.1$ ns A1 to $P_G = 5.0$ ns A1 to $G_G = 4.5 \text{ ns}$ A1 to $C_{n+4} = 5.0$

MECL 10K SERIES

4-BIT ARITHMETIC LOGIC UNIT/FUNCTION GENERATOR





 $F = A \odot B$ $F = A + \overline{B}$ $F = \overline{A} \circ B$

 $F = A \oplus B$ F = B

F = A + B

F = Logical "0" $F = A \cdot \overline{B}$

F = A • B F = A

н Н

H

Н

H

Н

Н

TITITITI

F = A plus B F = A plus (A + B) $F = (A + \overline{B}) plus 0$

F = A minus B minus 1 $F = (A + \overline{B}) \text{ plus } (A \cdot B)$

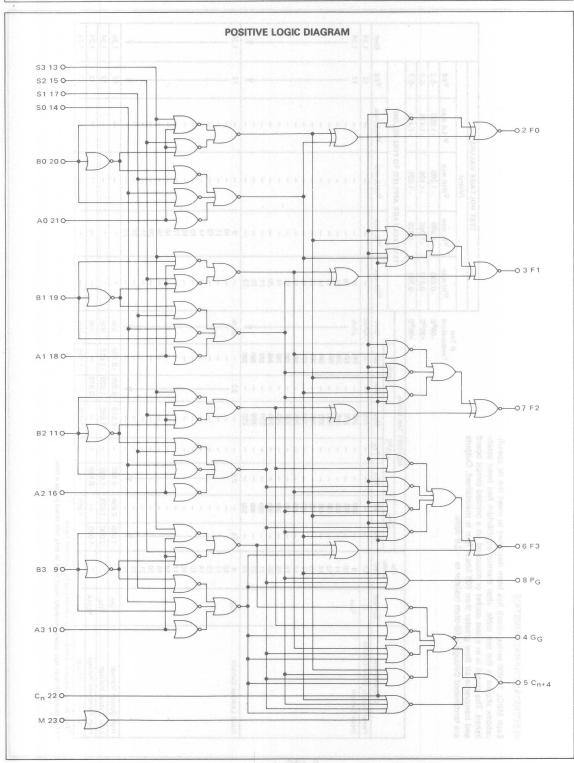
F = minus 1 (two's complement)

= A plus (A + B)

 $F = (A \circ \overline{B}) \text{ minus } 1$

F = (A · B) minus 1 F = A minus 1

		T.	ii d
V _{CC1}	1	24	VCC2
F0	2	23	M
F1 _	3	22	□ c _n
G _G □	4	21	A0
Cn + 4	5	20	B0
F3 🗆	5	19	B1
F2 _			A1
PG 🗆	7 8 9	17	□ S1
В3 🗆			A2
А3 🗆	10		S2
B2 🗀		14	□ S0
VEE [12	Brit 1252	S3



TEST VOLTAGE VALUES (Volts) @ Test VIL min VEE Temperature VIH max VIHA min VILA max -1.890 -30°C -0.890 -1.205 -1.500 -5.2 +25°C -0.810 -1.850 -1.105 -1.475 -5.2 +85°C -0.700 -1.825 -1.035 -1.440 -5.2

			1			_			8 8	+85-0	-0.700	-1.825	-1.035	-1.440	-5.2	
		Pin			N		1 Test Lim	33 L	- N.V		т	EST VOLTAG	E APPLIED TO	PINS BELOW:		11/24
Marie leave level level	land 1	Under	-30	o°C	and be	+25°C		+8	5°C			T.		1		
Characteristic	Symbol	Test	Min	159	Min	Тур	Max	Min	159	Unit	VIH max	VIL min	VIHA min	VILA max	VEE	Gnd
Power Supply Drain Current	1E	12	-	-	-	-	145	-	19-11	mAdc	-	-	_	-	12	1,24
Input Current	linH	9	-11	390	- 1	-	245	11-	245	μAric	9	-	-	-/	12	1,24
		10	1	350	- 1	-	220	-	220	1	10	-	-	-	1	18
		11		390	- 1	-	245	-	245		11	-	-			1 15
		13	-	320	- 1	-	200	-	200		13	-	-	-		1 38
		14	-	425	-	-	265	-	265		14	-	_			1.3
		15	-	425		-	265	- 5	265		15		-			
	-	16	4	350		-	220	-	220		16	-		-		1
	-	17	-	425		-	265	-	265		17	-	-	-	1 1 1	
		18	- 1	350	-	-	220	b -	220		18	-	-	-		- 0
		19	-	390	-	-	245	-	245		19	-	-	-		1 9
		20	- 1	390	-	-	245	-	245	114 3	20	-	-	-		
	7 11	21	-	350	-	-	220	-	220		21	-	-			1 22
		22	-	460	-	-	290	-	290		22	-	-	-		
		23	-	320	-	-	200	-	200	T.	23	-	-	-		V 44
Input Leakage Current	linL	9	0.5	-	0.5	-	5	0.3	-	μAdc		9		-	12	1,24
	7-31	10		-		-	-		-	1	-	10	-	T		1 -
	Larry 1	11		-	Level 1	-	-		-	Arriva I	7	11	Land -	Lawrence To		
		13	1 34	-			-		-		= 1	13				
	100	14	- 2	-	A R	7		战 与		100	- A	14	1 7	4 2		
/ / X	1 7	15	1	-/		7-	-		V	1 1	A / - \ /	15	7 7 7	/ / -		
	1 1 1 1 1	16		× - 1		-	- 11		-			16				
	100	17	THE	-	THE STATE OF	1	100	THE	1734	17	THE STATE OF	17	7 7	TO HTM	1 - 1 - 5	
		18		-					7000	1		18		- T	1123	
	11	19				-		+6			1	19			-	
		20		-						4-1		20 21		- T		
	4.4	22			1					1-1-2	1 -	22	-		- 1	
	= 1 Line	23			4			4		V	1-12-1	23	11.	L.		
High Output Voltage	VOH		-1.060	-0.890	-0.960	-	-0.810	-0.890	-0.700	Vdc			- 1	-	12	1,24
Low Output Voltage	VOL	1.	-2.000	-1.675	-1.990	-	-1.650	-1.920	-1.615	Vdc	1		- /	-	12	1,24
High Threshold Voltage	VOHA		-1.080	_	-0.980	-		-0.910	_	Vdc		-			12	1,24
Low Threshold Voltage	VOLA		-	- 1.655	-	_	-1.630	-	-1.595	Vdc		-			12	1,24

^{*}Test all input-output combinations according to Function Table.

^{**} For threshold level test, apply threshold input level to only one input pin at a time

			3123436	Martin 101 Best	20000		AC Sv	vitchin	g Chara	cterist	ics	
the state of the s					-3	0°C *		+25°C		+8	5°C *	150,0
Characteristic	Symbol	Input	Output	Conditions [†]	Min	Max	Min	Тур	Max	Min	Max	Unit
Propagation Delay Rise Time, Fall Time	t++, t t+,t-	C _n	C _{n+4} C _{n+4}	A0,A1,A2,A3 A0,A1,A2,A3	1.0	5.1 3.2	1.1	3.1 2.0	5.0 3.0	1.1	5.4 3.2	ns ns
Propagation Delay Rise Time, Fall Time	t++, t+- t-+, t t+, t-	C _n	F1	A0	1.7 1.7 1.3	7.2 7.2 5.3	2.0 2.0 1.5	4.5 4.5 3.0	7.0 7.0 5.0	2.0 2.0 1.5	7.5 7.5 5.3	ns
Propagation Delay Rise Time, Fall Time	t++, t+- t-+, t t+, t-	A1	F1	of reference a cancilorate ball agazona aiq c	2.6 2.6 1.3	10.4 10.4 5.4	3.0 3.0 1.5	6.5 6.5 3.0	10 10 5.0	3.0 3.0 1.5	10.8 10.8 5.3	ns
Propagation Delay Rise Time, Fall Time	t++, t t+, t-	A1 A1	P _G P _G	\$0,\$3 \$0,\$3	1.6	7.0 3.7	2.0	5.0	6.5 3.5	2.0	7.0 3.8	ns ns
Propagation Delay Rise Time, Fall Time	t++, t t+, t-	A1 A1	G _G G _G	A0,A2,A3,C _n A0,A2,A3,C _n	1.1	7.4	2.0 1.5	4.5 4.0	7.0 5.0	1.3	7.7· 5.3	ns ns
Propagation Delay Rise Time, Fall Time	t+-, t-+ t+, t-	A1 A1	C _{n+4}	A0,A2,A3,C _n A0,A2,A3,C _n	1.7 1.0	7.3 3.1	2.0	5.0	7.0 3.0	2.0 1.0	7.8 3.2	ns ns
Propagation Delay Rise Time, Fall Time	t++, t-+ t+, t-	B1 B1	F1 F1	S3, C _n S3,C _n	2.7	11.3 5.3	3.0	8.0 3.5	11 5.0	3.0	11.9 5.3	ns ns
Propagation Delay Rise Time, Fall Time	t++, t t+, t-	B1 B1	PG PG	S0, A1 S0, A1	1.6 1.0	7.7	2.0	6.0	7.5 3.5	2.0	8.0 3.9	ns ns
Propagation Delay Rise Time, Fall Time	t++, t t+, t-	B1 B1	GG GG	S3. C _n S3.C _n	1.7 1.4	8.2 5.2	2.0	6.0 3.0	8.0 5.0	2.0 1.2	8.6 5.4	ns ns
Propagation Delay Rise Time, Fall Time	t+-, t-+ t+, t-	B1 B1	C _{n+4}	S3, C _n S3,C _n	1.8 0.9	8.2 3.1	2.0	6.0 2.0	8.0 3.0	2.0	8.7 3.2	ns
Propagation Delay , Rise Time, Fall Time	t++, t+- t+, t-	M	F1 F1		2.4 1.1	10.3 5.1	3.0 1.5	6.5 4.0	10 5.0	3.0 1.5	10.8 5.3	ns ns
Propagation Delay Rise Time, Fall Time	t+-, t-+ t+, t-	S1 S1	F1 F1	A1, B1 A1, B1	2.5 1.0	10.7 5.4	3.0 1.5	6.5 3.0	10 5.0	3.0 1.5	10.8 5.4	ns ns
Propagation Delay Rise Time, Fall Time	t-+, t+- t+, t-	S1 S1	P _G P _G	A3, B3 A3, B3	1.7 0.8	8.3 5.1	2.0	6.0 3.0	8.0 5.0	2.0 1.1	8.4 5.2	ns ns
Propagation Delay Rise Time, Fall Time	t+-, t-+ t+, t-	S1 S1	C _{n+4} C _{n+4}	A3, B3 A3, B3	1.6 0.9	9.3 5.3	2.0	6.0	9.0 5.0	2.0 1.0	9.9 5.2	ns
Propagation Delay Rise Time, Fall Time	t+-, t-+ t+, t-	S1 S1	G _G G _G	A3, B3 A3, B3	1.5	9.6 6.2	2.0	6.0	9.0	1.9	9.7 6.5	ns

 $^{^{\}dagger}$ Logic high level (+1.11 Vdc) applied to pins listed. All other input pins are left floating or tied to +0.31 Vdc. VCC1 = VCC2 = +2.0 Vdc, VEE = -3.2 Vdc

*L Suffix Only

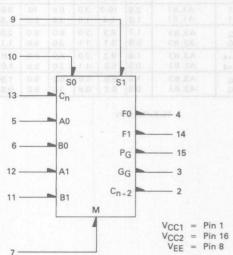
Arithmetic logic operations are selected by applying the appropriate binary word to the select inputs (S0 and S1) as indicated in the tables of arithmetic/logic functions. Group carry propagate (PG) and carry generate (GG) are provided for a second order look ahead carry using the MC10179. The internal carry is enabled by applying a low level voltage to the mode control input (M).

The MC10182 provides an alternate to the MC10181 four-bit ALU for applications not requiring the extended functions of the MC10181 or for applications requiring a 16-pin package. The MC10182 also differs from the MC10181 in that Word A and Word B are treated equally for addition and subtraction (A plus B, A minus B, B minus A).

 $\begin{array}{lll} P_D &=& 575 \text{ mW typ/pkg (No Load)} \\ t_{pd} & \text{(typ): A1 to F} &=& 7.5 \text{ ns} \\ C_n & \text{to } C_{n+2} &=& 2.7 \text{ ns} \\ A1 & \text{to } P_G &=& 6.5 \text{ ns} \\ A1 & \text{to } G_G &=& 5.5 \text{ ns} \\ A1 & \text{to } C_{n+2} &=& 7.0 \text{ ns} \end{array}$

 $t_{r, t_f} = 2.5 \text{ ns typ } (20\%-80\%)$

LOGIC DIAGRAM



		PC	SITIVE LOGIC
Functio S1	n Select S0	Logic Function M is High F	Arithmetic Operation M is Low F
L	L		F = A plus B plus Carry
L	Н	F = A ⊕ B	F = A plus B plus Carry
Н	L	F = A • B	F = A plus B plus Carry
Н	Н	F = A + B	F = A times 2

MC10182

MECL 10K SERIES

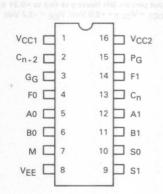
2-BIT ARITHMETIC LOGIC UNIT/FUNCTION GENERATOR

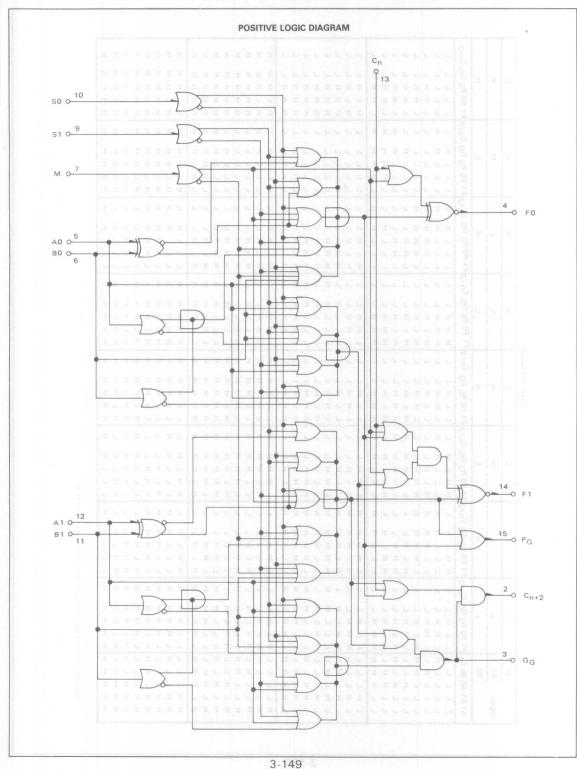
P SUFFIX
PLASTIC PACKAGE
CASE 648



L SUFFIX CERAMIC PACKAGE CASE 620

PIN ASSIGNMENT





CDI	177.14	TA	DI	-

																	IH	UII	1 1/	ABLE																		
	M	9			L	L			L	10		9		L				L				N. Carlo	Н		-		Н		Tal			Н				Н		
nput	S1				L				L			1		Н				Н					L				L		L			Н				Н		III.
	SO				L	TY			Н	100		1	\$ 11	L				Н					L				Н			8,10		L				Н		
A1B1	A0 B0	Cn	F1 F	O PG	GG	Cn+2	F1	FO I	PG G	G Cr	n+2 F	1 F	0 Pc	GG	Cn+2	F1	FO I	G G	G	C _{n+2}	F1	FO F	G G	G Cn+	F1	F0	PG G	G C	n+2	F1 I	FO P	G G	3 Cn+2	F1	F0	PG (GG (C _{n+}
LL	LL	L	LI	- н	L	L	Н	Н	LH	Н	L	нь	H L	Н	L	L	L	н	-	L	Н	Н	H L	L	L	L	LH	4/	L	L	L	L H	L	L	L	L	L	L
LL			LI			L	L		LF			LL			Н	L		H I		L			H L	L	L		L		Н			L H	Н	1	L	L		L
LL			LI		L	L	L	-	HH			H L			L	_		H		L	Н		H L				H		Н			LL	L			Н		L
LL	HL	Н	HI		L	-	L		HH	Н		HH		L	L	L		HI		_			H L		L		HI		H			LL	L			Н		_
1 1		Н	H		10.00	1	Н		HL			LH		Н	Н	1		Н		-			HL				HI		L			LH		1		Н		1
LL		L	н				Н		LH		-	HH		Н	1			н		1			H L				LH		1			н н		1		н		L
LL	нн	н	н	н н	L	L	L	L	LH	н		LL		Н	н			н		L			нц				L		Н			н н		1		Н		L
L H	LL	L	н	Н	L	L	L	Н	н	н	н	LH	1 1	L	L	L	L	н		L	L	Н	H L	L	Н	L	Н	L	L	L	L	LL	L	Н	L	Н	L	L
L H	LL	Н	н	н н	L	L	Н	L	HE	н	н	HL	- +	L	L	L	Н	н		L	L	Н	H L	L	Н	L	н	L	L	L	L	LL	L	Н	L	Н	L	L
L H	L H	L	H	H L	Н	L	H	L	H	н	н	LL	- +	L	L	L	L	н	_	L	L	L	LH	L	H	Н	н	L	L	L	L	LL	L	Н	Н	Н	L	L
L H		Н	The state of	_ L		Н			HH		н	LH			L			H		L	L		LH	Н	Н	100	H		L			LL	L			Н		L
LH	1		12000	H L		L	L		H		100	H L		L	L			Н		L	L		LH		H		H		L	0.77		LL	L			Н		L
LH		-				Н			H			HH			L	13		Н		L			LH		H		Н		L	100		LL	L			H		L
LH		-	L			H	H		HH		10	HL		L	-	H		H		_			H F		10.37		H		L	(A) (A)		H L	_	1000		Н		L
														0.0		-				17	10							17.1		-				-				
HL			Н		L	-	H		HI	TO 10		HI			H	1	1	H		HH			H L	-	1		HI		L	L		LF		1	L	Н		H
HL	037		11/2/27	1 L	1	-	Н	-	HI			LL		Н	Н	L		Н		Н			LF				H		-	L		LL		1	Н	Н		+
HL			L			н	1 2		н і			LH			н			н		н			LH		Н		н		L	L		LL			н	Н		Н
H L	HL	L	н	1 L	Н	L	L	L	HI	L		HL		Н	Н	Н		Н		н			LH		Н		н		L	1000		LH		н	н	Н	Н	H
H L	H L	Н	L	_ L	Н	Н	L	Н	H 1	L	L	HH	H H	Н	Н	Н	Н	Н	Н	н	L	L	LH	Н	Н	н	H 1	L	L	L	L	LH	н	Н	Н	Н	Н	H
HL		L	17.60	L H		Н			H		L	LH	H F	Н	Н	Н		Н		Н			H H				H		L	100		HH		Н	H	Н	Н	H
HL	нн	Н	L	н н	Н	Н	Н	L	ΗΙ	Ľ	L	HI	- 1	Н	Н	Н	Н	Н	Н	Н	L	H	HH	Н	Н	L	н	L	L	L	Н	НН	H	Н	Н	Н	Н	+
н н	100	L	L			Н			LI			H	H L	. н	L			Н		Ĥ			нн		L	L	L	Н	L	100		н н			L	Н		H
нн	100		L			Н	L	-	-			LI			Н	_		Н		Н			HH		L	L	L		Н			HH		Н	L	Н	Н	H
HH				нн		H	L		H			H			L	1		H		Н			H F		L		H		Н	Н		H F		1	Н	H	Н	+
HH	Laborator I	H	Н	L H		Н	L		HI			HH		H H	Н	L		H		Н			HH		L		H		H	H		H F		1	H	Н	Н	H
нн		7.1	Н			Н			HI			LI			Н	100		Н		Н			HH		L		Н		L	V. C. C.		HH		-	Н	Н	Н	H
нн		L	н		Н	Н						H			L	1		Н		Н			HH		1		L		L	01.0		НЕ		1	Н	Н	н	-
	нн		1000	-		Н			L			LI			Н	1000		Н		н			Н		L		-		Н			нь			н		Н	·

These outputs are not normally used during logic operation.

3-151

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

		TEST VO	LTAGE V	ALUES	
	16.		Volts		9
@ Test Temperature	VIHmax	VILmin	VIHAmin	VILAmax	VEE
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

					- 573			7. 7. 1	letty*	+85°C	-0.700	-1.825	-1.035	-1.440	-5.2	
		Pin			M		Test Limit		Sec. Plans	AV PASS	19		GE APPLI		1	
	-	Under	-	0°C	20	+25°C	-		5°C	district.			ISTED BE			(Vcc
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	VIHmax	VILmin	VIHAmir	VILAmax	VEE	Gnd
Power Supply Drain Current	I E	8	-	152	- 7	110	138	19	152	mAdc	-	-	-	- 3	8	1,1
nput Current	linH	7	177	350	-	- 1	220	-	220	μAdc	7	- 1	-	- 4	8	1,1
	£ 50.	5	0.00	620	-	-	390	-	390	1888	5		-			
		6	-	460	-	y - [290	-	290	1	6		- 1			
		13	-	560	-	- 1	350		350	Y	13	-	-			
	linL	5	0.5	- 1	0.5	-	-	0.3	-	μAdc	-	5	- 1	-	8	1,1
Logic "1" Output Voltage	VOH	2	-1.060	-0.890	-0.960	- 6	-0.810	-0.890	-0.700	Vdc	5,6,11	-	3 -		8	1,1
		3	-							-	12,13		1			
		4				-						-	-	-		
		14	-	W	-	-	-	_	-	-	-	-	-	-	-	-
		15			V	-	V	V				-	_	-		- 4
Logic "0" Output Voltage	VOL	2	-1.890	-1.675	-1.850	- 1	-1.650	-1.825	-1.615	Vdc	7,9,10	-	-	-	8	1,1
		3			1837	= 2.2						12.12	2 - 3	1-11	1	8
		4	0 54		6989	8 5 1						2 0	8 - 3	3-15	1	0
		14	1	1		0 8 5		-		1		3 5	- 4	4 7-9		8
		15	V						V	-	V	-	-	7-4		
ogic "1" Threshold Voltage	VOHA	2	-1.080	-	-0.980	0.00	-	-0.910	1 4	Vdc	6,7,9	+ 0	5	- C- 9	8	1,1
		3	5	-	1.8	-	-		14	1 27	5,10,13	E 3	6	1-5	B	9
		4	1-63	-	10-	-	-		-	1.2	7,9,10	9 8	5	10	13	100
		14	-	-	-	-	-		-		9,10	三 章 以	5	45-12	-	3
		15	-	-		2	-		1 -		6,7,9	7 %	5	1 -		-
ogic "0" Threshold Voltage	VOLA	2	-	-1.655	19-	8.3	-1.630	-	-1.595	Vdc	6,7,9	15.5	12 - 3	5	8	1,
		3	-		-	2 8		-	1 8	1 8 8	5,10,13	919	2 - 1	6	15	3
		4	-		10-	-		-		100	7,9,10	8 8	0 - 3	5	1 5	2
		14	-	1	LATE .	Stall A	-	20	1	-	9,10	T 10	0-	5	-	-
9 19 14		15	-	V	-	-		-0		V	6,7,9	2 0	77 - 7	5		D 1
Switching Times								30				+1.11 V		Pulse Out	-3.2V	+2.0
(50 Ω Load)	t13+2+	2 4	1.5	5.9	1.5	2.7	5.6	1.6	6.2	ns	-	10	13	2	8	1,1
Propagation Delay	t13+4-		1.5	5.9	1.5	2.7	5.6	1.6	6.2		-	5	13	4		3
	t5+4-	4	2.3	10.5	2.3	7.0	10	2.4	11		-	7	5	4	18 15	130
	t6-4-	14				7.0	11 1	15	1 1 5	1 1 1	_	9,10	12	14		772
	112-14+	14	6		1 1	7.0	14	100				2.8	11	14	1	0
	t11-14- t5+2+	2	-14	20	1/2	7.0	8 1			1 1 5		9	5	2	1	
	t12-2-	2	19	(U) (E)	1 10	7.0	159		11 4	000		9.10	12	2	2 .	8
	t6-2-	2	A		V	7.0		V	V	9 7	_	10	6	2	3 6	12
	t11+2+	2	2.8	12.6	2.8	7.0	12	2.9	13.2		_	12	11	2	D B	3
	t5-15-	15	2.3	10.5	2.3	6.5	10	2.4	11		_	10	5	15		3
	t6+15+	15		1		6.5			1		_	10	6	15	6 6	8
	t5+3-	3		1		5.5			114		_	10	5	3	9 9	W 1
	t6-3+	. 3	W	- 4		5.5	. *	*	W		-	9	6	3	-	3
	t7-4+	4	2.3	10.5	2.3	4.0	10	2.4	11		-	9,10	7	4		8
	t10-4-	4	2.3	10.5	2.3	6.0	10	2.4	11		-	6,11,13	10	4	V	- 4
Rise Time												3.0	4 4	5 H	1 5	0
(20% to 80%)	14+	4	1.5	4.7	1.5	2.5	4.5	1.6	5.0	ns	-	2 1	5	4	8	1,1
Fall Time	1											B & -	8	2	6	8
(20% to 80%)	t4-	4	1.5	4.7	1.5	2.5	4.5	1.6	5.0	ns	_	_	5	4	8	1,1
	14-			***		~			0.0					75	1 0	1 .,

4 X 2 MULTIPLIER

The MC10183 is a 4 x 2 bit multiplier that can multiply 2's complement numbers producing a 2's complement product without correction. The device can be used as a 4 x 2 bit multiplier cell to build larger iterative arrays.

The part performs the function defined as F = XY + K, where K is an input field used to add partial products in an array or to add a constant to the least significant part of the array product. The algorithm used is a modified Booth's algorithm or multiplier coding technique. The device consists of a shift network and an adder/subtracter in which 0, 1 times X, or 2 times X is either added or subtracted to input constant K. The Y inputs control multiplication as shown in the Truth Table.

The most significant digit in a word carries a negative weight allowing 2's complement numbers of various lengths to be multiplied. An M-bit by N-bit multiplication produces an M $\,+\,$ N bit product.

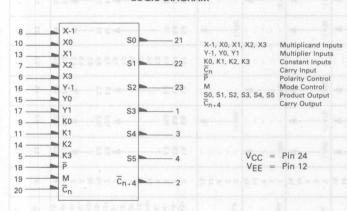
The \overline{P} polarity input allows multiplication in either positive logic ($\overline{P}=$ high) or negative logic ($\overline{P}=$ low) representation. Also, mode control M inverts \overline{C}_n when high and passes \overline{C}_n directly when left low.

PD = 760 mW typ/pkg (No Load)

 $t_{pd} = 50 \text{ ns typ } (8 \times 8 \text{ bit product})$

 t_r , $t_f = 3.5 \text{ ns typ } (20\%-80\%)$

LOGIC DIAGRAM



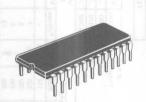
TRUTH TABLE

Y-2	Y0	Y1	P	Α	В	C	Operation	Complementor
L	L	L	L	L	L	L	Add Zero	Direct
Н	L	L	L	Н	L	L	Add 1X	Direct
L	Н	L	L	Н	L	L	Add 1X	Direct
H	Н	L	L	L	H	L	Add 2X	Direct
L	L	Н	L	L	Н	Н	Sub 2X	Invert
Н	L	Н	L	Н	L	Н	Sub 1X	Invert
L	Н	Н	L	Н	L	Н	Sub 1X	Invert
Н	Н	Н	L	L	L	Н	Sub Zero	Invert
L	L	L	Н	L	L	L	Sub Zero	Direct
Н	L	L	Н	Н	L	Н	Sub 1X	Invert
L	Н	L	Н	Н	L	Н	Sub 1X	Invert
Н	H	L.	Н	L	Н	Н	Sub 2X	Invert
L	L	Н	Н	L	Н	L	Add 2X	Direct
H	L	Н	Н	Н	L	L	Add 1X	Direct
L	H.	Н	Н	Н	L	L	Add 1X	Direct
Н	H	Н	Н	L	L	Н	Add Zero	Invert

MC10183

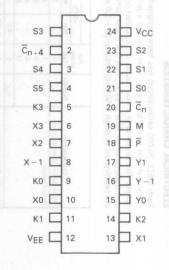
MECL 10K SERIES

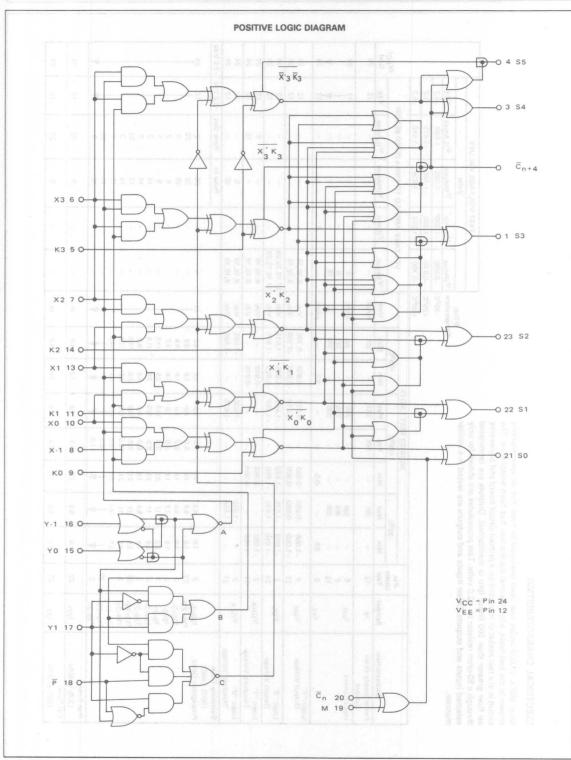
4 X 2 MULTIPLIER



L SUFFIX CERAMIC PACKAGE CASE 623

PIN ASSIGNMENT





Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only selected inputs and outputs. Other inputs and outputs are tested in a similar manner.

		TEST V	OLTAGE VA	LUES							
@Test	Volts										
Temperature	V _{IHmax}	VILmin	VIHAmin	VILAmax	VEE						
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2						
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2						
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2						

					MC	10183 T	EST LIMIT	rs					ED TO DINE	ICTED DEL	NA.	
		Pin Under	-30	ос		+25°C		+85	5°C	1	VOLI	AGE APPLI	ED TO PINS L	IS LED BELC	VV:	(Vcc)
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	VIHmax	VILmin	VIHAmin	VILAmax	VEE	Gnd
Power Supply Drain Current	1E	12	-	201	-	146	183		201	mAdc	11-11				12	24
Input Current	linH	6	-	390	-	-	245		245	μAdc	6	- 11	1 1 + 1	- 1	12	24
		8	-	350	-	-	220	-	220		8			111-11	A THE S	
		18	-	320	-	-	200	-	220	V	18		2 J+1 -1		*	-
	linL	8	0.5	-	0.5		-	0.3	-11	μAdc		8	1 1		12	24
Logic "1" Output Voltage		2	-1,060	-0.890	-0.960		-0.810	-0.890	-0.700	Vdc	8.16.19				12	24
Output Voltage	VOH	21	-1.060	-0.890	-0.960	T.	-0.810	-0.890	-0.700	Vdc	8,16,19	L			12	24
	-			-									-			
Logic "0"	VOL	2	-1.890	-1.675	-1.850	/-	-1.650	-1.825	-1.615	Vdc	17,18,19,20			3/1	12 12	24
Output Voltage		21	-1.890	-1.675	-1.850	7-1	-1.650	-1.825	-1.615	Vdc	17,18,19,20	- A-A-		BUILT		
Logic "1"	VOHA	2	-1.080	-	-0.980	Latin.	Territor	-0.910		Vdc	8,16,19		-	5	12	24
Threshold Voltage		21	-1.080	-	-0.980	1-	-	-0.910	- 1	Vdc	8,16,19	13	- 6	15	12	24
Logic "0"	VOLA	2	-	-1.655	-	-	-1.630	-	-1.595	Vdc	8,16,19	-	5	-	12	24
Threshold Voltage		21	- 5	-1.655	-	1-1	-1.630	\ -	-1.595	Vdc	8,16,19	/- 1	10	-	12	24
Switching Times (50 Ω Load)			-1	1				1					Pulse In	Pulse Out	-3.2 Vdc	-2.0 V d
Propagation Delay	t20+2-	2	1.0	5.3	1.0	4.5	5.0	1.0	5.5	ns			20	2	12	24
	t20+22+	22	1.8	8.4	1.8	6.0	8.0	1.8	8.8	161	_		20	22		
	t20+3-	3	1.8	8.4	1.8	8.0	8.0	1.8	8.8		_	- Z N	20	3	1-1	
	t9+2-	2	1.6	7.3	1.6	5.5	7.0	1.6	7.7	No. il for			9	2		
	t9+1+	1	2.5	11	2.5	8.0	10.5	2.5	11.5			27	9	1		
	t14+3-	3	2.5	11	2.5	8.5	10.5	2.5	11.5		-		14	3		
X I I I I I I I I I I I I I I I I I I I	t10-2+	2	1.8	8.4	1.8	6.0	8.0	1.8	8.8	1/10		/ = /	10	2	1	1
	t13+23+	23	2.5	11	2.5	9.5	10.5	2.5	11.5		- 1	4 -14	13	23		
	t14-3+	3	2.5	- 11	2.5	10.0	10.5	2.5	11.5	-	A - 1	4-7-6	14	3	harried by	-42
	t15-2-	2	3.2	14.1	3.2	10.5	13.5	3.2	14.8			and the second	15	2		
	t15+23+	23				10.5		1			-		15	23		
	t15-3+	3	-	W	-	11.5	-	-	1	-	-	-	15	3		V
Rise Time (20% to 80%)	t22+	22	1.0	6.3	1.0	3.5	6.0	1.0	6.6	ns -	- 1	_	9	22	12	24
Fall Time (20% to 80%)	t ₂₂ -	22	1.0	6.3	1.0	3.5	6.0	1.0	6.6	ns		_	9	22	12	24

MC10183 APPLICATIONS INFORMATION

The MC10183 is a 4 \times 2 bit multiplier that uses a modified Booth's algorithm or multiplier coding technique. The device generates the function: S = X \cdot Y + K

where

X = 4-bit multiplicand

Y = 2-bit multiplier

K = 4-bit constant

The addition of the constant allows the device to be used in an iterative array of parts for larger words. The algorithm for multiplication is:

yi−1	Уį	Yi+1	Operation
0	0	0	add zero
1	0	0	add multiplicand
0	1	0	add multiplicand
1	1	0	add 2 times multi-
			plicand
0	0	1	sub 2 times multi-
			plicand
1	0	1	sub multiplicand
0	1	1	sub multiplicand
1	1	1	sub zero

DEVICE OPERATION

The device consists of three main sections; a decoder, a shifter, and a high speed look-ahead carry adder/subtractor.

1. The decoder uses the Y inputs to generate the control signals for the shifter and the adder/subtractor. Also, the polarity control \overline{P} is used to allow operation in either positive or negative logic. Referring to the logic diagram, the control signals are:

$$\begin{array}{l} A = Y_{-1} \stackrel{\frown}{\bigoplus} Y_0 \ (1 \ times \ multiplicand) \\ B = Y_{-1}Y_0\overline{Y}_1 + \overline{Y}_{-1}\overline{Y}_0Y_1 \\ (2 \ times \ multiplicand) \\ \overline{C} = \overline{PY}_1 + \overline{Y}_{-1}\overline{Y}_0\overline{Y}_1 + PY_1(\overline{Y}_{-1} + \overline{Y}_0) \\ (add/subtract) \end{array}$$

The \overline{P} input is tied to a high logic level or ground for positive logic operation.

2. The shift network is a multiplexer that ripples through number X (1 times multiplicand), shifts number X by one bit (2 times multiplicand), or sets the output to zero. The network is controlled by decoder functions A and B which are generated in accordance with the multiply algorithm.

3. The adder/subtractor follows the shift network which performs the actual multiplication. The adder/subtractor produces the sum or difference of the newly formed partial product and the accumulated partial product (constant K). Subtraction is accomplished by inverting the shifted product and doing a two's complement addition. The carry in of the least significant bit must be a logic one during subtraction.

The two most significant bits of the product are used for sign detection and overflow for a two's complement multiply. These outputs are used only as the two most significant bits of the accumulated product at each addition level within a multiplier array.

Overflow can occur either as the result of 2 times the multiplicand, and/or of an addition or subtraction. To show all possible conditions (including overflow), the most significant bit (S5) must carry a negative binary weight. To show this for a 4 X 2 bit multiply plus constant, consider the following addition:

	×4 ·	x'3 x'2 x'1 x'0	shifter outputs
+	кз •	K3 K2 K1 K0	constant
S5	S4 ·	S3 S2 S1 S0	sum

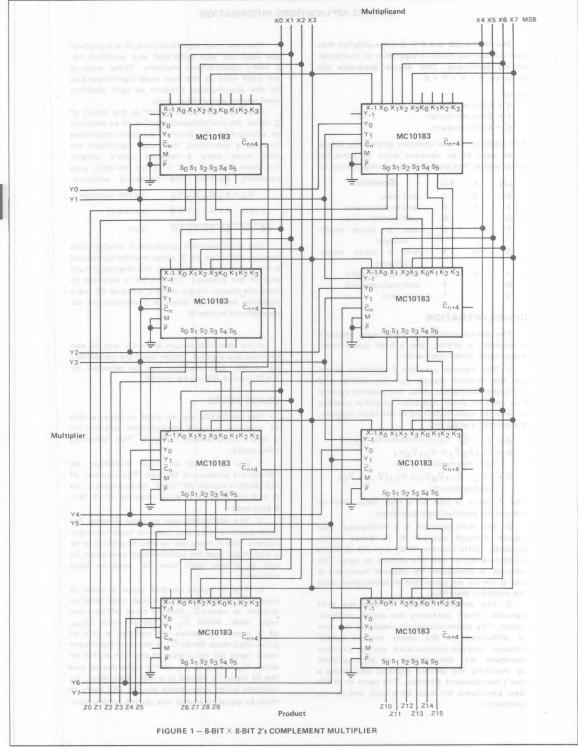
The shift network produces 5 product bits (maximum value of 2 times multiplicand) and a 4-bit constant is added to the least significant end of the product. The K3 bit is repeated to hold the proper binary weight. Because S5 has a negative weight all possible combinations are represented properly.

If no overflow occurs S4 = S5, and S4 can be used as a sign bit. Under overflow conditions S4 \neq S5, and overflow can be detected by EXCLUSIVE-ORing S4 and S5.

USAGE RULES

The MC10183 can be used in larger arrays to produce a two's complement product of 2 two's complement numbers. The following rules apply:

- 1. For an M-bit by N-bit multiplier, an (M+N)-bit product is formed. The number of MC10183's equals (M*N)/8. As an example, an 8 \times 8 bit (Figure 1) array requires $(8\times8)/8 = 8$ packages.
- 2. The MC10183 can be used directly for both positive logic and negative logic representations. The \overline{P} input can be tied to ground or to a high logic level for positive logic operation, or left at a low logic level for negative logic operation.
- 3. The M mode control input is used to invert \overline{C}_n when placed at a high logic level or ground, or passes \overline{C}_n directly when left as a low logic level. When \overline{C}_n is driven from \overline{C}_{n+4} of a preceding device, M control is left in a low logic state. When \overline{C}_n is the least significant input carry bit for a level of addition within an array, \overline{C}_n is tied to Y₁ of the same device, and the M input is placed at a high logic level. Y₁ controls when subtraction occurs, and carry in must be equal to a logic one during subtraction.



8 × 4 BIT EXAMPLE

Figure 2 shows 4 MC10183's in an 8 X 4 bit array. A 12-bit two's complement product is produced from a 4-bit multiplier and an 8-bit multiplicand. The array is used for positive logic representation, and all P inputs are tied to ground. At the first level of multiplication, the X_{-1} and Y_{-1} inputs are left open (logic "O") because the initial condition is treated as an add operation. The K inputs are used to add the accumulated partial product at each level of the array. If the initial partial product is zero, the least significant K inputs are left at a zero logic state (CONSTANT inputs in the figure). However, these inputs can also be used to add a constant to the least significant end of the product.

When the MC10183 is expanded to longer numbers, the carry out (\overline{C}_{n+4}) of a device must be rippled to the carry in (\overline{C}_n) of the next most significant device at the same level of multiplication. The least significant device must have the carry input equal to zero for an add and equal to one for a subtraction. In observing the multiplication algorithm v_{i+1} is always equal to 1 for a subtraction, and the carry input can be tied to Y_1 . However, the M mode input must be tied to ground for this device to invert the carry input (\overline{C}_n) because the input requires a complemented signal.

The S4 and S5 outputs are used only at the most significant part of the array. These two sum outputs only have meaning as the two most significant bits of a two's complement number.

OTHER ARRAYS

The normal parallelogram structure consists of several stages, each multiplying two bits of multiplier times the multiplicand and adds the partial product. In larger arrays, faster configurations can be made by moving some multiplier blocks while maintaining the relative weight of each partial product. The typical times possible for various N-bit X N-bit arrays are:

Number	Total	
of Bits	Multiply Time (ns)	Package Count
8	43	8
12	67	18
16	90	32

The times do not include wiring delays.

Because of the versatility of the MC10183, many other types of arrays can also be built. Faster arrays using additional adders, pipeline techniques, one's complement and magnitude multipliers, and truncated product multipliers can all be built.

Multiplicand

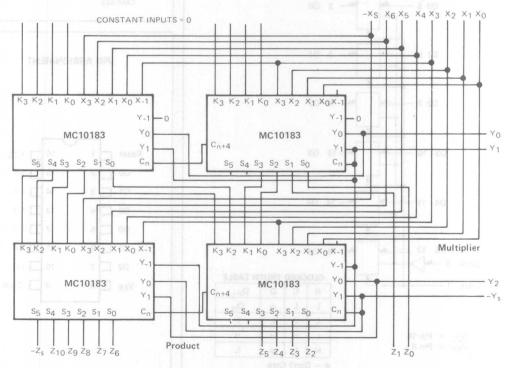


FIGURE 2 - 8-BIT BY 4-BIT 2's COMPLEMENT MULTIPLIER



MC10186

HEX "D" MASTER-SLAVE FLIP-FLOP/WITH RESET

The MC10186 contains six high-speed, master slave type "D" flip-flops. Clocking is common to all six flip-flops. Data is entered into the master when the clock is low. Master to slave data transfer takes place on the positive-going Clock transition. Thus, outputs may change only on a positive-going Clock transition. A change in the information present at the data (D) input will not affect the output information any other time due to the master-slave construction of this device. A common Reset is included in this circuit. Reset only functions when clock is low.

P_D = 460 mW typ/pkg (No Load)

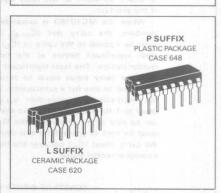
f_{toggle} = 150 MHz (typ)

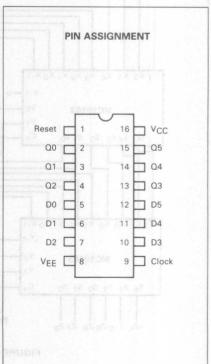
 t_{r} , $t_{f} = 2.0 \text{ ns typ } (20\%-80\%)$

LOGIC DIAGRAM D0 5 2 Q0 D1 6 3 Q1 D2 7 4 02 D3 10 13 Q3 D4 11 14 Q4 D5 15 Q5 Clock 9 **CLOCKED TRUTH TABLE** Reset R C Q_{n+1} φ Qn L L L H L L VCC = Pin 16 L H H H VEE = Pin 8 H L φ L $\phi = Don't Care$ *A clock H is a clock transition from a low to a high state.

MECL 10K SERIES

HEX "D" MASTER-SLAVE FLIP-FLOP/WITH RESET





Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to $-2.0 \ \text{volts}$. Test procedures are shown for only one data input, the clock input, and the reset input, and for one output. Other inputs and outputs tested in the same manner.

		TEST VOLTAGE VALUES										
@ Test	(Volts)											
Temperature	VIHmax	VILmin	VIHAmin	VILAmax	VEE							
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2							
+25°C	-1.810	-1.850	-1.105	-1.475	-5.2							
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2							

		Pin			M	C10186	Test Limi	ts							251 0111	
		Under	-30	o°C		+25°C		+85	5°C		TEST VO	L TAGE A	PPLIED TO P	INS LISTED	BELOW:	(VCC
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	V _{IHmax}	VILmin	VIHAmin	VILAmax	VEE	Gnd
Power Supply Drain Current	1E	8	-	121	-	88	110	-	121	mAdc	-	-	1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 -		8	16
Input Current	linH	5 9 1	-	350 495 920	=	-	220 310 575	-	220 310 575	μAdc	5 9 1		5 10 10		8 8	16 16 16
Input Leakage Current	linL	5	0.5	_	0.5	-	-	0.3	_	μAdc	-	5	- 220	_	8	16
Logic "1" Output Voltage	VOH	2† 15†	-1.060 -1.060	-0.890 -0.890	-0.960 -0.960	_ 69	-0.810 -0.810	-0.890 -0.890	-0.700 -0.700	Vdc Vdc	5 12	II.	1 2 3	Ī	8	16 16
Logic ''0'' Output Voltage	VOL	2† 15†	-1.890 -1.890	-1.675 -1.675	-1.850 -1.850	_	-1.650 -1.650	-1.825 -1.825	-1.615 -1.615	Vdc Vdc	-	5 12	16 47 10 0 0 10 0 0	_	8	16 16
Logic ''1'' Threshold Voltage	VOHA	2† 15†	-1.080 -1.080	T/E	-0.980 -0.980	-1	-	-0.910 -0.910	-	Vdc Vdc	1.8	6-8	5 12	1831	8	16 16
Logic "0" Threshold Voltage	VOLA	2† 15†	7	-1.655 -1.655		4	-1.630 -1.630	Ī	-1.595 -1.595	Vdc Vdc	-	83	576	5 12	8	16 16
Switching Times Propagation Delay	CK -		L			L	-		- 8		+1.11 Vdc	+0.31 Vdc	Pulse In	Pulse Out	-3.2 Vdc	+2.0 Vdc
(50 Ω Load)	t ₁₊₃₋	3 4	1.6	4.6	1.6	2.5	4.5	1.6	5.0	ns	6 7	678	1,9 1,9	3 4	8	16
Rise Time (20 to 80%)	t9+2+ t9+2-	2 2	V		+	3.5 3.5 1.8	V	+				1 _6	5,9			П
Fall Time (20 to 80%)	t ₂₊	2 2	1.0	4.1 4.1	1.1	1.8	4.0	1.1	4.4		_	37	734			
Setup Time	t _{setup}	2	2.5	-	2.5	2.5	-	2.5	-	ns	-	<u> </u>	5,9	2	8	16
Hold Time	thold	2	1.5	_	1.5	-1:5	-	1.5	-	ns	_	9-8	5,9	2	8	16
Toggle Frequency	ftog	2	125	-	125	150	- 1	125	-	MHz	_	19 -03	3 5 2 6	-	8	16

†Output level to be measured after a clock pulse.

VIL appears at clock input (pin 9).

HEX BUFFER WITH ENABLE

The MC10188 is a high-speed hex buffer with a common Enable input. When Enable is in the high state, all outputs are in the low state. When Enable is in the low state, the outputs take the same state as the inputs.

Power Dissipation = 180 mW typ/pkg (No Load) Propagation Delay = 2.0 ns typ (B - Q) 2.5 ns typ (A - Q)

MECL 10K SERIES

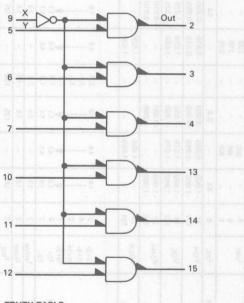
HEX BUFFER WITH ENABLE

P SUFFIX PLASTIC PACKAGE CASE 648



CERAMIC PACKAGE CASE 620

LOGIC DIAGRAM



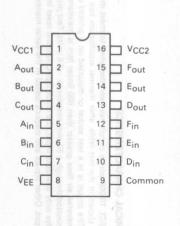
TRUTH TABLE

Inp	uts	Output				
X	Y	OUT				
L	L	L				
L	Н	Н				
Н	L	L				
Н	Н	L				

V_{CC1} = Pin 1

V_{CC2} = Pin 16 VEE = Pin 8

PIN ASSIGNMENT



Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for one set of conditions. Complete testing according to truth table.

		TES	ST VOLTAGE	VALUES	Basi
@ Test			(Volts)	121	(3
Temperature	V _{IHmax}	V _{ILmin}	VIHAmin	VILAmax	VEE
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

									100 C	-0.700	-1.025	-1.033	-1.440	-3.2	
		Pin			Test L	mits		Lind (
		Under	-30)°C	+2	5°C	+85	5°C		TEST VO	LTAGE APP	LIED TO PIN	IS LISTED BI	ELOW	(Vcc
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Unit	V _{IHmax}	V _{ILmin}	VIHAmin	VILAmax	VEE	Gnd
Power Supply Drain Current	I _E	8	-	46	-	42		46	mAdc	-	-	- 17	3 3	8	1,16
Input Current	linH	5		425	- 1	265		265	μAdc	5	-	- 91	¥ 8_	8	1,16
	linH	9	-	460	-	290	-	290	μAdc	9	-	- 8	ğ g-	8	1,16
Logic "1" Output Voltage	VOH	2	-1.060	-0.890	-0.960	-0.810	-0 890	0.700	Vdc	5	-8	- 5	18 Kg Kg Kg Kg Kg Kg Kg Kg Kg Kg Kg Kg Kg	8	1,16
Logic "0" Output Voltage	VOL	2	1.890	-1 675	-1.850	1 650	-1 825	1 615	Vdc		9 0	- E	100 AT 100	8	1,16
Logic "1" Threshold Voltage	VOHA	2	-1.080	- 3	-0.980	À	0.910		Vdc		5 O Topic	5		8	1,16
Logic "O" Threshold Voltage	VOLA	2		-1.655		1.630	later to a	-1.595	Vdc		40 (g	503	5	8	1,16
Switching Times (50 \Omega Load) Propagation Delay	^t PHL					10.55		- 8	ns		2 0 th	Pulse In	Pulse Out	-3.2 V	+ 2.0
Enable Data	tPLH	2 2	1.1 1.0	3.9 3.3	1.1	3.5 2.9	1.1	3.9 3.3		_	2 G	9 5	and and the	8	1, 16
Rise Time, Fall Time (20% to 80%)	tTLH- tTHL	2	1.1	3.7	1.1	3.3	1.1	3.7	*	-	-	▼ S. S.	2 24	*	*

MC10189

HEX INVERTER WITH ENABLE

The MC10189 provides a high-speed Hex Inverter with a common Enable input. The hex inverting function is provided when Enable is in the low state. When Enable is in the high state all outputs are low.

 $P_D = 200 \text{ mW typ/pkg (No Load)}$

 $t_{pd} = 2.0 \text{ ns typ } (B - Q)$

= 2.5 ns typ (A - Q)

MECL 10K SERIES

HEX INVERTER WITH ENABLE

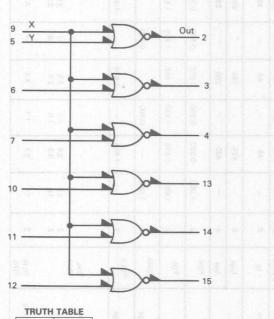
P SUFFIX PLASTIC PACKAGE CASE 648





CASE 620

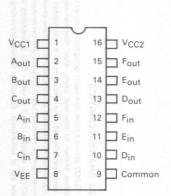
LOGIC DIAGRAM



	Inp	uts	Output
	X	Y	OUT
	L	L	Н
	Ė	Н	L
-	Н	L	L
	Н	Н	L

V_{CC1} = Pin 1 V_{CC2} = Pin 16 V_{EE} = Pin 8

PIN ASSIGNMENT



3-162

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for one set of conditions. Complete testing according to truth table.

		TE	ST VOLTAGE	VALUES	23
@ Test			(Volts)	of The	
Temperature	V _{IHmax}	VILmin	VIHAmin	VILAmax	VEE
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

									.00 0	0.700	1.020	1.000	1.440	0.2	
		Pin			Test Li	mits	1					I			al las
		Under	-30)°C	+2!	5°C	+8!	5°C		TEST VO	LTAGE APP	LIED TO PIN	S LISTED B	ELOW	(VCC
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Unit	V _{IHmax}	V _{ILmin}	VIHAmin	VILAmax	VEE	Gnd
Power Supply Drain Current	ΙE	8	7.7	44	-	40	I	44	mAdc		8 11	1 to 1 to 1 to 1 to 1 to 1 to 1 to 1 to	-	8	1,16
Input Current	linH	5	-	425	-	265	1	265	μAdc	5	59-11	15 8 8		8	1,16
	linH	9	_	890	-	555	1 -	555	μAdc	9	6 g- 3 1	1982.	-	8	1,16
Logic "1" Output Voltage	VOH	2	-1.060	-0.890	-0.960	-0.810	-0.890	-0.700	Vdc	- 9	5	1 1 1 1	j	8	1,16
Logic "0" Output Voltage	VOL	2	1.890	-1 675	-1.850	-1.650	-1.825	-1.615	Vdc	9		Burks Burks	_	8	1,16
Logic "1" Threshold Voltage	VOHA	2	-1.080	7 -	-0.980	1	-0.910		Vdc	0.5		14 2 4	5	8	1,16
Logic "0" Threshold Voltage	VOLA	2	A	-1.655	_	-1.630		-1.595	Vdc		POLY POLY PARTIN	5	1 A S	8	1,16
Switching Times (50 Ω Load) Propagation Delay	tphL.	8				rosio			ns gall an	S LIMA O	HA BI BI SIN	Pulse In	Pulse Out	-3.2 V	+2.0 V
Enable Data		2 2	1.1 1.0	3.9 3.3	1.1 1.0	3.5 2.9	1.1 1.0	3.9 3.3		8 - 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8	Supple of	9	2	8	1, 16
Rise Time, Fall Time (20% to 80%)	t _{TLH} , t _{THL}	2	1,1	3.7	1.1	3.3	1.1	3.7	*	3 - 3	8070 B		3 *	*	*

QUAD MST TO MECL 10,000 TRANSLATOR

The MC101090 is a quad translator for interfacing from IBM MST-type logic signals to standard MECL 10,000 logic levels. This circuit features differential inputs for high noise environments or may be used with single ended lines by tieing one of the inputs to ground. Since the MC10190 is designed to accept signals centered around ground, it is a useful interface element for many communication systems. When pin 9 is connected to V_{CC} the circuit becomes a line receiver for MECL signals. The outputs go to a low level whenever the inputs are left floating.

P_D = 215 mW typ/pkg (No Load)

 $t_{pd} = 2.5 \text{ ns typ}$

 t_r , $t_f = 2.0$ ns typ (20%–80%)

MECL 10K SERIES

QUAD MST TO MECL 10,000 TRANSLATOR

P SUFFIX
PLASTIC PACKAGE
CASE 648

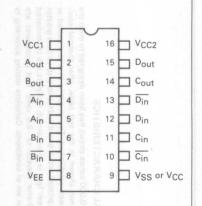
L SUFFIX
CERAMIC PACKAGE

CASE 620

LOGIC DIAGRAM 4 5 2 7 6 3 10 11 11 13

VCC1 = Pin1 VCC2 = Pin 16 VEE = Pin 8 VSS = Pin 9 Translator VCC = Pin 9 Receiver

PIN ASSIGNMENT



Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only selected inputs and outputs. Other inputs and outputs test in the same manner.

sted				TE	ST VOLT	AGE VAI	LUES					
				4 2 5	(V	olts)			8			
@ Test Temperature	VIHmax	VILmin	VILAmin	VILAmax	VIHM*	VILM*	VIHH*	VILH*	VIHL*	VILL*	VSS*	VEE
-30°C	-0.890	-1.890	-1.205	-1.500	+0.374	-0.523	+0.186	-0.850	-1.486	-2.53	+1.25	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	+0.440	-0.490	+0.186	-0.850	-1.486	-2.53	+1.25	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	+0.548	-0.454	+0.186	-0.850	-1.486	-2.53	+1.25	-5.2

									7.6	85°C	-0.700	-1.825	-1.035	-1.440	+0.548	-0.454	+0,186	-0.850	-1.486	-2.53	+1.25	-5.2	
		Pin			MC1	0190	Test Limit	ts		d		port of	TECT	VOLTAG	E ADDI IE	D TO BIN	CLICTED	DEL OW					
		Under	-3	O _o C		+25°C		+8	5°C	o. 111		1	1531	VOLTAG	AFFLIC	DIOFIN	S LISTED	BELOW.	1	-			(Vcc)
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	VIHmax	VILmin	VILAmir	VILAmax	VIHM*	VILM*	VIHH*	VILH*	VIHL*	VILL*	V _{SS} *	VEE	Gnd
Power Supply Drain Current	1E	8	-	57	-	41	52	-	57	mAdo	4,6,10,12	5,7,11,13	1 -/	5 -/	-				60 -	-(8)	9	8	1,16
	1cc	9	-	27	-	22	27	-	27	mAdd	4,6,10,12	5,7,11,13	-	15 - 3		2 3		-	19-	- 111	9	8	1,16
Input Current	linH	4 5	_	70 70	Ī	1 1	45 45	0.2 %	45 45	μAdc μAdc	4 5	5 4	7-1	100		1		-	7	-31	9	8	1,16 1,16
Reverse Leakage Current	СВО	4	-	1.5	-	-	1.0	0.0	1.0	μAdc	-	- 1	10-	10-10	and bu		-10	-	14 -		9	4,8	1,16
Logic ''1'' Output Voltage	VOH	2 2	-1.060 -1.060	-0.890 -0.890	-0.960 -0.960	-	-0.810 -0.810	-0.890 -0.890	-0.700 -0.700	Vdc Vdc	5	4	-		5	- 4	-8	-	<	_	9	8	1,9,16 1,16
Logic "0" Output Voltage	VOL	2 2	-1.890 -1.890	-1.675 -1.675	-1.850 -1.850	-	-1.650 -1.650	-1.825 -1.825	-1.615 -1.615	Vdc Vdc	4	5	-	-	4	- 5	-	=	_	Ξŝ	9	8	1,9,16
Logic "1" Threshold Voltage	VOHA	2	-1.080	-	-0.980		4 3	-0.910	7-3	Vdc	-8	0 -	5	4	-	-	-	-	-	-3	-	8	1,9,16
Logic "0" Threshold Voltage	VOLA	2	-	-1.655	-	-	-1.630	2 2 9	-1.595	Vdc		ä -	4	5	-		- (+	1-10	1.	-00	-	8	1,9,16
Common Mode Rejection Test	VOH	2 2	-1.060 -1.060	-0.890 -0.890	-0.960 -0.960	-	-0.810 -0.810	-0.890 -0.890	-0.700 -0.700	Vdc Vdc	-18		_	T	1	-	5	4	5	_ 	_	8	1,9,16 1,9,16
	VOL	2 2	-1.890 -1.890	-1.675 -1.675	-1.850 -1.850	-	-1.650 -1.650	-1.825 -1.825	-1.615 -1.615	Vdc Vdc	-<	95	-	-	1	138	4	5	- 4	- 5	-	8	1,9,16
Switching Times (50 ohm load)							1 7	5 2 3	2 1		100	61	Pulse In	Pulse Out	-	2					+3.25 V	-3.2 V	+2.0 V
Propagation Delay	t4-2+ t4+2-	2	1.0	3.9 3.9	1.0 1.0	2.5 2.5	3.7	1.0	4.1	ns ns	- 0	4.7	4	2	3	-	-	-	-	-	9	8	1,5,6,11,12
Rise Time (20% to 80%)	t2+	2	1.1	4.5	1.5	2.0	4.3	1.1	4.7	ns	-13	OZ -	4	2	-	-	-	-	-	-	9	8	1,5,6,11,12
Fall Time (20% to 80%)	12-	2	1.1	4.5	1.5	2.0	4.3	1.1	4.7	ns	-	-	4	2	-	-	-	-	-	-	9	8	1,5,6,11,12

^{*}VSS = IBM Supply Voltage.

V_{IHM} = Input Logic "1" for IBM levels.

V_{ILM} = Input Logic "0" for IBM levels.

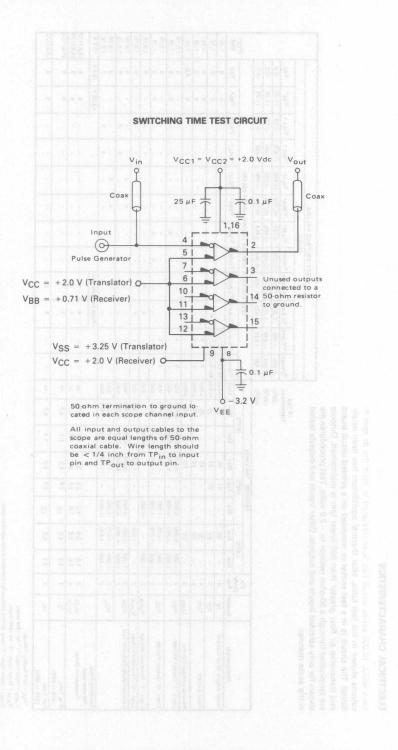
V_{ILM} = Input Logic "0" for IBM levels.

V_{IH} = Input logic "1" level shifted positive for common mode rejection tests.

V_{ILM} = Input logic "0" level shifted positive for common mode rejection tests.

V_{ILL} = Input logic "1" level shifted negative for common mode rejection tests.

V_{ILL} = Input logic "0" level shifted negative for common mode rejection tests.





HEX MECL 10,000 TO MST TRANSLATOR

The MC10191 is a hex MECL to IBM MST type logic translator. A common enable (active low) is provided for gating. Open emitter outputs are provided for gating. Open emitter outputs are provided to permit direct transmission line driving.

The MC10191 is useful for interfacing to both MST-II and MST-IV systems.

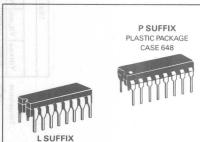
P_D = 170 mW typ/pkg (No Load)

t_{pd} = 2.2 ns typ Input to Output

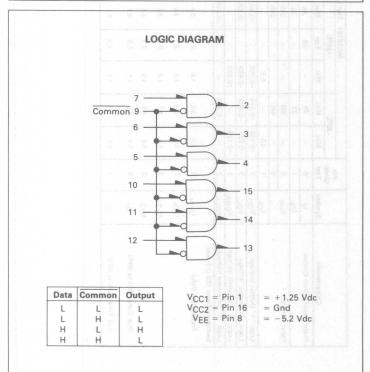
= 3.3 ns typ Enable to Output

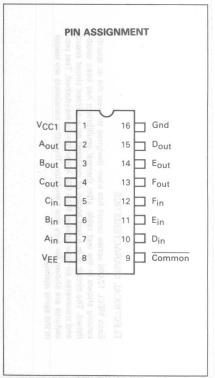
MECL 10K SERIES

HEX MECL 10,000 TO MST TRANSLATOR





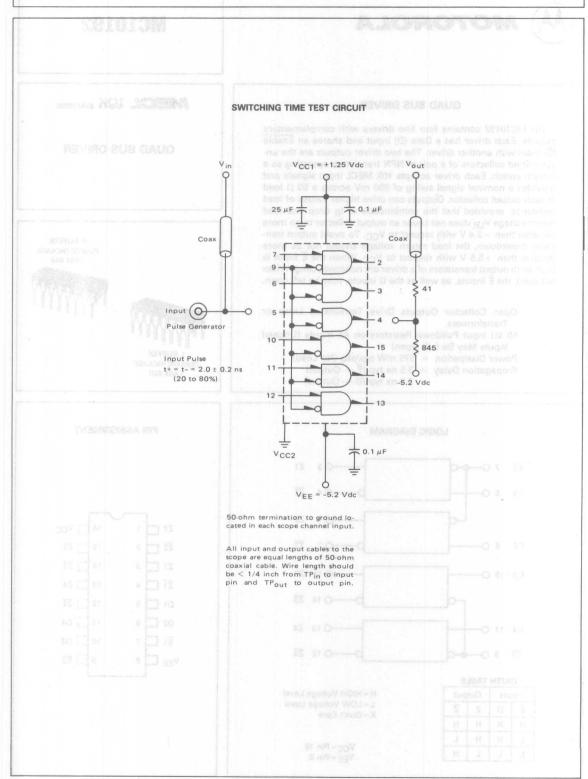




		TE		GE VALU	ES	1075
49			Vo	lts	refer	
@ Test Temperature	VIHmax	VILmin	VIHAmin	VILAmax	VEE	V _{CC1}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2	+1.25
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2	+1.25
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2	+1.25

		Pin				MC1019	1 Test Li	mits									111
		Under	-30	ос		+25°C		+85	5°C		VOL	TAGE AP	PLIED TO	PINS LIST	TED BEL	OW:	(VCC2
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	VIHmax	VILmin	VIHAmin	VILAmax	VEE	V _{CC1}	Gnd
Power Supply Drain Current	1E	8	-	39	_	28	35		39	mAdc	9	- 4	4 9	2-	8	1	16
	1cc	1	_	23	-	-	23	-	23	mAdc	9	- 9	20	E5	8	1	16
Input Current	linH	5	-	390	-	-	245	-	245	μAdc	5	-	= 0	11-	8	1	16
		9	-	425	-	-	265	-	265	μAdc	9	- 10	6 10 3	0-	8	1	16
	linL	7	0.5		0.5	-		0.3	-	μAdc	-	7 5	2 4 5	0-0	8	1	16
Logic "1" Output Voltage	VOH	2	+0.156	+0.374	+0.255	-	+0.440	+0.327	+0.548	Vdc	7	9	3 4	2 -	8	1	16
Logic "0" Output Voltage	VOL	2	-0.523	-0.323	-0.490		-0.290	-0.454	-0.254	Vdc	K-	9	7		8	1	16
Logic "1" Threshold Voltage	VOHA	2	+0.136		+0.235		+ 1	+0.307	-	Vdc	5 9-	9	7	22-	8	1	16
Logic "0" Threshold Voltage	VOLA	2	8.	-0.303	-	-8	-0.270	-	-0.234	Vdc	-	9	34	7	8	1	16
Switching Times (50 Ω Load)	136	34	11	MA	1157-1	56	(SEALINE)	17.67.5		25	-0.890 V	-1.690 V	Pulse In	Pulse Out	-5.2 V	+1.25 V	+2.0 V
Propagation Delay	t7+2+	2	1.0	3.6	1.0	2.2	3.4	1.0	3.7	ns	5,6,10, 11,12	9	7	2	8	1	16
	t7-2-	2	1.0	3.6	1.0	2.2	3.4	1.0	3.7	1	5,6,10, 11,12	9	7	2			
	t9-2+	2	1.0	4.7	1.0	3.3	4.5	1.0	5.0	9	7	5,6,10, 11,12	9	2			
	t9+2-	2	1.0	4.7	1.0	3.3	4.5	1.0	5.0		7	5,6,10, 11,12	.9	2			
Rise Time (20% to 80%)	t ₂₊	2	1.1	4.5	1.1	2.5	4.3	1.1	4.7		5,6,10, 11,12	9	7	2			
Fall Time (20% to 80%)	t2-	2	1.1	4.5	1.1	2.5	4.3	1.1	4.7	1	5,6,10, 11,12	9	7	2			1

3-168



MC10192

3

QUAD BUS DRIVER

The MC10192 contains four line drivers with complementary outputs. Each driver has a Data (D) input and shares an Enable ($\overline{\rm E}$) input with another driver. The two driver outputs are the uncommitted collectors of a pair of NPN transistors operating as a current switch. Each driver accepts 10K MECL input signals and provides a nominal signal swing of 800 mV across a 50 Ω load at each output collector. Outputs can drive higher values of load resistance, provided that the combination of IR drop and load return voltage VLR does not cause an output collector to go more negative than -2.4 V with respect to VCC. To avoid output transistor breakdown, the load return voltage should not be more positive than +5.5 V with respect to VCC. When the $\overline{\rm E}$ input is high, both output transistors of a driver are nonconducting. When not used, the $\overline{\rm E}$ inputs, as well as the D inputs, may be left open.

Open Collector Outputs Drive Terminated Lines or Transformers

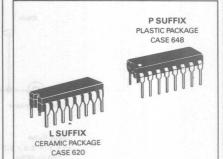
50 kΩ Input Pulldown Resistors on All Inputs (Unused Inputs May Be Left Open)

Power Dissipation = 575 mW typ/pkg (No Load) Propagation Delay = 3.5 ns typ (\overline{E} — Output)

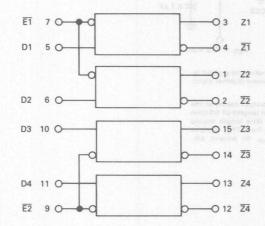
3.0 ns typ (D — Output)

MECL 10K SERIES

QUAD BUS DRIVER







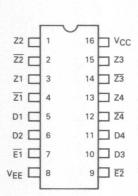
TRUTH TABLE

1	Inp	uts	Out	put
	Ē	D	Z	Z
	Н	X	Н	Н
	L	Н	Н	L
	L	L	L	Н

H = HIGH Voltage Level L = LOW Voltage Level X = Don't Care

> V_{CC}=Pin 16 V_{FF}=Pin 8

PIN ASSIGNMENT



Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to ground volts. Test procedures are shown for one set of conditions. Complete testing according to truth table.

1		TES	T VOLTAGE VAL	UES	
@ Test			(Volts)		San Carlo
Temperature	VIHmax	VILmin	VIHAmin	VILAmax	VEE
-30°C	-0.890	-1.890	- 1.205	- 1.500	-5.2
+25°C	-0.810	- 1.850	- 1.105	- 1.475	-5.2
+85°C	-0.700	- 1.825	- 1.035	-1.440	-5.2

	6	74	3.		Test	Limits			0 8 12 1						
		Pin Under	-3	0°C	+2	25°C	+8	85°C	8 1	TE	ST VOLTAGE A	PPLIED TO PIN	S LISTED BELOV	N	(Vcc)
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Unit	VIHmax	VILmin	VIHAmin	VILAmax	VEE	Gnd
Power Supply Drain Current	IE	8	-	154	=	140	-	154	mAdc		-		=	8	16
Input Current	linH	5		350		220	_	220	μAdc	5	_		_	8	16
	linL	5	0.5	_	0.5	-	0.3	_	μAdc		5	3 H	2 2-8	8	16
Logic "1" Output Current High	ЮН	2	_	m _	e _	2.0	_	-	mAdc		5,6,10,11		7 5 5	8	16
Logic "0" Output Current Low	lOL	2	13.5	+18	14	18	14	19	mAdc	5,6,10,11	100			8	16
Logic "1" Output Current High	Іонс	2	_	2.0	-	2.0	L	2.0	mAdc		5,7,9,10,11	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	6	8	16
Logic "0" Output Current Low	lorc	2	13.5	1-2	14		14	_	mAdc	5,10,11	7,9	6	1 5 <u>5</u> 5	8	16
Logic "0" Output Sink Current Low	los	2	13.3	1_	13.9	1-	13.3	_	mAdc	5,6,10,11	2.3	建建	1	8	16
Load Return Voltage Absolute Max Rating (Note 1)	VLR		854	5.5		5.5		5.5	Volts	Lateral Latera	at judes	Mark Park	Tayout Newsork	8	16
Output Voltage Low (Note 2)	Vols	#			-2.4				Volts	111	444		100	8	16
Switching Times (50 Ω Load) Propagation Delay E to Output D to Output	tPHL tPLH	TANDETTO TAL	_		2.0 1.5	6.0 4.5		_	ns	100 × 100 ×	10'900 duer ondans du hatse ju bad	purvided the total	MARKETERS OF STANKING	4 6	
Rise Time, Fall Time (20% to 80%)	tTLH tTHL	-	- 4	27	_	3.3	3.75	_			0.5 %				

NOTE 1 The 5.5 V value is a maximum rating, do not exceed. A 270 OHM resistor will prevent output transistor breakdown.

NOTE 2 Limitations of load resistor and load return voltage combinations. Refer to page 1 description.

MC10194

DUAL SIMULTANEOUS BUS TRANSCEIVER

The MC10194 is a dual line driver/receiver which is capable of transmitting and receiving full duplex digital signals on a high speed bus line. Because of the current source line driver, two independent messages may be transmitted on one line at the same time.

The MC10194 is designed to work with a wide range of line impedances by connecting a resistor equal to one half the line impedance between the $R_{\rm E1}$ and $R_{\rm E2}$ inputs and $V_{\rm EE}$. Each driver in the circuit will drive lines down to 75 ohms or the two drivers may be operated in parallel for lines down to 37 ohms. The data inputs and outputs on the MC10194 are fully compatible with other MECL 10,000 circuits.

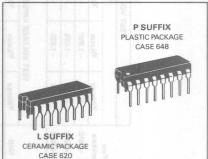
 $P_D = 405 \text{ mW typ/pkg (No Load)}$

 $t_{pd} = 2.5 \text{ ns typ}$

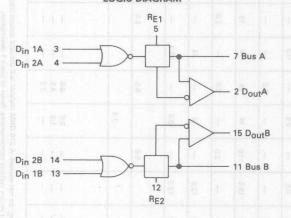
 t_r , $t_f = 2.0 \text{ ns typ } (20\%-80\%)$

MECL 10K SERIES

DUAL SIMULTANEOUS BUS TRANSCEIVER



LOGIC DIAGRAM



	TRU	TH TABLE	
Inp	uts	Outp	outs
Din 1	Din 2	Bus	Dout
L	L	V _{Bus} O	Н
Н	L	V _{Bus} H	Н
L	Н	VBusH	H
Н	Н	V _{Bus} H	Н
L	L	V _{BusH}	L
Н	L	V _{Bus} L	L
L	Н	VBusL	L
Н	Н	VBusL	L

V_{CC1} = Pin 1 V_{CC2} = Pin 16 V_{EE} = Pin 8

PIN ASSIGNMENT VCC1 1 16 VCC2 Dout A 2 15 Dout B Din 1A 🔲 3 14 Din 2B Din 2A 4 13 Din 1B RE1 5 12 RE2 N.C. 6 11 Bus B 10 N.C. Bus A 7 9 N.C. VEE

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Data outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown only for selected inputs and outputs. Other inputs and outputs are tested in a similar manner.

			TE	ST VOLT	AGE/CUR	RENT VALU	IES			
@ Test		(mAdc)				(Volts	:)	310		
Temperature	ICS1	ICS0A	ICS1A	VIHmax	VILmin	VIHAmin	VILAmax	VCL	VCH	VEE
-30°C	-21.1	6.35	14.50	-0.890	-1.890	-1.205	-1.500	-1.508	0	-5.2
+25°C	-22.6	6.80	15.27	-0.810	-1.850	-1.105	-1.475	-1.618	0	-5.2
+85°C	-24.2	7.27	16.35	-0.700	-1.825	-1.035	-1.440	-1.738	0	-5.2

the state of the s										+85°C	-24.2	7.27	16.35	-0.700	-1.825	-1.035	-1.440	-1.738	0	-5.2	
5 %		Pin				35,040,415	LIMITS					TEST	VOLTAG	E/CURRE	NT APPLI	ED TO PINS	LISTED BEL	ow:			(VCC)
		Under		0°C		+25°C			5°C				La Contraction	0.0			B E				Gnd
Characteristic	Symbol	Test	* Min	Max	Min	Тур	Max	Min	Max	Unit	I _{CS1}	ICS0A	ICS1A	VIHmax	VILmin	VIHAmin	VILAmax	VCL	VCH	VEE	
Power Supply Drain Current	1E	8	-	107	-1	78	97	-	107	mAdc	-	1 -	-		3,4,13,14	- 1	-	-14	-	8	1,16
Input Current	linH	3	-	525	-	-	330	-	330	μAdc	-	-	-	3	-	- 1	-		-	8	1,16
		7	-	40	-	-	25	-	25	μAdc	-	-	7-		-	-	-	- 1	7	8	1,16
Input Leakage Current	linL	4	-	32	0.5	1	20	-	20	μAdc	-	-	-	3,13,14	-	-	-	-	-	8	1,16
		7	-	32	-	-	20	-	20	μAdc	-	-	-	-	71	- A		7	-	8	1,16
Logic "1" Output Voltage	VOH	2	-1.060	-0.890	-0.960	-	-0.810	-0.890	-0.700	Vdc	-	- 1	3-	3,4	FA	- /	-	- 3	ps	8	1,16
Logic "0" Output Voltage	VOL	2	-1.890	-1.675	-1.850	-	-1.650	-1.825	-1.615	Vdc	7		1-5-	3,4	1-		1 - 1		4 -	8	1,16
Logic "1" Threshold Voltage	VOHA	2	-1.080	-	-0.980	-	- 1	-0.910	-	Vdc	-	7	1-	1	1	- 0	- 1	- 1	-	8	1,16
Logic "0" Threshold Voltage	VOLA	2	-	-1.655	-	-	-1.630	-	-1.595	Vdc	-	~	7	1	1		- 9	-	-	8	1,16
Bus Driver Zero Voltage Level	V _{Bus0}	7	-10	+10	-10	7 1	+10	-10	+10	mVdc	-	-	1-1	-1-1	. 1	-	-1	1-1	- 1	8	1,16
Bus Driver High Voltage Level	V _{BusH}	7	-0.915	-0.715	-0.970	1 7	-0.770	-1.030	-0.830	Vde	-	-	05	3,4	-		-1	1-0	e - '1	8	1,16
Bus Driver Low Voltage Level	VBusL	7	-1.708	-1.508	-1.818	3 3	-1.618	-1.938	-1.738	Vdc	7	-	-	3,4	-	-	A	-	-	8	1,16
Bus Driver Zero Threshold Voltage Level	V _{BusOA}	7	-30	10	-30		E-8	-30	-	mVdc	-	-		17	-	/A = 1	3,4	\ -	-	8	1,16
Bus Drivet High Threshold Voltage Level	V _{BusHA+}	7	-0.935	-0.695	-0.990	1 7	-0.750	-1.050	-0.810	Vdc	-	-	- 1	-5	-	3,4	-1-	-	7.84	8	1,16
Bus Driver High Threshold Voltage Level	V _{BusHA} -	7	-0.935	-0.695	-0.990	50	-0.750	-1.050	-0.810	Vdc	7	-	-	1	-		3,4	-	-	8	1,16
Bus Driver Low Threshold Voltage Level	V _{BusLA}	7	152	-1.488	15	N in	-1,598		-1.718	Vdc	7	-	-	Ť	-	3,4		-		8	1,16
	-		0.12		2 5	W 4.	H. 17	Di-	53						RE1*	RE2*	+0.31Vdc	Pulse In	Pulse Out	-3.2 V	+2.
Switching Times (50-ohm	t 3 - 7 +	7	1.0	3.1	1.0	1.5	2.9	1.0	3.2	ns	_		100	_	5	7	4	3	7	8	1.
load) Propagation Delay	13+7-	7	12 3	3.1	150	1.5	2.9	1.0	3.2		-	-	3	100		1	4	3	7	1	
	17-2-	2	1 6	4.5	63 1	2.5	4.3	1.0	4.7	10.00	0.4	Sec.	-	-			3,4	7	2		
	t7+2+	2	V	4.5	V	2.5	4.3	1.0	4.7	1	1.4	5-8	-	3 8			3,4	7	2		1
Rise Time	17 17 17	100	- 23	100	5 5	1 3	W-102	RS: 1	Til.	4	3.8	2 3									
(20% to 80%) Fall Time	t 2 +	2	1.1	4.4	1.1	2.0	4.2	1.1	4.6	ns	1	T	-	-	5	7	4	7	2	8	1,
(20% to 80%)	12-	2	1.1	3.5	1.1	2.0	3.3	1.1	3.6	ns		8-25	_	2	5	7	4	7	2	8	1,1

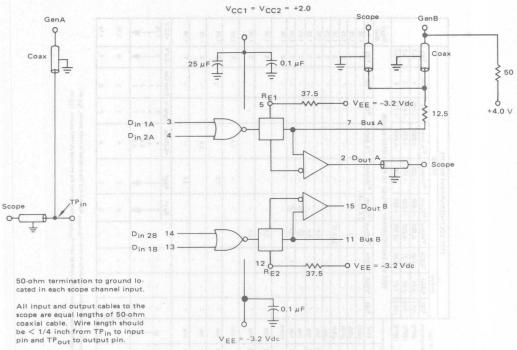
 $[\]textcircled{1} \quad \text{V_{OHA} and V_{OLA} threshold test limits remain the same with V_{IHmax} or V_{ILmin} applied.}$

V_{CL} = Low bias voltage for testing bus driver input loading V_{CH} = High bias voltage for testing bus driver input loading I_{CS1} = External current source input to the bus driver

ICSTA = Upper threshold level of external current source input to the bus driver ICSOA = Lower threshold level of external current source input to the bus driver

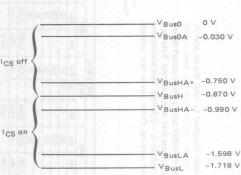
② VBusHA+ denotes the upper output threshold level with VIHAmin applied and the external current source, ICS off. 3 VBusHA- denotes the lower output threshold level with VILAmax applied and the external current source, ICS on.

^{*}RE1 = 37.5 ohms connected to VEE, RE2 = 37.5 ohms connected to VCC.

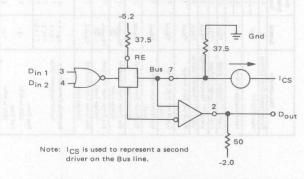


DC LOGIC LEVEL DESCRIPTION

The bus terminal (pin 7) can be at any one of three possible levels $V_{BusO}, V_{BusH},$ or V_{BusL} depending upon the combination of inputs applied. The MECL inputs (pins 3 and 4) cause the bus terminal to switch between two levels, V_{BusO} and V_{BusH} when the external current source (ICS) is off, and V_{BusH} and V_{BusL} when the external current source is on. The bus ouput threshold voltage levels caused by applying input threshold voltages V_{ILA} and V_{IHA} at pins 3 and 4, are also translated depending upon the state of ICS. These threshold levels are V_{BusOA} and V_{BusHA} when ICS is off, and V_{BusHA} and V_{BusLA} when ICS is on. These relative voltage levels are shown in the figure on the right.



DC TEST CONFIGURATION



APPLICATIONS INFORMATION

The MC10194 Dual Simultaneous Bus Driver/Receiver is designed for high speed data transfer over multi-port bus lines. Full duplex data transmission can improve system performance by increasing message density and overcoming the requirement to wait two line propagation delay times between messages.

Figure 1 illustrates system uses for the MC10194. One mode of operation is with two drivers on the bus line at locations X and Z. Any input to D_{in} X is seen at D_{out} Z one line propagation delay later. Similarly, any input to D_{in} Z is transmitted to D_{out} X. Each driver inhibits the data being sent on the bus from appearing at its receiver output, so full duplex signal transmission is possible. In addition, current source drivers allow two messages to pass on the same line so there are no timing restrictions between sending messages.

A second type of system operation is with a multiterminal bus as illustrated in Figure 1 by points X, Y, and Z. In this mode, any one terminal can transmit data and all other points will receive the message. Alternately, any two terminals can simultaneously exchange data, but the other receivers will not see valid data.

The MC10194 uses current source line driving and is designed to operate with a load to V_{CC} (normally ground). This load is usually the line termination resistors at each end of the line as shown in Figure 2. In addition, to match the driver to a given impedance line, an external resistor equal to one-half the line termination resistor value is connected between the RE output and V_{EE} .

When the circuit is used with a multi-terminal bus, each driver must have the resistor between R_E and V_{EE} , but the termination resistors are required only at each end of the bus line.

Each MC10194 driver in a package is capable of driving 75-ohm lines. Higher impedance lines may be used with no loss of performance if the line is properly matched with RE. If it is desirable to drive 50-ohm lines, both drivers in a package should be operated in parallel with each having 50-ohm resistors at RE and the driver outputs both connected to the 50-ohm bus line.

To allow very high data rates, the rise and fall times on the bus line are quite fast (typically 1.0 ns). With full duplex operation, it is possible to get a crosstalk pulse of several hundred mV at a receiver output. A 10-20 pF capacitor connected between each driver output and VEE will slow down the rise and fall times, greatly reduce any crosstalk pulse, and still give good system performance.

The adjustable current source drive feature of the MC10194 makes this circuit a useful output driver for many applications. For example, it is possible to drive the 50-ohm to ground load required by many interface systems. This driver will sink the 14 to 18 mA required to meet the AEC Committee specification for Nuclear Instrument Modules. The MC10114 MECL Line Receiver makes a good interface receiver for the MC10194 driver in these applications.

FIGURE 1 - MC10194 SYSTEM OPERATION

3

MC10195

MECL 10K SERIES

HEX INVERTER/BUFFER

HEX INVERTER/BUFFER

The MC10195 is a Hex Buffer Inverter which is built using six EXCLUSIVE NOR gates. There is a common input to these gates which when placed low or left open allows them to act as inverters. With the common input connected to a high logic level the MC10195 is a hex buffer, useful for high fanout clock driving and reducing stub lengths on long bus lines.

hears are the bring PD = 200 mW typ/pkg (No Load)

 $t_{pd} = 2.8 \text{ ns typ (B-Q)}$

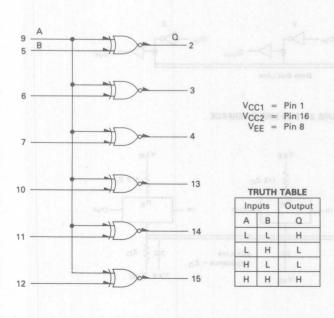
 $t_{pd} = 3.8 \text{ ns typ (A-Q)}$

 t_r , $t_f = 2.5 \text{ ns typ } (20\%-80\%)$

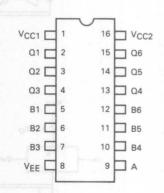
P SUFFIX
PLASTIC PACKAGE
CASE 648

L SUFFIX
CERAMIC PACKAGE
CASE 620

LOGIC DIAGRAM



PIN ASSIGNMENT



3-176

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to $-2.0\ volts$. Test procedures are shown for only selected inputs and outputs. Other inputs and outputs tested in the same manner.

	1	TEST V	OLTAGE \	ALUES	
			Volts		
@ Test Temperature	VIHmax	VILmin	VIHAmin	VILAmax	VEE
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

										.00	0.700	1.020	-1.000	1.440	0.2	4
		Pin		12.27	M	C10195	Test Limi	ts			VOLTAG	E APPLIE	ED TO PIN	IS LISTED	BELOW:	
		Under	-30	o°C		+25°C	LLC	+8!	5°C		VOLTAG	L AFFER	LD TOT III	3 LISTED	BELOW.	(VCC)
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	V _{IHmax}	VILmin	VIHAmin	VILAmax	VEE	Gnd
Power Supply Drain Current	1E	8	-	54	-	39	49	-	54	mAdc	-	- 5	-	-	8	1,16
Input Current	linH	5 9	_	425 460	_	-	265 290	_	265 290	μAdc μAdc	5 9	-6	-	§ -	8	1,16 1,16
	linL	5	0.5	_	0.5	-		0.3	-	μAdc	8	5	-	-	8	1,16
Logic "1" Output Voltage	VOH	2	-1.060	-0.890	-0.960	-	-0.810	-0.890	-0.700	Vdc	4 10	13-48	-	S - FN	8	1,16
Logic "0" Output Voltage	VOL	2	-1.890	-1.675	-1.850	W - 1	-1.650	-1.825	-1.615	Vdc	9	4-2	-	7 - 16	8	1,16
Logic "1" Threshold Voltage	VOHA	2	-1.080	-19	-0.980	22 -	-	-0.910	-	Vdc	7 7	7-3	1-	5	8	1,16
Logic "0" Threshold Voltage	VOLA	2	-	-1.655	-	C1 -	-1.630	-	-1.595	Vdc	4-3	3-5	5	P 2	8	1,16
Switching Time (50 ohm load) Propagation Delay	t5+2- t7-4+ t10+13+ t11-14- tg-14- t2+	2 4 13 14	1.1	4.2 V 5.2 4.7	1.1	2.8	4.0 5.0 4.5	1.1	4.4 5.4 5.0	ns	1- 4 -1 518 us	100 = 500 mg	9 5	Pulse Out 2 4 13 14 14 2	-3.2 Vdc	+2.0 Vdd
(20% to 80%)													3	g .		
Fall Time (20% to 80%)	t ₂₋	2	1.1	4.7	1.1	2.5	4.5	1.1	5.0	*	-		5	2	*	*

HEX "AND" GATE

The MC10197 provides a high speed hex AND function with strobe capability.

 $P_D = 200 \text{ mW typ/pkg (No Load)}$

 $t_{pd} = 2.8 \text{ ns typ (B-Q)}$

 $t_{pd} = 3.8 \text{ ns typ (A-Q)}$

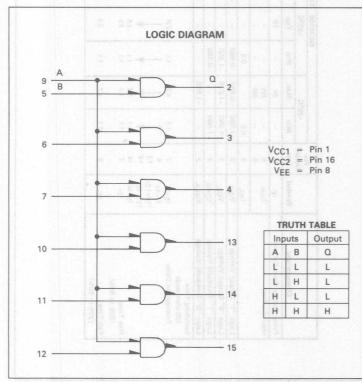
 t_r , $t_f = 2.5 \text{ ns typ } (20\%-80\%)$

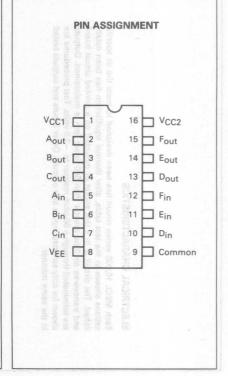
MECL 10K SERIES

HEX "AND" GATE









ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to $-2.0\ volts$. Test procedures are shown for only selected inputs and outputs. Other inputs and outputs tested in the same manner.

		TEST V	OLTAGE \	ALUES	
			Volts	1958.	
@ Test Temperature	VIHmax	VILmin	VIHAmin	VILAmax	VEE
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

										.00	0.700	1.020	1.000	1.440	0.2	1.0
[44][2]	220	Pin		12.0	M	C10197	Test Limi	ts		7.5	VOLTAG	SE APPLIE	D TO PIN	IS LISTED	BELOW-	
	12.22	Under	-30	o°C		+25°C		+8!	5°C	1 2 5	VOLTAG	JE AFFEIL		SLISIED	BLLOW.	(Vcc)
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	VIHmax	VILmin	VIHAmin	VILAmax	VEE	Gnd
Power Supply Drain Current	16	8	- 1	54	- 3	39	49	-	54	mAdc	5 3 8	里. 美 道	B - B	8-3	8	1,16
Input Current	linH	5 9	_	425 460	- 0	2 - 0	265 290	6 6	265 290	μAdc μAdc	5 9	8 1 1	0 - 3 0 - 3	1 8 1 8 1 8 1 8 1 8 1 8 1 8 1 8 1 8 1 8	8	1,16 1,16
	linL	5	0.5	-	0.5	-	0.3	- 8	2 -	μAdc	6 4 9	5	0 - 3	14 - 5	8	1,16
Logic "1" Output Voltage	VOH	2	-1.060	-0.890	-0.960	-	-0.810	-0.890	-0.700	Vdc	5,9	0 - 0	16 - 5	8 8 8	8	1,16
Logic "0" Output Voltage	VOL	2	-1.890	-1.675	-1.850	-	-1.650	-1.825	-1.615	Vdc	8 = 3	0 - 2	2 - 0	3 2 3	8	1,16
Logic "1" Threshold Voltage	VOHA	2	-1.080	-	-0.980	-90	9-3	-0.910	3 -	Vdc	9	3 - 5	5	8 = 5	8	1,16
Logic "0" Threshold Voltage	VOLA	2	D- 1	-1.655	-87	- %	-1.630	10 mm	-1.595	Vdc	9	-	44 - 25	5	8	1,16
Switching Time (50 ohm load)			8		0 141		百里至	五星		S E	200	+1.11Vdc	Pulse In	Pulse Out		+2.0 Vdc
Propagation Delay	t5+2+	2	1.1	4.2	1.1	2.8	4.0	1.1	4.4	ns	3 7 7	9	5	2	8	1,16
	t9+2+	2	1.1	5.3	1.1	3.5	5.0	1.1	5.5	E 1 8	8 8 8	5	9	3 4 6	155	
Rise Time (20% to 80%)	t ₂₊	2	1.1	4.7	1.1	2.5	4.5	1.1	5.0	2011	Sport Bush	9	5	Street Street		
Fall Time (20% to 80%)	t2-	2	1.1	4.7	1.1	2.5	4.5	1.1	5.0	1	1 1	9	5	* V *	E	1

MOTOROLA

MC10198

MONOSTABLE MULTIVIBRATOR

The MC10198 is a retriggerable monostable multivibrator. Two enable inputs permit triggering on any combination of positive or negative edges as shown in the accompanying table. The trigger input is buffered by Schmitt triggers making it insensitive to input rise and fall times.

The pulse width is controlled by an external capacitor and resistor. The resistor sets a current which is the linear discharge rate of the capacitor. Also, the pulse width can be controlled by an external current source or voltage (see applications information).

For high-speed response with minimum delay, a hi-speed input is also provided. This input bypasses the internal Schmitt triggers and the output responds within 2 nanoseconds typically.

Output logic and threshold levels are standard MECL 10,000. Test conditions are per Table 2. Each "Precondition" referred to in Table 2 is per the sequence of Table 1.

> $P_D = 415 \text{ mW typ/pkg (No Load)}$ tpd = 4.0 ns typ Trigger Input to Q 2.0 ns typ Hi-Speed Input to Q

Min Timing Pulse Width Max Timing Pulse Width Min Trigger Pulse Width	PW _{Qmin} PW _{Qmax} PW _T	10 ns typ ¹ >10 ns typ ² 2.0 ns typ
Min Hi-Speed	PWHS	3.0 ns typ
Trigger Pulse Width		
Enable Setup Time	t _{set}	1.0 ns typ
Enable Hold Time	thold	1.0 ns typ

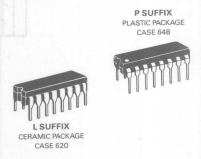
LOGIC DIAGRAM

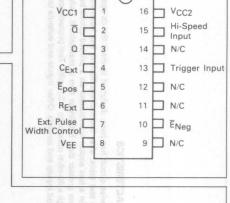
VEE

PIN ASSIGNMENT VCC1 [

MECL 10K SERIES

MONOSTABLE MULTIVIBRATOR

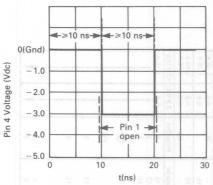




	6 0 0 4	V _{CC1} = V _{CC2} = V _{EE} =	Pin 16	Ext. Pulse 7 10 ENeg Width Control 9 9 N/C
5	R _{Ext} C _{Ext}			20 1 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2
7 ——	External Pulse Width Control	Market State of State		TRUTH TABLE
40		PIE	NPUT	OUTPUT
10 —	ENeg	Ē _{Po}	ENeg	82888860
	- 12 2 3 2 3 2 3 4 3 4 4 5 6 1	61101	1	\$1 CO. 10
13	Trigger Input Hi-Speed Q 2	L	H	Triggers on both positive & negative input slopes Triggers on positive input slope Triggers on negative input slope Trigger is disabled

 $^{^{1}}$ C_{Ext} = 0 (Pin 4 open), R_{Ext} = 0 (Pin 6 to VEE) 2 C_{Ext} = 10 μ F, R_{Ext} = 2.7 $k\Omega$

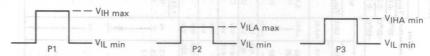




- 1. At t = 0 a.) Apply V_{IHmax} to Pin 5 and 10. b.) Apply V_{ILmin} to Pin 15. c.) Ground Pin 4.
- 2. At t ≥10 ns a.) Open Pin 1.
 - b.) Apply -3.0 Vdc to Pin 4. Hold these conditions for ≥10 ns.
- 3. Return Pin 4 to Ground and perform test as indicated in Table 2.

TABLE 2 — CONDITIONS FOR TESTING OUTPUT LEVELS

(See Table 1 for Precondition Sequence)



Pins 1, 16 = V_{CC} = Ground Pins 6, 8 = V_{EE} = 5.2 Vdc Outputs loaded 50 Ω to -2.0 Vdc

		Pin Cor	nditions	
Test P.U.T.	5	10	13	15
Precondition	1			+ N1 49
VOH 2			VIL min	ona II
VOH 3	1 58		P1	100
Precondition				
VOL 3	2.00		VIL min	k in in
V _{OL} 2			P1	
Precondition	the section that the	w Mi	and the	n 20 20 10
VOHA 2				VILA max
VOHA 3	3 10 10	DAYANG TANK		VIHA min
Precondition	1	3 3	3 3	
VOHA 2		- Aggst	V _{IL} min	111111111111111111111111111111111111111
VOHA 3	to Start		P3	
Precondition		A Section 1		
VOHA 2	t the state of the	101 2 2 1	P2	
VOHA 3			P3	2 8 318
Precondition			111	Property of the same of the sa
VOHA 2		VIH max	P2	
VOHA 3		VIH max	P3	
Precondition				
VOHA 2		V _{IH} max	P1	1 1

VIH max

P1

V_{OHA} 3

	1 3	Pin Con	ditions	F 18 F
Test P.U.T	. 5	10	13	15
Precondition	13		12 E	
VOHA 2		VIHA min	P1	
VOHA 3	8 8	VILA max	P1	F 2 -
Precondition				E E Y
VOLA 3	1 10			VILA max
VOLA 2				VIHA min
Precondition		4		-1-5
VOLA 2			VIL min	
VOLA 3	To la		VIL min	1 4 3
Precondition	11-11	1		
VOLA 3			P2	
VOLA 2			P3	148
Precondition	J. relig	1 1		医皮黄 夏
VOLA 3	1 98	VIH max	P2	13 3 5
VOLA 2	11:41	VIH max	P3	186
Precondition	12 Me			To E
VOLA 3	VIHA min	VIH max	P1	Ed & F
VOLA 2	VILA max	VIH max	P1	Lid. b
Precondition				
VOLA 3	VIH max	VIHA min	P1	
VOLA 2	VIH max		P1	

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to $-2.0 \ \text{volts}$. Test procedures are shown for only selected inputs and outputs. Other inputs and outputs tested in the same manner.

		TEST	VOLTAGE '	VALUES									
@Test		Volts											
Temperature	VIHmax	VILmin	VIHAmin	VILAmax	VEE								
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2								
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2								
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2								

3 3 9										+85°C	-0.700	-1.825	-1.035	-1.440	-5.2	13.7
1 11		Pin			MC1	0198 TI	EST LIMI	rs					Miles Say			94
		Under	-30	ос		+25°C		+85	°C		VOLTAGE APPLIED TO PINS LISTED BELOW:					(VCC)
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	VIHmax	VILmin	VIHAmin	VILAmax	VEE	Gnd
Power Supply Drain Current	1E	8		110	du:	80	100	-	110	mAdc	-	-		10	6,8	1,4,16
Input Current	linH	5.10	W 28	415 350	2015 S O 2		260 220		260 220	μAdc	5,10 13	(Em.). 11	-		6,8	1,4,16
	link	15	0.5	560 —	0.5	-	350	0.3	350	μAdc	15	5 - 5		- 8	1	*
Logic "1" Output Voltage	VOH	2 3	-1.060 -1.060	-0.890 -0.890	-0.960 -0.960	-1	-0.810 -0.810	-0.890 -0.890	-0.700 -0.700	Vdc Vdc	13 4	13	-	1110	6,8 6,8	1,4,16
Logic "0" Output Voltage	VOL	2 3	-1.890 -1.890	-1.675 -1.675	-1.850 -1.850	-	-1.650 -1.650	-1.825 -1.825	-1.615 -1.615	Vdc Vdc	13 4	13	-	-	6.8 6,8	1,4,16
Logic ''1'' Threshold Voltage	Vона	2 3	-1.080 -1.080		-0.980 -0.980	-	=	-0.910 -0.910		Vdc Vdc	- 10	9	15	15	6,8 6,8	1,16,4
Logic ''0'' Threshold Voltage	VOLA	2	=	-1.655 -1.655	-		-1.630 -1.630		-1.595 -1.595	Vdc Vdc	- 8	3	15	15	6,8 6,8	1,16,4
Switching Times	8	100				10		CH S			1.11 Vdc	3	Pulse In	Pulse Out	-3.2 Vdc	+2.0 V
Trigger Input	t _{T+Q+}	3	2.5 2.5	6.5 6.5	2.5 2.5	4.0	5.5 5.5	2.5	6.5 6.5	ns 	10	ğ I	13 13	3	6,8	1,16,
Hi-Speed Trigger Input	tHS+Q+	3	1.5	3.2	1.5	2.0	2.8	1.5	3.2		-	1	15	3		
Minimum Timing Pulse Width	PWQmin	3	T E	11	- (%)	10.0		81	- 10	1	Š -	1	-63	2		
Maximum Timing Pulse Width	PWQmax					-10		10.00	- 1	nis	+	8	- 9	3	FT	
Minimum Trigger Pulse Width	PWT	3			9	2.0				ns			13	3		
Minimum Hi-Speed Trigger Pulse Width	PWHS	3	-	- 10	1	3.0	2.5	1.5	40	er in the photo			15	3		
Rise Time (20% to 80%) Fall Time (20% to 80%) Enable Setup Time		3 3	1.5 1.5	4.0	1.5 1.5	1.0	3.5 3.5	1.5 1.5	4.0				5	3	2 0	0
Enable Setup Time Enable Hold Time	tsetup(E thold(E)	3	-		I I	1.0	_	_	- 4	1	ed _		5	3	1	1

es: 1 The monostable is in the timing mode at the time of this test.

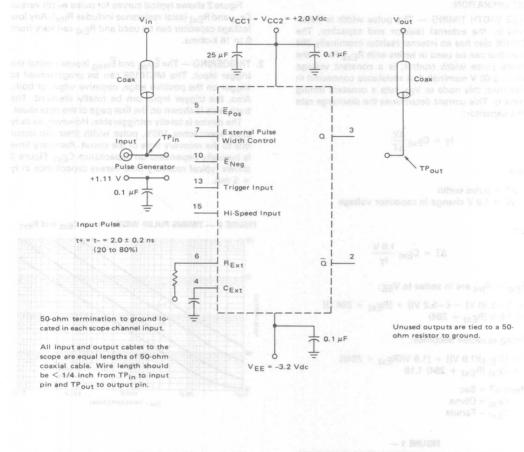
② CEXT = 0 (Pin 4 open) REXT 0 (Pin 6 tied to VEE)

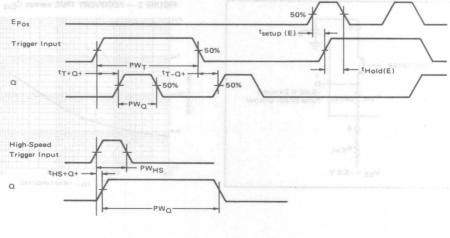
③ C_{EXT} 10 μF (Pin 4) R_{EXT} 2.7 k (Pin 6)

4 _____VIH

3-182

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS (a 25°C





APPLICATIONS INFORMATION

0 to 16 k-ohms.

= 5 mA.

CIRCUIT OPERATION:

1. PULSE WIDTH TIMING — The pulse width is determined by the external resistor and capacitor. The MC10198 also has an internal resistor (nominally 284 ohms) that can be used in series with R_{Ext}. Pin 7, the external pulse width control, is a constant voltage node (-3.60 V nominally). A resistance connected in series from this node to V_{EE} sets a constant timing current I_T. This current determines the discharge rate of the capacitor:

$$I_T = C_{Ext} \frac{\Delta V}{\Delta T}$$

where

 ΔT = pulse width

 $\Delta V = 1.9 V$ change in capacitor voltage

Then:

$$\Delta T = C_{Ext} \frac{1.9 \text{ V}}{I_T}$$

If Rext + Rint are in series to VEE:

$$I_T = [(-3.60 \text{ V}) - (-5.2 \text{ V})] \div [R_{Ext} + 284 \Omega]$$

 $I_T = 1.6 \text{ V/(}R_{Ext} + 284)$

The timing equation becomes:

$$\Delta T = [(C_{Ext})(1.9 \text{ V})] \div [1.6 \text{ V}/(R_{Ext} + 284)]$$

 $\Delta T = C_{Ext} (R_{Ext} + 284) 1.19$

where ΔT = Sec

 $R_{Ext} = Ohms$ $C_{Ext} = Farads$ Design (4)

Figure 2 shows typical curves for pulse width versus

CEXt and REXt (total resistance includes Rint). Any low leakage capacitor can be used and REXt can vary from

2. TRIGGERING — The Epos and ENeg inputs control the

trigger input. The MC10198 can be programmed to

trigger on the positive edge, negative edge, or both.

Also, the trigger input can be totally disabled. The

truth table is shown on the first page of the data sheet.

shows typical recovery time versus capacitance at IT

The device is totally retriggerable. However, as duty cycle approaches 100%, pulse width jitter can occur due to the recovery time of the circuit. Recovery time is basically dependent on capacitance CExt. Figure 3

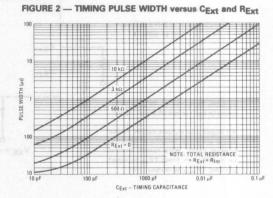


FIGURE 1 —

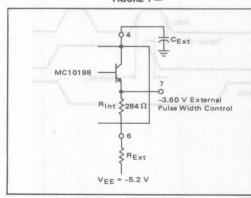
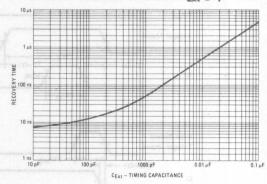
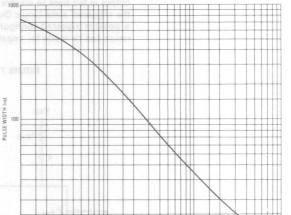


FIGURE 3 - RECOVERY TIME versus CExt @ IT = 5 mA



3. HI-SPEED INPUT — This input is used for stretching figure 5 — PULSE WIDTH versus I_T (a C_{Ext} = 13 pF very narrow pulses with minimum delay between the 1000 output pulse and the trigger pulse. The trigger input should be disabled when using the high-speed input. The MC10198 triggers on the rising edge, using this input, and input pulse width should narrow, typically less than 10 nanoseconds.



IT - TIMING CURRENT

USAGE RULES:

- 1. Capacitor lead lengths should be kept very short to minimize ringing due to fast recovery rise times.
- 2. The E inputs should not be tied to ground to establish a high logic level. A resistor divider or diode can be used to establish a -0.7 to -0.9 voltage level.
- 3. For optimum temperature stability; 0.5 mA is the best timing current IT. The device is designed to have a constant voltage at the EXTERNAL PULSE WIDTH CONTROL over temperature at this current value.
- 4. Pulse Width modulation can be attained with the EXTERNAL PULSE WIDTH CONTROL. The timing current can be altered to vary the pulse width. Two schemes are:
 - (a) The internal resistor is not used. A dependent current source is used to set the timing current as shown in Figure 4. A graph of pulse width versus timing current (CExt = 13 pF) is shown in Figure 5.

(b) A control voltage can also be used to vary the pulse width using an additional resistor (Figure 6). The current $(I_T + I_C)$ is set by the voltage drop across $R_{Int} + R_{Ext}$. The control current IC modifies IT and alters the pulse width. Current IC should never force IT to zero. RC typically 1 kΩ.

FIGURE 4 -

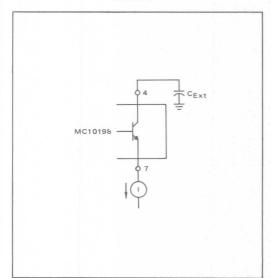
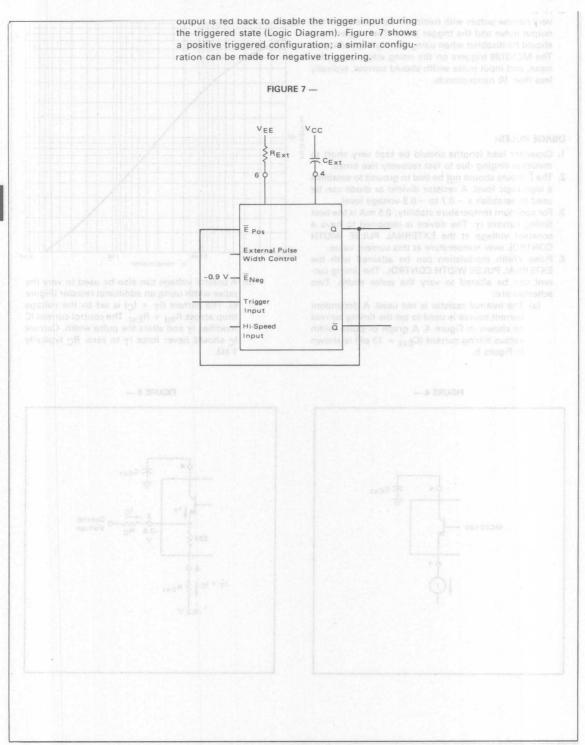


FIGURE 6 -





DUAL 3-INPUT 3-OUTPUT "OR" GATE

The MC10210 is designed to drive up to six transmission lines simultaneously. The multiple outputs of this device also allow the wire "OR" -ing of several levels of gating for minimization of gate and package count.

The ability to control three parallel lines with minimum propagation delay from a single point makes the MC10210 particularly useful in clock distribution applications where minimum clock skew is desired.

PD = 160 mW typ/pkg (No Loads)

tpd = 1.5 ns typ (All Output Loaded)

 t_r , $t_f = 1.5$ ns typ (20%–80%)

MECL 10K SERIES

DUAL 3-INPUT 3-OUTPUT "OR" GATE

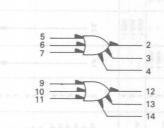
> P SUFFIX PLASTIC PACKAGE CASE 648



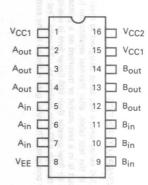
CASE 620



LOGIC DIAGRAM



V_{CC1} = Pin 1, 15 V_{CC2} = Pin 16 V_{EE} = Pin 8 **PIN ASSIGNMENT**



3-188

		TEST	OLTAGE VA	LUES	31
			(Volts)	6.0	. 8
@ Test Temperature	VIH max	VIL min	VIHA min	VILA max	VEE
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

										+85°C	-0.700	-1.825	-1.035	-1.440	-5.2	1 1
		Pin			N	1C10210	Test Lim	its	THE VIEW		TEOT	01 TA OF AD	N IED TO DIA	C. LICTED DEL	OW	
		Under	-30	o°C		+25°C		+8!	5°C		IEST VI	DL TAGE API	PLIED TO PIN	S LISTED BEL	.Ow:	(Vcc
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	VIH max	VIL min	VIHA min	VILA max	VEE	Gnd
Power Supply Drain Current	1E	8	-	42	_	-	38	-	42	mAdc	-	-	-	-	8	1,15,1
Input Current	linH	5,6,7	-	650	_	-	410	-	410	μAdc		-	-	-	8	1,15,
	linL	5,6,7	0.5	-	0.5	-	-	0.3	-	μAdc	-	1 2	8 -8 5	ğ -	8	1,15,
Logic "1" Output Voltage	VOH	2 3 4	-1.060 -1.060 -1.060	-0.890 -0.890 -0.890	-0.960 -0.960 -0.960	_	-0.810 -0.810 -0.810	-0.890 -0.890 -0.890	-0.700 -0.700 -0.700	Vdc Vdc Vdc	5 6 7	10 10 10 10 10 10 10 10 10 10 10 10 10 1	5 77 S	8 -	8 8 8	1,15, 1,15, 1,15,
Logic ''0'' Output Voltage	VOL	2 3 4	-1.890 -1.890 -1.890	-1.675 -1.675 -1.675	-1.850 -1.850 -1.850	-	-1.650 -1.650 -1.650	-1.825 -1.825 -1.825	-1.615 -1.615 -1.615	Vdc Vdc Vdc		ACTOR 20 Dis	1 1/2	i E	8 8 8	1,15, 1,15, 1,15,
Logic ''1'' Threshold Voltage	Vона	2 3 4	-1.080 -1.080 -1.080	-	-0.980 -0.980 -0.980	- ,	-	-0.910 -0.910 -0.910	-	Vdc Vdc Vdc	(a-	RUS III	5 6 7		8 8 8	1,15, 1,15, 1,15,
Logic "0" Threshold Voltage	VOLA	2 3 4	-	-1.655 -1.655 -1.655	-	-	-1.630 -1.630 -1.630	-	-1.595 -1.595 * -1.595	Vdc Vdc Vdc	199	Wilder E 100		5 6 7	8 8 8	1,15, 1,15, 1,15,
Switching Times (50-ohm load)		31	Us							- 6	5 %	Dille of the second	Pulse In	Pulse Out	-3.2 V	+2.0
Propagation Delay	t5+2+ t5-2- t5+3+ t5-3- t5+4+ t5-4-	2 2 3 3 4 4	1.0	2.6	1.0	1.5	2.5	1.0	2.8	ns	adada Vahala ba	n Inioq sign oliqqu maku	5	2 2 3 3 4 4	8	1,15,
Rise Time (20 to 80%)	t ₂₊ t ₃₊ t ₄₊	2 3 4	-71	a na								1000	Same of the confict	2 3 4		
Fall Time (20 to 80%)	t ₂₋ t ₃₋ t ₄₋	2 3 4	*	V	•		*	l v	*	1	9-	tight aptroi	TO DE	2 3 4		

^{*}Individually test each input using the pin connections shown.



DUAL 3-INPUT 3-OUTPUT "NOR" GATE

The MC10211 is designed to drive up to six transmission lines simultaneously. The multiple outputs of this device also allow the wire "OR"-ing of several levels of gating for minimization of gate and package count.

The ability to control three parallel lines with minimum propagation delay from a single point makes the MC10211 particularly useful in clock distribution applications where minimum clock skew is desired.

P_D = 160 mW typ/pkg (No Loads)

tpd = 1.5 ns typ (All Output Loaded)

 t_r , $t_f = 1.5 \text{ ns typ } (20\%-80\%)$

MECL 10K SERIES

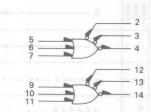
DUAL 3-INPUT 3-OUTPUT "NOR" GATE

> P SUFFIX PLASTIC PACKAGE



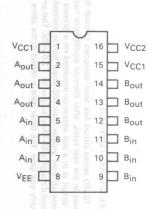
L SUFFIX CERAMIC PACKAGE CASE 620 CASE 648

LOGIC DIAGRAM



V_{CC1} = Pin 1, 15 V_{CC2} = Pin 16 V_{EE} = Pin 8

PIN ASSIGNMENT



3-189

		TEST \	OLTAGE VA	LUES	Bust
			(Volts)	SI	53
@ Test Temperature	VIH max	VIL min	VIHA min	VILA max	VEE
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2
	1				

		Pin			N	IC10211	Test Lim	its		- THE PERSON	TEST VOLTAGE APPLIED TO PINS LISTED BELOW:		OW.			
		Under	-30	o°C		+25°C		+85	°C		I IEST VI	JL TAGE AP	PLIED TO PIN	S LISTED BEL	.Ow.	(VCC)
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	VIH max	VIL min	VIHA min	VILA max	VEE	Gnd
Power Supply Drain Current	1E	8	-	42	-	30	38	-	42	mAdc		-	= 1		8	1,15,16
Input Current	linH	5,6,7		650	-	-	410	-	410	μAdc		-	-	-	8	1,15,16
	linL	5,6,7	0.5	-	0.5	-	- 1	0.3	-	μAdc	-			-	8	1,15,16
Logic "1" Output Voltage	VOH	2 3 4	-1.060 -1.060 -1.060	-0.890 -0.890 -0.890	-0.960 -0.960 -0.960	-	-0.810 -0.810 -0.810	-0.890 -0.890 -0.890	-0.700 -0.700 -0.700	Vdc Vdc Vdc	=	TO DE			8 8 8	1,15,16 1,15,16 1,15,16
Logic "0" Qutput Voltage	VOL	2 3 4	-1.890 -1.890 -1.890	-1.675 -1.675 -1.675	-1.850 -1.850 -1.850	-	-1.650 -1.650 -1.650	-1.825 -1.825 -1.825	-1.615 -1.615 -1.615	Vdc Vdc Vdc	5 6 7	turn.	79.0		8 8 8	1,15,16 1,15,16 1,15,16
Logic ''1'' Threshold Voltage	Vона	2 3 4	-1.080 -1.080 -1.080	-	-0.980 -0.980 -0.980			-0.910 -0.910 -0.910	-	Vdc Vdc Vdc	1	1201		5 6 7	8 8 8	1,15,16 1,15,16 1,15,16
Logic ''0'' Threshold Voltage	VOLA	3 4	101	-1.655 -1.655 -1.655	-	=	-1.630 -1.630 -1.630	-	-1.595 -1.595 -1.595	Vdc Vdc Vdc	8-	MODE PA MO	5 6 7		8 8 8	1,15,16 1,15,16 1,15,16
Switching Times (50-ohm load)										8 1		10	Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t5+2- t5-2+ t5+3- t5-3+ t5+4- t5-4+	2 2 3 3 4 4	1.0	2.6	1.0	1.5	2.5	1.0	2.8	ns		dought and a	5	2 2 3 3 4 4	8	1,15,16
Rise Time (20 to 80%)	t ₂₊ t ₃₊ t ₄₊	2 3 4	-100								1 1	ACTUAL OF STREET	Mush s lengy	2 3 4		
Fall Time (20 to 80%)	t2- t3- t4-	2 3 4	1		1		*		*		0-	5 5	A STAN	2 3 4		

^{*}Individually test each input using the pin connections shown.



HIGH SPEED DUAL 3-INPUT 3-OUTPUT OR/NOR GATE

The MC10212 is designed to drive up to six transmission lines simultaneously. The multiple outputs of this device also allow the wire "OR"-ing of several levels of gating for minimization of gate and package count.

The ability to control three parallel lines with minimum propagation delay from a single point makes the MC10212 particularly useful in clock distribution applications where minimum clock skew is desired.

PD = 160 mW typ/pkg (No Load)

t_{pd} = 1.5 ns typ (All Outputs Loaded)

 t_r , $t_f = 1.5$ ns typ (20% to 80%)

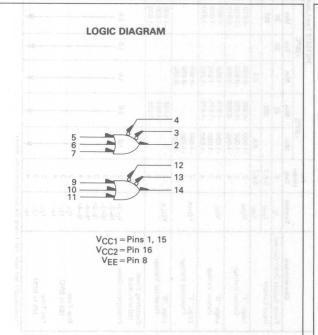
MECL 10K SERIES

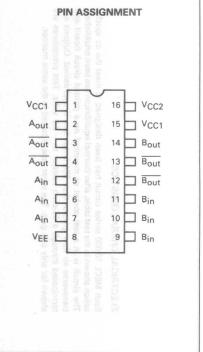
HIGH SPEED DUAL 3-INPUT 3-OUTPUT OR/NOR GATE

P SUFFIX PLASTIC PACKAGE CASE 648



CERAMIC PACKAGE CASE 620





Each MECL 10,000 series circuit has been designed to meet the dc specification shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gate is tested in the same manner.

		TEST \	OLTAGE VA	LUES	
			(Volts)	Sec. 191	
@ Test Temperature	VIH max	VIL min	VIHA min	VILA max	VEE
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

										100 C	-0.700	-1.825	-1.035	-1.440	-5.2	
					P	VIC 1021	2 Test Limi	ts							0111	-
		Pin Under	-30	ос		+25°C		+85	5°C		TEST V	OLTAGE AP	PLIED TO PIN	S LISTED BEL	.Ow:	(VCC)
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	VIH max	VIL min	VIHA min	VILA max	VEE	Gnd
Power Supply Drain Current	1 _E	8		42		30	38		42	mAdc	1016		-	- 1	8	1,15,16
Input Current	linH	5,6,7	-	650		-	410	i e di	410	μAdc	5,6,7*	0.34	23		8	1,15,16
	linL	5,6,7	0.5		0.5	-	- 1	0.3	1	μAdc	- 1	5,6,7*	0 8		8	1,15,16
Logic "1" Output Voltage	VOH	2 3 4	-1.060 -1.060 -1.060	-0.890 -0.890 -0.890	-0.960 -0.960 -0.960	-	-0.810 -0.810 -0.810	-0.890 -0.890 -0.890	-0.700 -0.700 -0.700	Vdc Vdc Vdc	5		olle o	=	8 8 8	1,15,16 1,15,16 1,15,16
Logic "0" Output Voltage	VOL	2 3 4	-1.890 -1.890 -1.890	-1.675 -1.675 -1.675	-1.850 -1.850 -1.850		-1.650 -1.650 -1.650	-1.825 -1.825 -1.825	-1.615 -1.615 -1.615	Vdc Vdc Vdc	- 5 5	100	Paragonia de la constanta de l		8 8 8	1,15,16 1,15,16 1,15,16
Logic "1" Threshold Voltage	VOHA	2 3 4	-1.080 -1.080 -1.080		-0.980 -0.980 -0.980			-0.910 -0.910 -0.910		Vdc Vdc Vdc	(B) -	Anne e	5 18 18	5 5	8 8 8	1,15,16 1,15,16 1,15,16
Logic "0" Threshold Voltage	VOLA	2 3 4	1	-1.655 -1.655 -1.655	2	-	-1.630 -1.630 -1.630		-1.595 -1.595 -1.595	Vdc Vdc Vdc	8 -	# 293 # 293	5 5	5	8 8 8	1,15,16 1,15,16 1,15,16
Switching Times (50-ohm load)	. /	1	1	J						900	lo .	2800	Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t5+2+ t5-2- t5+3- t5-3+ t5+4- t5-4+	2 2 3 3 4 4	1.0	2.6	1.0	1.5	2.5	1.0	2.8	ns qui an a	NA MW 88	dala indiluta	5 0 9 8 8 8 8	2 2 3 3 4 4	8	1,15,16
Rise Time (20 to 80%)	t ₂₊ t ₃₊ t ₄₊	2 3 4	100							11 11	4 -	100		2 3 4		
Fall Time (20 to 80%)	t2- t3- t4-	2 3 4		+		+				4	<u> </u>	15 17 18 18 18 18 18 18 18 18 18 18 18 18 18	iga co ougly	2 3 4		

^{*}Individually test each input using the pin connections shown.



MC10216

HIGH SPEED TRIPLE LINE RECEIVER

The MC10216 is a high speed triple differential amplifier designed for use in sensing differential signals over long lines. The base bias supply (VBB) is made available at pin 11 to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necessary.

Active current sources provide the MC10216 with excellent common mode noise rejection. If any amplifier in a package is not used, one input of that amplifier must be connected to VBB (pin 11) to prevent upsetting the current source bias network.

Complementary outputs are provided to allow driving twisted pair lines, to enable cascading of several amplifiers in a chain, or simply to provide complement outputs of the input logic function.

P_D = 100 mW typ/pkg (No Load)

t_{pd} = 1.8 ns typ (Single ended)

= 1.5 ns typ (Differential)

LOGIC DIAGRAM

 t_r , $t_f = 1.5 \text{ ns typ } (20\%-80\%)$

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MECL 10K SERIES

HIGH SPEED TRIPLE LINE RECEIVER

P SUFFIX PLASTIC PACKAGE **CASE 648**

PIN ASSIGNMENT



CERAMIC PACKAGE CASE 620





VBB

15 11

VCC1 [16 VCC2 Aout [Cout Cout Aout 14 Ain 13 🗖 C_{in} 12 Cin Bout 11 VBB 10 🔲 Bin Bout 7 9 Bin VEE 8

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

3 8 22		TE	ST VOLTAGE	VALUES		255
3 4			(Volts)			197
@ Test Temperature	V _{IH} max	VIL min	V _{IHA} min	VILA max	VBB	VEE
-30°C	-0.890	-1.890	-1.205	-1.500	From	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	Pin	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	11	-5.2

										+85°C	-0.700	-1.825	-1.035	-1.440	11	-5.2	-
		Pin			N	C10216	Test Lim	its				TEST VOLT	ACE ABBLIEF	TO BING BE	1.00		
		Under	-3	0°C		+25°C		+8	5°C		TEST VOLTAGE APPLIED TO PINS BELOW:						(Vcc)
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	VIH max	VIL min	VIHA min	VILA max	VBB	VEE	Gnd
Power Supply Drain Current	1E	8	-	27	-	20	25		27	mAdc	4,9,12	- 4	3 5	4-10	5,10,13	8	1,16
Input Current	linH	4	-	180	-	-	115	- 1	115	μAdc	4	9,12	9.9	F 55 Ta 65	5,10,13	8	1,16
	СВО	4 9	_	1.5 1.5	-	-	1.0		1.0 1.0	μAdc μAdc	1 5	9,12 4,12	9 5	182,5	5,10,13 5,10,13	8,4 8,9	1,16 1,16
High Output Voltage	VOH	2 3	-1.060 -1.060	-0.890 -0.890	-0.960 -0.960	_	-0.810 -0.810	-0.890 -0.890	-0.700 -0.700	Vdc Vdc	9,12	9,12	1 2		5,10,13 5,10,13	8	1,16 1,16
Low Output Voltage	VOL	2 3	-1.890 -1.890	-1.675 -1.675	- 1.850 - 1.850	-	-1.650 -1.650	-1.825 -1.825	-1.615 -1.615	Vdc Vdc	9,12	9,12	m 3	123 5	5,10,13 5,10,13	8	1,16 1,16
High Threshold Voltage	VOHA	2 3	-1.080 -1.080	- 20-05	-0.980 -0.980	=	_	-0.910 -0.910	12	Vdc Vdc	9,12	9,12	4	4	5,10,13 5,10,13	8	1,16 1,16
Low Threshold Voltage	VOLA	2 3	1 1	-1.655 -1.655	_	=	-1.630 -1.630	Ξ	-1.595 -1.595	Vdc Vdc	9,12	9,12	- 4	4 -	5,10,13 5,10,13	8	1,16 1,16
Reference Voltage	VBB	- 11	-1.420	-1.280	-1.350	-	-1.230	-1.295	-1.150	Vdc	- 8	是是門具	景 年 級	12-2	5,10,13	8	1,16
Switching Times (50-ohm Load)		-4	7 7 7	43			- 8		Ŕ		1		Pulse In	Pulse Out	2.5	-3.2 Vdc	+2.0 Vdc
Propagation Delay	t ₄₊₂₊ t ₄₋₂₋ t ₄₊₃₋ t ₄₋₃₊	2 2 3 3	1.0	2.6	1.0	1.8*	2.5	1.0	2.8	ns		A DESCRIPTION OF THE PROPERTY	4 5 8 ege	2 2 3 3	5,10,13	8	1,16
Rise Time (20% to 80%)	t ₂₊	2				1.5	4	1			1 - 9		19 19 18 1	3	1 2		
Fall Time (20% to 80%)	t2- t3-	2 3	*	+	V	•	+	¥	V	+	- 98		9 1 8	2 3		1	1

^{*}Delay is 1.5 ns when inputs are driven differentially Delay is 1.8 ns when inputs are driven single ended

The MC10231 is a dual master-slave type D flip-flop. Asynchronous Set (S) and Reset (R) override Clock (CC) and Clock Enable (C_F) inputs. Each flip-flop may be clocked separately by holding the common clock in the low state and using the enable inputs for the clocking function. If the common clock is to be used to clock the flip-flop, the Clock Enable inputs must be in the low state. In this case, the enable inputs perform the function of controlling the common clock.

The output states of the flip-flop change on the positive transition of the clock. A change in the information present at the data (D) input will not affect the output information at any other time due to master-slave construction.

 $P_D = 270 \text{ mW typ/pkg (No Load)}$

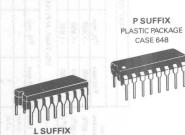
 $t_{pd} = 2 \text{ ns typ}$

t_{Tog} = 225 MHz typ

 t_r , $t_f = 2.0 \text{ ns typ } (20\%-80\%)$

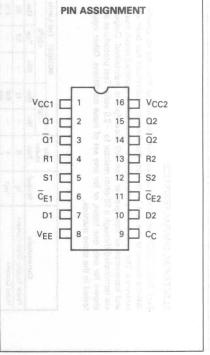
MECL 10K SERIES

HIGH SPEED DUAL TYPE D **MASTER-SLAVE FLIP-FLOP**



CERAMIC PACKAGE CASE 620

LOGIC DIAGRAM D1 01 Q1 VCC1 = Pin 1 VCC2 = Pin 16 CC 9 VEE = Pin 8 R2 13 02 C_{E2} 11 D2 10 02 S2 12 **CLOCK TRUTH TABLE R-S TRUTH TABLE** CD Q_{n+1} S Qn+1 L φ Q_n L Q_n H H H H Н Н H L $\phi = Don't Care$ HH N.D. $C = \overline{C}_E + C_C$. N.D. = Not Defined A clock H is a clock transition from a low to a high state. 3-195



Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table after the thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs tested in the same manner.

	Ten Calif	TEST	VOLTAGE VALI	UES	Pro-
	1-257		(Volts)	빗듯	展
@ Test Temperature	VIH max	VIL min	VIHA min	VILA max	VEE
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

	3 3	Pin		3	MC102		t Limits		M. C	A SECOND	VC	DLTAGE APPI.	IED TO PINS LI	STED BELOW:	188	
	TD4	Under	-30			+25°C		7	5°C	10				30.53	- 55	(VCC)
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	VIH max	VIL min	VIHA min	VILA max	VEE	Gnd
Power Supply Drain Current	1E	8	-	72	-	52	65	- 1	72	mAdc	MAG -	-		-	8	1, 16
Input Current	linH	4	-	650	-	-	410	-	410	μAdc	4		-	-	8	1, 16
		5	-	650			410		410	-	5					-
		6		350 350		-	220	7.7	220	-	6					
		9	-	460		-	290		290	*	9		_		*	
Input Leakage Current	linL	4,5,*	13.	-	0.5	-	-	-	-	μAdc	-	F 20.00	-	61 (14)	8	1, 16 1, 16
Logic "1"		6,7,9*		-			-	-	-	μAdc	-	2 6 3	4 4 9 1	12 27 3	8	1, 16
Output Voltage	VOH	2 2†	-1.060 -1.060	-0.890 -0.890	-0.960 -0.960	-	-0.810 -0.810	-0.890	-0.700 -0.700	Vdc Vdc	5 7	551	1 2 2 3 3	莫望是	8	1, 16
Logic "0" Output Voltage	VOL	3 3t	-1.890 -1.890	-1.675 -1.675	-1.850 -1.850	-	-1.650 -1.650	-1.825 -1.825	-1.615 -1.615	Vdc Vdc	5 7	- 3-3-3	0 4 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5	3 3 6	8	1, 16 1, 16
Logic "1" Threshold Voltage	Vона	2 2†	-1.080 -1.080		-0.980 -0.980	Ξ	-	-0.910 -0.910	-	Vdc Vdc		518	5 7	9	8	1, 16 1, 16
Logic "O" Threshold Voltage	VOLA	3 3†	-	-1.655 -1.655	2	-	-1.630 -1.630		-1.595 -1.595	Vdc Vdc		6-3 8	5 7	9	8	1, 16 1, 16
Switching Times		1		-1	1						+1.11 Vdc	- Note -	Pulse In	Pulse Out	-3.2 Vdc	+2.0 Vd
Clock Input Propagation Delay	t9+2- t6+2+	2 2	1.5	3.4	1.5	2.0	3.3	1.6	3.7	ns	7	1 1 1	9	2 2	8	1, 16
Rise Time (20 to 80%)	t ₂₊	2	0.9	3.3	1.0	1.3	3.1	1.0	3.6	50	7	17 25 17	9	2	- 1	
Fall Time (20 to 80%)	t2-	2	0.9	3.3	1.0	1.3	3.1	1.0	3.6	*		F 5-2 8	9	2	2	
Set Input		7					123			-27 5	5	D B P T	5 2 2	4 5 6	20	
Propagation Delay	t5+2+	2	1.1	3.4	1.1	2.0	3.3	1.2	3.7	ns		2 2-3 3	5	2	8	1, 16
	t12+15+	15					1			4 2	6	2 9 2 6	12	15	30 B	
	t5+3+ t12+14-	3 14	1	-	A	-	-	V		- V	9	4 41 4	5	3	111	
Reset Input	12114		100	-	-	- 60	-		-	P 2	- 4	5 2 2 5	12	14	54 22	-
Propagation Delay	t4+2-	2	1.1	3.4	1.1	2.0	3.3	1.2	3.7	ns	P2 P2	0 3-60	4	2	8	1, 16
	t13+15-	15	1713	1	Z B	83	1		1	TIE	6	5 5-0 8	13	15	The 40	1
	t4+3-	3			O. A	W	V			- V	9	4 4 5 5	4	3		
Setup Time	t13+14+	7	1.5	· ·	1.0	- 4	. 4	1.5	V	25	- 9		6.7	14	8	1, 16
Hold Time	^t Setup		1.5	-			-	1.5	-	ns		W 2 0 P	45 35 35 35 35			
	[†] Hold	7	0.9	-	0.75	-	-	0.9		ns		0	6,7	2	8	1, 16
Toggle Frequency (Max)	fTog	2	200	-	200	225	-	200	-	MHz		A C C C	6	2	8	1, 16

^{*}Individually test each input; apply VIL min to pin under test.

VIL min

VIH max

 $^{^\}dagger$ Output level to be measured after a clock pulse has been applied to the $\overline{C}_{\mathsf{E}}$ input (pin 6)

HIGH SPEED 2 x 1 BIT ARRAY MULTIPLIER BLOCK

The MC10287 is a dual high speed iterative multiplier. It is designed for use as an array multiplier block. Each device is a modified full adder/subtractor that forms a single-bit binary product at each operand input of the adder. Internal carry lookahead is employed for high speed operation.

An addition or subtraction is selected by mode controls (M0, M1). The mode controls are buffered such that they can be grounded or taken to a standard high logic level to accomplish subtraction. When left open or taken to a low logic level, M0 and M1 cause addition.

 P_D = 400 mW typ/pkg (No Load) t_{pd} : (Outputs loaded 1 kΩ to V_{EE}) C0 to C2 = 1.7 ns typ a0 to C2 = 2.8 a0 to S0 = 2.7 b0 to S0 = 3.1 a0 to S1 = 3.9 b0 to S1 = 4.4

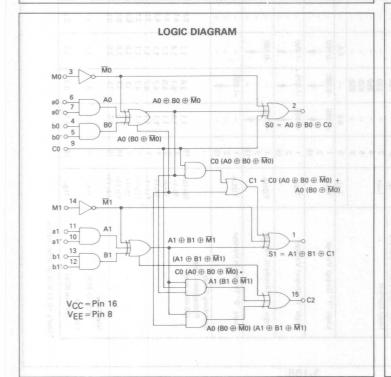
M0 to S1 = 8.7

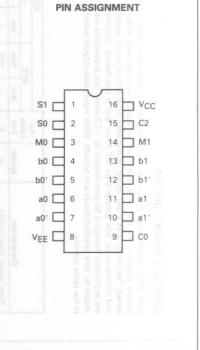
MECL 10K SERIES

HIGH SPEED 2 x 1 BIT ARRAY MULTIPLIER BLOCK

P SUFFIX
PLASTIC PACKAGE
CASE 648

L SUFFIX
CERAMIC PACKAGE
CASE 620





3

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to $-2.0\,\text{volts}.$ Test procedures are shown for only selected inputs and outputs. Other inputs and outputs tested in the same manner.

	2	TECT	OLTAGE '	VALUES	-	
		TEST V	Volts	VALUES	1	
@ Test Temperature	V _{IHmax}	VILmin	VIHAmin	VILAmax	VEE	
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2	
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2	
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2	

	E 9 3	Pin	14		N	1C10287	Test Limit	s O	1000						251 0111	
		Under	-30	o°C		+25°C	5	+85	5°C		VOLTAG	E APPLIE	DTOPIN	SLISTED	BELOW:	(Vcc)
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	V _{IHmax}	V _{ILmin}	VIHAmin	V_{ILAmax}	VEE	Gnd
Power Supply Drain Current	IE.	8	-	106	-	77	96	-	106	mAdc	-	-	-	-	8	16
Input Current	linH	3	-	320	-	-	200	-	200	μAdc	3	-	-	-	8	16
		4	-	350	-	-	220		220		4	-				
		6	-	425		-	265	-	265		6	-	-	-		
		9	-	650		-	410	-	410	1	9	-	-	-	1	1
	linL	3	0.5	-	0.5	-	-	0.3	-	μAdc	W-1- 2	3	576		8	16
Logic "1" Output Voltage	VOH	1	-1.060	-0.890	-0.960	-	-0.810	-0.890	-0.700	Vdc	5,9	8-16	0-2	-	8	16
	() () () () ()	2				-					9	w - 1	3-53	- 1		
6 8	9 %	15	- 81	1	1	-	1	1	1	1	6,9,10	0 - 9		-	1	1
Logic "0" Output Voltage	VOL	1	-1.890	-1.675	-1.850	-	-1.650	-1.825	-1.615	Vdc	9 47 9	3- 8	70 9	-	8	16
		2	BLA			-	1				209	8- 3	256	7		W
		15		1	1	-	1	1	1	1	9 -7 2	9- 5	D-46 5		1	1
Logic "1" Threshold Voltage	VOHA	31	-1.080	-	-0.980	-	-	-0.910	-	Vdc	6,7	8- 8	9	- 7	8	16
		2	-11			-			6	1	2.4	9- 1	4	- 1		
		15		-	1	-	- 2	1	# 8	1	6,7,10,11	-c- E	9		1	1
Logic "0" Threshold Voltage	VOLA	1	-	-1.655	-	-	-1.630	-	-1.595	Vdc	6,7	11- 0	5-35 5	9	8	16
		2	-		-			-			9 - 3	0 - 3	1 -2 1	4		
		15	-	1	-	- 1	1	-	3 25		6,7,10,11	8-	N - 0	9		1
Switching Times Propagation Delay		T.		8					2 5 6		+1.11 V	+0.31 V	Pulse In	Pulse Out	-3.2 Vdc	+2.0 Vdc
(50 ohm load)	t9+15+	15	1.1	3.6	1.1	2.0	3.4	1.1	3.7	ns	- 3	E . B	9	15	8	16
	t6-1-	1	1.4	6.1	1.4	4.5	5.8	1.4	6.4		3	2 19 3	6	1		
	t4+2-	2	1.1	4.9	1.1	3.5	4.7	1.1	5.2		6	100	4	2	2	
	t4-1+	1	1.1	4.7	1.1	4.5	4.5	1.1	4.8		6	5 5 0	4	1 3		
	t11+1-	1	1.1	4.7	1.1	3.0	4.5	0 1:1 0	4.8		13	7 8 6	11	1		
	t13+1-	1.	1.1	4.7	1.1	3.5	4.5	1.1	4.8		3,9	EES	13	1		
	t3+1+	1	3.0	13	3.0	8.5	12.5	3.0	13.5	1 1	9	1261	3	1		
	t3+15+	15	2.5	13	3.0	8.0	12.5	2.5	13.5	9	9,14	Y DE	3	15		
# 12 12 12 12 12 12 12 12 12 12 12 12 12	¹ 14+15+	15	3.0	13	3.0	8.0	12.5	3.0	13.5		- 11	6 5 8	14	15	100	
Rise Time			TY Y	1	1 2. 3		42.3				9 0 3	E C	8 1		1 20	
(20% to 80%)	t15+	15	1.1	3.3	1.1	2.0	3.1	1.1	3.4		1 5 5 5	8 8 9	3	15		
Fall Time (20% to 80%)	t15-	15	1.1	3.3	1.1	2.0	3.1	1.1	3.4		1 1 1 1 1	2 3 5	3	15		

^{*}Apply +0.31 V to all other inputs.

3

APPLICATION INFORMATION

The MC10287 is a stand alone fully iterative dual multiplier cell. It is intended for use in parallel multiplier arrays where maximum speed is desired. Each cell is a modified gated adder/subtractor individually controlled by a mode select line. Internal carry lookahead (also called anticipated carry) is used to minimize sum and carry out delay times.

The mode controls are specifically buffered such that they can be grounded. Normally, MECL 10,000 device inputs should not be placed at ground to establish a high logic level. However, M0 and M1 can be used at ground potential for ease of layout in large arrays.

An array multiplier is defined as a multi-input, multioutput combinational logic circuit that forms the product of two binary numbers. Binary multiplication can be treated in two categories, that is, simple magnitude multiplication and 4-quadrant multiplication (requiring both positive and negative numbers).

MAGNITUDE BINARY MULTIPLICATION

Magnitude multiplication consists of the product of two binary numbers in which all digits are number bits (no sign bit). Magnitude representation then includes only positive numbers.

Thus, for a 4-bit number X the representation is:

$$X = x_3 x_2 x_1 x_0$$

A 4-bit by 4-bit product becomes:

$$Z = X \cdot Y = (x_3 x_2 x_1 x_0) \cdot (y_3 y_2 y_1 y_0)$$

The product consists of the sum of the single-bit products formed by this expression. The standard "paral-

TABLE 1 — TYPICAL MULTIPLY TIME FOR AN n-BIT BY

n-BIT BINARY MAGNITUDE ARRAY MULTIPLIER

lelogram" matrix of the single-bit products (or summands) can be written:

z₇ z₆ z₅ z₄ z₃ z₂ z₁ z₀

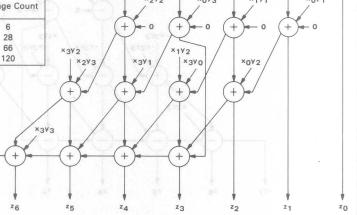
The MC10287 is used in an array summing the single-bit products to form the final result. It is observed that the arithmetic product of binary digits x_i and y_i is also the logical product (x_j times $y_i = x_j$ AND y_i). The AND function on the operand inputs of the MC10287 forms the single-bit products of the matrix directly and sums them internally. For magnitude binary multiplication, the MC10287 functions as a dual full adder (M0, M1 and both low).

The partial product array can be summed using a number of different techniques. The fastest technique is some form of matrix reduction scheme that prevents carry propagation until the final level of summation. Several of these schemes are discussed in detail in Reference 1.

As an example, if the matrix is rearranged and written in a different form:

FIGURE 1 — 4-BIT BY 4-BIT MAGNITUDE ARRAY MULTIPLIER

Number of Bits	Total Multiply Time (ns)	Package Count
4	14	6
8	25	28
12	39	66
16	44	120



A basic adder/subtractor can then handle all the varying situations that appear in the multiplication matrix. If the 2's complement matrix is rearranged:

Z1

- Z7 Z6 **Z**5 Z4 Z3 22 The adder/subtractor array for this configuration is shown in Figure 2. Care must be taken to insure that the proper mode of operation (add or subtract) appears at each summing node as a function of the positive and

negative weighted inputs.

The summand matrix can be altered different ways to speed up the multiplier array. Reference 2 discusses the algorithm used with the MC10287 in detail. Also, the techniques of Reference 1 also apply to 2's complement arrays using the MC10287.

Table 2 gives typical multiply times for 2's complement arrays for n-bit by n-bit multipliers.

TABLE 2 — TYPICAL MULTIPLY TIME FOR AN n-BIT BY n-BIT 2's COMPLEMENT ARRAY MULTIPLIER

Number of Bits	Total Multiply Time (ns)	Package Count
4	14	6
8	25	28
12	39	66
16	44	120

IMPROVED SWITCHING DELAYS

The specified ac switching delays are given for output loading of 50 Ω to -2 volts. With lower output current, propagation delays will be improved and decreased multiply times can result. For output loading of 1 kΩ to VFF, the following delays are typical.

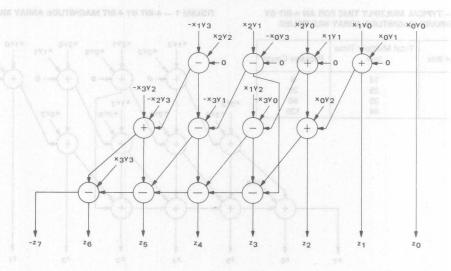
Input	Output	Delay (ns)
CO	m of b C2	rap bened.7ms
A0	C2	2.8
A0	SO SO	2.8
B0	S0	3.1
A0	a boulet \$1 ueos	3.9
B0	S1 S1	4.4
M0	S1 Sucys	8.7

REFERENCE AND ACKNOWLEDGEMENT

The techniques for implementing the MC10287 in multiplier arrays resulted from work done originally at M.I.T. Lincoln Laboratories. Also, applications information presented here developed in part from personal correspondence with P. Blankenship of Lincoln Labs. The following references are useful in developing multipliers using the MC10287:

- 1. A. Habibi and P. A. Wintz, "Fast Multipliers," IEEE Trans. Computers (Short Notes), Vol. C-19, Feb. 1970, pp. 153-157.
- 2. S. D. Pezaris, "A 40-ns 17-Bit by 17-Bit Array Multiplier," IEEE Trans. Computers, Vol. C-20, Number 4, April, 1971; pp. 442-447.

FIGURE 2 — 4-BIT BY 4-BIT 2's COMPLEMENT ARRAY MULTIPLIER



3

The summation of the partial products for this configuration is shown in Figure 1. The number of MC10287's for an n-bit by n-bit array is n(n-1)/2. Note also that the least significant product bit $(z_0 = x_0y_0)$ is formed by an individual AND gate (negative logic).

Table 1 gives package count and typical multiplication times for n-bit by n-bit magnitude multiplier arrays. The multiply times do not include wiring delays, and the package count does not include the gate for the least significant product bit.

FOUR-QUADRANT MULTIPLICATION

Sign-magnitude and 2's complement representations are commonly used for 4-quadrant multiplication. For sign-magnitude representation, the binary word consists of a sign bit and magnitude bits which indicate the absolute value of the number. For a 4-bit example:

For
$$X \cdot Y = Z$$

 $Z = X \cdot Y = (x_s x_2 x_1 x_0) \cdot (y_s y_2 y_1 y_0)$

An array multiplier for this representation consists of an (n-1)-bit by (n-1)-bit magnitude multiplier that produces the product of the magnitude bits of X and Y and of logic that produces the proper product sign bit $(z_S = x_S \bigcirc y_S)$.

2's complement representation also includes a sign bit which is a negative bit. That is:

$$X = -x_3 x_2 x_1 x_0$$

where x_3 is the sign bit. The product of two 4-bit 2's complement numbers becomes:

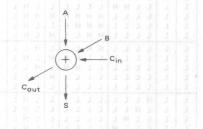
$$Z = X \cdot Y = (-x_3 x_2 x_1 x_0) \cdot (-y_3 y_2 y_1 y_0)$$

The matrix for this expression is:

$$-z_7$$
 z_6 z_5 z_4 z_3 z_2 z_1 z_0

The product is the sum of this array of single-bit products. However, notice that several summands are negative quantities. Therefore, they can not be simply added as is the magnitude binary multiplier. The subtraction capability of the MC10287 is utilized when considering these negative quantities.

A standard full adder is symbolized as:



in which all inputs are positive quantities. If one input is negative (such as B), the outputs C_{out} and S must be coded such that they can represent the 4 possible output conditions. If B can be a negative one or zero, the net output can then be:

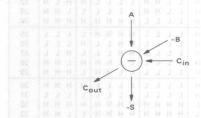
$$net output = \begin{cases} -1 \\ 0 \\ +1 \\ +2 \end{cases}$$

If Cout, whose weight is twice that of S, is assigned a positive value and S is a negative value, the above values can be represented:

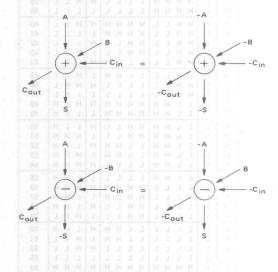
where:

$$-1 = 0 - 1
0 = 0 - 0
+1 = 2 - 1
+2 = 2 - 0$$

If the truth table is written and logic equations generated, the result is a subtractor. That is, a subtractor used in place of a full adder produces the proper outputs. The symbol for the subtractor is:



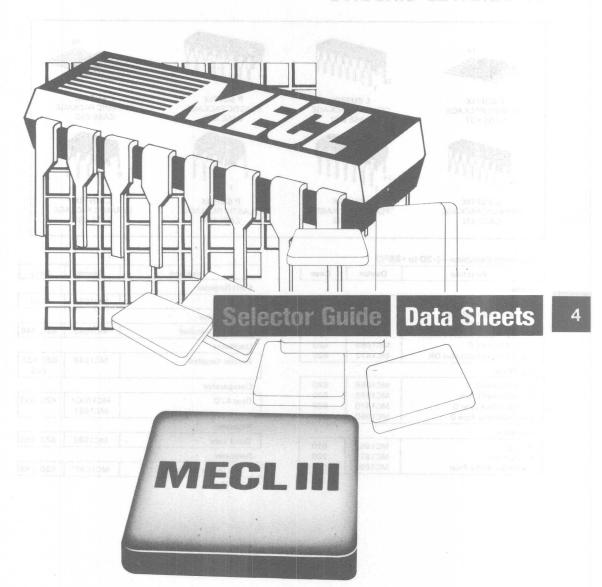
Also, if the input variables are multiplied by -1, the outputs also are multiplied by -1. Thus, the following devices are equivalent:



VI1	MO	b1 b1' a1 a1'	b0 b0'	a0 a0'	CO	SO	S1 C2	evitage	M1	MO	b1 b1' a1 a1'	b0 b0' a	a0 a0'	CO	S0 S1 C2	io is t
14	3	13 12 11 10	4 5	6 7	9	2	1 15	Word	14	3	13 12 11 10	4 5	6 7	9	2 1 15	Word
Н	Н	нннн	нн	нн	Н	Н	нн	0	L	Н	нннн	LLI	нн	Н	LHH	68
н	Н	нннн	нн	нн	L	L	LL	1	L	Н	нннн	LLI	H H	L	ннн	69
1	Н	нннн	нн	LL	Н	L	LL	2	L	Н	нннн	LL		H	ннн	70
	Н	нннн	НН	LL	L	Н		3	8.1	H	HHHH	HH		H	HLH	71 72
	Н	нннн	LL	нн	Н	L	1800 100	4	->Le	Н	The same of the same of					
	Н	нннн	LL	нн	L	100	нн	5	L	H	HHLL		H H	L	LHL	73 74
	H	H H H H	LL	LL	H		HH	6	L	Н	HHLL		LL	L	HHL	75
0	H	HHLL		НН	H		LL	8	io L	Н	HHLL		нн	Н	L L H	76
1	Н	HHLL		нн	L		H L	9	L	Н	HHLL	LL	н н	L	HLH	77
	Н	HHLL	нн	LL	н	L	HL	10	s/[ci	Н	HHLL	Co Car	LL	Н	HLH	78
1	Н	HHLL	нн	LL	L	Н	H L	11	KE	Н	HHLL		LL	L	LHL	79
	Н	HHLL	LL	НН	Н	L	LL	12	5 L 18	Н	LLHH	ALTONOUS DE LE	н н	H	H L H	80
	H	HHLL	LL	HH	L	H		13 14	l t	H	LLHH		HHL	H	LHL	81 82
1			LL		Н						F141VT164-0-01		0.4	2031	TOTAL COLUMN	10 011
	Н	HHLL	LL	LL	L		HL	15	L	H	LLHH		L L	H	HHL	83 84
	Н	LLHH	HH	HH	H	H	L H	16 17	L	Н	LLHH		НН	L	HLH	85
	Н	LLHH	нн	LL	H		нн	18	L	Н	LLHH		LL	н	HLH	86
	Н	LLHH	нн	LL	E	Н	нн	19	L	Н	LLHH	LL	LL	L	LHL	87
To the	Н	LLHH	LL	нн	Н	L	LH	20	at Inta	Н	LLLL	нн	нн	Н	HHL	88
	Н	LLHH		HH	L	100	LH	21	ra cla	Н	LLLL	HH	100	L	ULL	89
	Н	LLHH	LL	LL	H		LH	22	19.Ls	H	LLLL	HH	DAST-ALCO	H	HLL	90
	Н	LLHH	HH	LL	H		HH	23	L	H			HH	Н	LHL	92
			нн	нн	L	L	LL	25	L	Н	LLLL		нн	L	HHL	93
	H		НН	LL	H	L	LL	26	la L	Н			LL	Н	HHL	94
	н	LLLL	HH	LL	L	Н		27	L	Н	LLLL		LL	L	LLL	95
	Н	LLLL	LL	н н	Н	L	н н	28	L	L	нннн	The second of	H H	Н	ннн	96
	Н	LLLL	LL	HH	L	Н	нн	29	L	L	нннн	нн	нн	L	LHH	97
	Н	LLLL	LL	LL	Н	1	нн	30	L	L	нннн		LL	Н	LHH	98
	Н	LLLL	LL	LL	L	L	LL	31	L	L	нннн		LL	L	HLH	99
	L	H H H H	HH	HH	H	100	HH	32	L	L	H H H H		HH	H	HLH	100
	L	HHHH	НН	LL	H		НН	34	L	L	HHHH		LL	H	HLH	102
(1	Lo	нннн	нн	LL	t	Н	LL	35	LO	E	нннн		LL	L	LLH	103
	i.	H H H H		HH	H		HH	36	IO L	L	HHLL	100	HH	H	HLH	104
	L	нннн	LL	нн	L	100	LL	37	i L	L	HHLL	нн	н н	L	LLH	105
	L	нннн	LL	LL	Н	Н		38	L	L	HHLL		LL	Н	LLH	106
	L	нннн	LL	LL	L	L	LL	39	L	L	HHLL		LL	L	HHL	107
	L	HHLL	нн	НН	Н	Н	LL	40	L	L	HHLL		НН	Н	LLH	108
	L	HHLL	HH	HH	H	L	LL	41	L	L	HHLL		HH	L	HHL	109
	L	HHLL		LL	L	- 77	HL	42	L	L	HHLL		LL	L	LHL	111
	L	HHLL	LL	HH	H	L	LL	44	Ĺ	L	LLHH		H H	Н	HLH	112
	t	HHLL	LL	нн	L	Н	H L	45	L	L	LLHH	нн	нн	L	LLH	113
	L	HHLL	LL	LL	Н	Н		46	Ĺ	L	LLHH	FERSON FUNDSO	LL	Н	LLH	114
	L	HHLL	LL	LL	L	1	H L	47	L	L	LLHH		LL	L	HHL	115
	L	LLHH		HH	H		LH	48	L	L	LLHH		HH	H	LLH	116
	L	LLHH	нн		L	L	LH	49	L	L	LLHH	LL		L		117
	L	LLHH	HH	LL	H	H	L H	50 51	L	L	LLHH		LL	H	HHL	118 119
	L	LLHH	LL	HH	Н	L	LH	52	L	L	LLLL		HH	Н	HHL	120
	L	LLHH	LL	н н	L	Н	н н	53	L	L	LLLL	нн	нн	L	LHL	121
	L	LLHH	LL	LL	Н	Н	нн	54	L	L	LLLL	нн	LL	Н	LHL	122
	L	LLHH	LL	LL	L	L	н н	55	L	L	LLLL	H H		L	HLL	123
	L	LLLL	нн	HH	Н		H-H	56	L	L	LLLD	LL		Н	LHL	124
	L			HHLL	L		HH	57 58	L	L		LL	LL	H	HLL	125 126
	L	LLLL	НН	LL	L		LL	59	L	L		LL	LL	L	LLL	127
	L	LLLL	LL	нн	Н	L	нн	60	L	L	HLLL		LL	L	LHL	128
1	L			НН	L		LL	61	L	L	LHLL	LL	LE	L	LHL	128
	Ĺ	LLLL	LL	LL	Н	Н		62	Ĺ	L	LLHL	LL	LL	L	LHL	130
	L	LLLL	LL	LL	L		LL	63	L	L	LLLH	LL	LL	L	LHL	131
1	Н	нннн		НН	Н	Н	нн	64	L	L	LLLL			L	HLL	132
	Н	нннн		нн	L	L	LH	65	L	L	LLLL	LH	LL	L	HLL	133
	H	H H H H	HH		H	L	L H	66 67	L	L		LL	H L L H	L	HLL	134 135
J									L						HLL	

NECLHI

EGRATED CIRCUITS



MECL III INTEGRATED CIRCUITS

MC1600 Series (-30 to +85°C)



F SUFFIX CERAMIC PACKAGE CASE 607



L SUFFIX CERAMIC PACKAGE CASE 632



L SUFFIX CERAMIC PACKAGE CASE 620



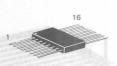
P SUFFIX PLASTIC PACKAGE CASE 646



P SUFFIX PLASTIC PACKAGE CASE 648



P SUFFIX PLASTIC PACKAGE CASE 626



F SUFFIX CERAMIC PACKAGE CASE 650



L SUFFIX CERAMIC PACKAGE CASE 693

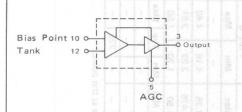
Function Selection—(-30 to +85°C)

Function	Device	Case
Gates		
Dual 4-Input OR/NOR	MC1660	620
Dual 4-5-Input OR/NOR	MC1688	620, 650
Quad 2-Input NOR	MC1662	620
Triple 2-Input Exclusive NOR	MC1674	620
Quad 2-Input OR	MC1664	620
Triple 2-Input Exclusive OR	MC1672	620
Flip-Flops	-)	
Dual Clocked R-S	MC1666	620
Dual Clocked Latch	MC1668	620
Master-Slave Type D	MC1670	620
UHF Prescaler Type D	MC1690	620
Counters		
Binary	MC1654	620
Bi-Quinary	MC1678	620
1 GHz Divide-by-Four	MC1699	620, 648

Function	Device	Case
Shift Register		
4-Bit Shift	MC1694	620
Multivibrator		
Voltage-Controlled	MC1658	620, 648
Oscillator		
Emitter Coupled	MC1648	607, 632 646
Comparator		5
Dual A/D	MC1650/ MC1651	620, 650
Receiver		
Quad-Line	MC1692	620, 650
Prescaler		
1 GHz Divide-by-Four	MC1697*	626, 693

MC1648/MC1648M

VOLTAGE-CONTROLLED OSCILLATOR



Input Capacitance = 6 pF typ

Maximum Series Resistance for L (External Inductance) = 50 Ω typ

Power Dissipation = 150 mW typ/pkg
(+5.0 Vdc Supply)

Maximum Output Frequency = 225 MHz typ

The MC1648 requires an external parallel tank circuit consisting of the inductor (L) and capacitor (C).

A varactor diode may be incorporated into the tank circuit to provide a voltage variable input for the oscillator (VCO). The MC1648 was designed for use in the Motorola Phase-Locked Loop shown in Figure 9. This device may also be used in many other applications requiring a fixed or variable frequency clock source of high spectral purity. (See Figure 2.)

The MC1648 may be operated from a +5.0 Vdc supply or a -5.2 Vdc supply, depending upon system requirements.

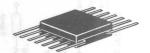
Supply Voltage	Gnd Pins	Supply Pins		
+5.0 Vdc	7, 8	1, 14		
-5.2 Vdc	1, 14	7, 8		



L SUFFIX CERAMIC PACKAGE CASE 632



P SUFFIX PLASTIC PACKAGE CASE 646



F SUFFIX CERAMIC PACKAGE CASE 607

FIGURE 1 - CIRCUIT SCHEMATIC

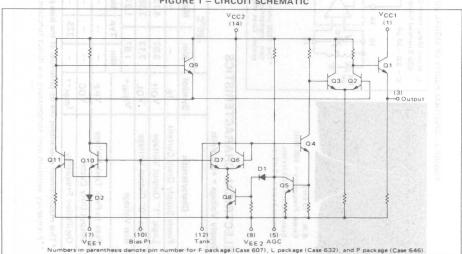
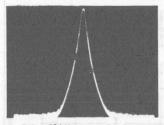
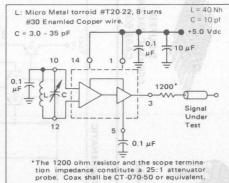


FIGURE 2—SPECTRAL PURITY OF SIGNAL OUTPUT FOR 200 MHZ TESTING



B.W. = 10 kHz
Center Frequency = 100 MHz
Scan Width = 50 kHz/div
Vertical Scale = 10 dB/div



	TE	ST VOLTAGE/CI	URRENT VALL	JES
@ Test	18 9 8 18		mAdc	
emperature	VIHmax	VILmin	Vcc	IL
	MC1648	. 9 3 3 5 1		
-30°C	+2.00	+1.50	5.0	-5.0
+25°C	+1.85	+1.35	5.0	-5.0
+85°C	+1.70	+1.20	5.0	-5.0
	MC1648M			
-55°C	+2.07	+1.57	5.0	-5.0
+25°C	+1.85	+1.35	5.0	-5.0
+125°C	+1.60	+1.10	5.0	-5.0

ELECTRICAL CHARACTERISTICS

Supply Voltage = +5.0 Volts

			-55°C	-	10	-30°C		1	+25°(+85°C		4	125°(С			
Characteristic	Symbol	Mir		Max	Min		Max	Mir		Max	Mir	1	Max	Min		Max	Unit	Conditions	
Power Supply Drain Current	IE	-		-8	_		_	-		41	9 -		_	-		-	mAdc	Inputs and outputs ope	
Logic "1" Output Voltage	Vон	3.93	2	4.13	3.955 4.185		4.185 4.0		4	4.25	4.1	1	4.36	4.16	3	4.40	Vdc	VILmin to Pin 12, IL	
Logic "0" Output Voltage	VOL	3.13	3	3.38	3.16	3	3.40	3.20	0	3.43	3.2	2 3	3.475	3.23	3	3.51	Vdc	VIHmax to Pin 12, IL	
Bias Voltage	VBias*	1.6	7	1.97	1.60		1.90	1.45	5	1.75	1.3	0	1.60	1.20		1.50	Vdc	V _{ILmin} to Pin 12.	
	1.132.1	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max			
Peak-to-Peak Tank Voltage	Vp.p	-	-	-	-	3 -	_	45	400	3-2		C-	D	-	F	-	mV		
Output Duty Cycle	VDC	-	-	-	>	1	-	-	50	3-8	20	-	-	1 k. I		-	%	See Figure 3.	
Oscillation Frequency	fmax**	-	225	-	-02	225		200	225	1-5	- 1	225	-	- 1	225	- MHz			

^{*}This measurement guarantees the dc potential at the bias point for purposes of incorporating a varactor turning diode at this point.

^{**}Frequency variation over temperature is a direct function of the $\Delta C/\Delta$ Temperature and $\Delta L/\Delta$ Temperature.

TEST VOLTAGE/CURRENT VALUES (Volts) mAdc @ Test Temperature VIHmax L VILmin VCC MC1648 -5.0 -30°C -3.20 -3.70-5.2+25°C -3.35 -3.85 -5.2 -5.0 -3.50+85°C -4.00 -5.2 -5.0 MC1648M -5.0 -55°C -3.13-3.63 -5.2 +25°C -3.35 -3.85 -5.2 -5.0 +125°C -4.10 -5.2 -5.0 -3.60

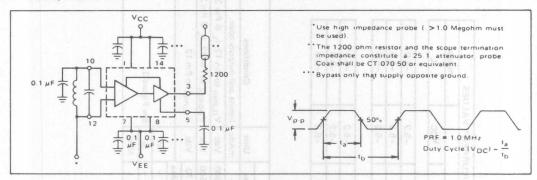
ELECTRICAL CHARACTERISTICS

			-55°	С		-30°	С		+25°		+85°C		+85°C		+85°C		+85°C		+85°C		+85°C		+125°C			
Characteristic	Symbol	Min	11	Max	Min	HE -	Max	Mir	2	Max	Mir	1	Max	Mir		Max	Unit	Conditions								
Power Supply Drain Current	1E	-			-		3- 8	-	7	41	0 %-	0.00	19-7	2 4	2 -	7-1	mAdc	Inputs and outputs open.								
Logic "1" Output Voltage	VOH	-1.08	30 -	-0.870	-1.04	15 -	-0.815	-0.90	60 -	0.750	-0.8	90	-0.640	-0.8	10 -	0.600	Vdc	VILmin to Pin 12, IL @ Pin 3.								
Logic "0" Output Voltage	VOL	-1.92	20 -	-1.670	-1.89	90 -	-1.650	-1.8	50 -	1.620	-1.8	30 -	-1.575	-1.83	20 -	1.540	Vdc	VIHmax to Pin 12, IL @ Pin 3.								
Bias Voltage	V _{Bias} *	-3.5	3	-3.23	-3.6	0	-3.30	-3.7	5	-3.45	-3.9	00	-3.60	-4.00	-4.00	-4.00	-4.00 -3.7		-4.00 -3.70		-4.00 -3.70		Vdc	VILmin to Pin 12.		
		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max										
Peak-to-Peak Tank Voltage	V _{P-P}	-	-	1 - 7	-	-	3 -0	-	400	1.6-2	2 -0	0	1 2 5	8-6	8 =	+	mV	ELT THE PARTY								
Output Duty Cycle	VDC	-	-	1-7	-	- I	-	9 -8	50	1 5-8	-	- 12	5 = .	1-2	1 +	+ 19	%	See Figure 3.								
Oscillation Frequency	fmax**	-	225			225		200	225	1 3-5	9 4	225	1 2 9	3-9	225	1	MHz	4 Alt-11.								

^{*}This measurement guarantees the dc potential at the bias point for purposes of incorporating a varactor turning diode at this point.

^{**}Frequency variation over temperature is a direct function of the $\Delta C/\Delta$ Temperature and $\Delta L/\Delta$ Temperature.





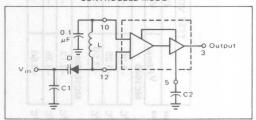
OPERATING CHARACTERISTICS

Figure 1 illustrates the circuit schematic for the MC1648. The oscillator incorporates positive feedback, by coupling the base of transistor Q6 to the collector of Q7. An automatic gain control (AGC) is incorporated to limit the current through the emitter-coupled pair of transistors (Q7 and Q6) and allow optimum frequency response of the oscillator.

In order to maintain the high Ω of the oscillator, and provide high spectral purity at the output, transistor $\Omega 4$ is used to translate the oscillator signal to the output differential pair $\Omega 2$ and $\Omega 3$. $\Omega 2$ and $\Omega 3$, in conjunction with output transistor $\Omega 1$, provides a highly buffered output which produces a square wave. Transistors $\Omega 9$ and $\Omega 11$ provide the bias drive for the oscillator and output buffer. Figure 2 indicates the high spectral purity of the oscillator output (pin 3).

When operating the oscillator in the voltage controlled mode (Figure 4), it should be noted that

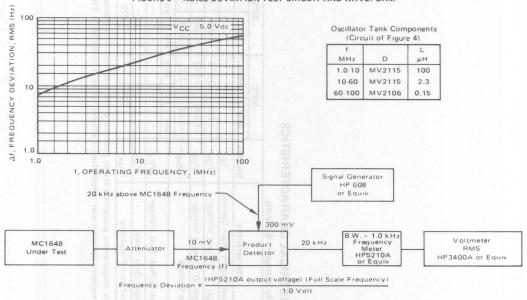
FIGURE 4 – THE MC1648 OPERATING IN THE VOLTAGE CONTROLLED MODE



the cathode of the varactor diode (D) should be biased at least 2 VBE above VEE (\approx 1.4 V for positive supply operation).

When the MC1648 is used with a constant dc voltage to the varactor diode, the output frequency will vary slightly because of internal noise. This variation is plotted versus operating frequency in Figure 5.

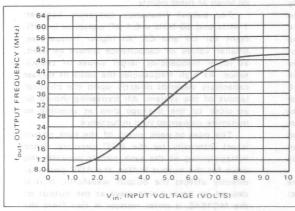
FIGURE 5 - NOISE DEVIATION TEST CIRCUIT AND WAVEFORM



4

TRANSFER CHARACTERISTICS IN THE VOLTAGE CONTROLLED MODE USING EXTERNAL VARACTOR DIODE AND COIL. $T_A = 25^{\circ}$ C

FIGURE 6



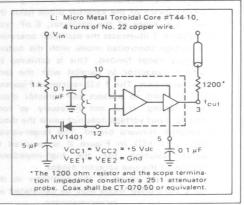
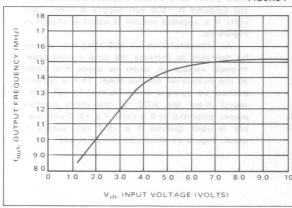


FIGURE 7



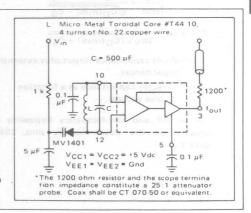
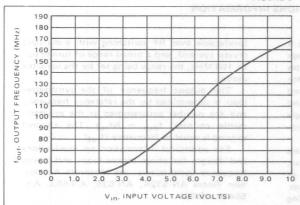
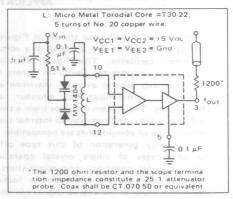


FIGURE 8





Typical transfer characteristics for the oscillator in the voltage controlled mode are shown in Figures 6, 7, and 8. Figures 6 and 8 show transfer characteristics employing only the capacitance of the varactor diode (plus the input capacitance of the oscillator, 6 pF typical). Figure 7 illustrates the oscillator operating in a voltage controlled mode with the output frequency range limited. This is achieved by adding a capacitor in parallel with the tank circuit as shown. The 1 k\O resistor in Figures 6 and 7 is used to protect the varactor diode during testing. It is not necessary as long as the dc input voltage does not cause the diode to become forward biased. The larger-valued resistor (51 k Ω) in Figure 8 is required to provide isolation for the high-impedance junctions of the two varactor diodes.

The tuning range of the oscillator in the voltage controlled mode may be calculated as:

$$\frac{f_{max}}{f_{min}} = \frac{\sqrt{c_D(max) + c_S}}{\sqrt{c_D(min) + c_S}}$$
 where $f_{min} = \frac{1}{2\pi\sqrt{L(C_D(max) + C_S)}}$

C_S = shunt capacitance (input plus external capacitance).

C_D = varactor capacitance as a function of bias voltage.

Good RF and low-frequency bypassing is necessary on the power supply pins. (See Figure 2.)

Capacitors (C1 and C2 of Figure 4) should be used to bypass the AGC point and the VCO input (varactor diode), guaranteeing only dc levels at these points.

For output frequency operation between 1 MHz and 50 MHz a 0.1 μ F capacitor is sufficient for C1 and C2. At higher frequencies, smaller values of capacitance should be used; at lower frequencies, larger values of capacitance. At high frequencies the value of bypass capacitors depends directly upon the physical layout of the system. All bypassing should be as close to the package pins as possible to minimize unwanted lead inductance.

The peak-to-peak swing of the tank circuit is set internally by the AGC circuitry. Since voltage swing of the tank circuit provides the drive for the output buffer, the AGC potential directly affects the output waveform. If it is desired to have a sine wave at the output of the MC1648, a series resistor is tied from the AGC point to the most negative power potential (ground if +5.0 volt supply is used, -5.2 volts if a negative supply is used) as shown in Figure 10.

At frequencies above 100 MHz typ, it may be desirable to increase the tank circuit peak-to-peak voltage in order to shape the signal at the output of the MC1648. This is accomplished by tying a series resistor (1 k Ω minimum) from the AGC to the most positive power potential (+5.0 volts if a +5.0 volt supply is used, ground if a -5.2 volt supply is used). Figure 11 illustrates this principle.

APPLICATIONS INFORMATION

The phase locked loop shown in Figure 9 illustrates the use of the MC1648 as a voltage controlled oscillator. The figure illustrates a frequency synthesizer useful in tuners for FM broadcast, general aviation, maritime and landmobile communications, amateur and CB receivers. The system operates from a single +5.0 Vdc supply, and requires no internal translations, since all components are compatible.

Frequency generation of this type offers the advantages of single crystal operation, simple channel selection, and elimination of special circuitry to prevent harmonic lockup. Additional features include dc digital switching (preferable over RF switching with a multiple crystal system), and a broad range of tuning (up to 150 MHz, the range being set by the varactor diode).

The output frequency of the synthesizer loop is determined by the reference frequency and the number programmed at the programmable counter; $f_{out} = Nf_{ref}$. The channel spacing is equal to frequency (f_{ref}) .

For additional information on applications and designs for phase locked-loops and digital frequency synthesizers, see Motorola Application Notes AN-532A, AN-535, AN-553, AN-564 or AN594.

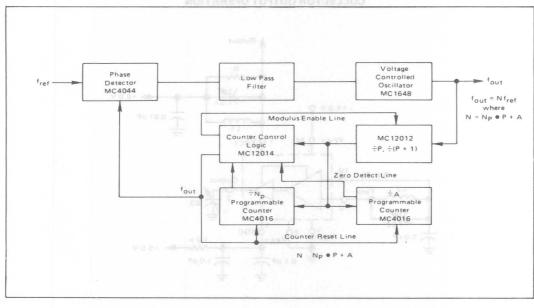


FIGURE 9 - TYPICAL FREQUENCY SYNTHESIZER APPLICATION

Figure 10 shows the MC1648 in the variable frequency mode operating from a +5.0 Vdc supply. To obtain a sine wave at the output, a resistor is added from the AGC circuit (pin 5) to VEE.

Figure 11 shows the MC1648 in the variable frequency mode operating from a +5.0 Vdc supply. To extend the useful range of the device (maintain a square wave output above 175 MHz), a resistor is added to the AGC circuit at pin 5 (1 k-ohm minimum).

FIGURE 10 - METHOD OF OBTAINING A SINE-WAVE OUTPUT

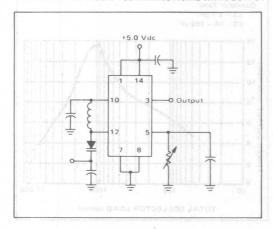


Figure 12 shows the MC1648 operating from +5.0 Vdc and +9.0 Vdc power supplies. This permits a higher voltage swing and higher output power than is possible from the MECL output (pin 3). Plots of output power versus total collector load resistance at pin 1 are given in Figures 13 and 14 for 100 MHz and 10 MHz operation. The total collector load includes R in parallel with Rp of L1 and C1 at resonance. The optimum value for R at 100 MHz is approximately 850 ohms.

FIGURE 11 — METHOD OF EXTENDING THE USEFUL RANGE OF THE MC1648 (SQUARE WAVE OUTPUT)

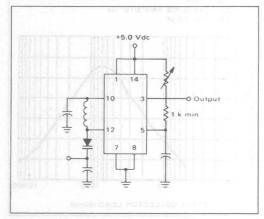


FIGURE 12 – CIRCUIT USED FOR COLLECTOR OUTPUT OPERATION

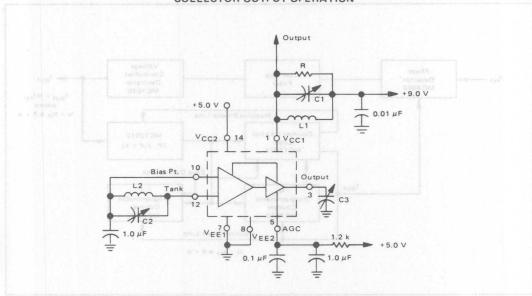
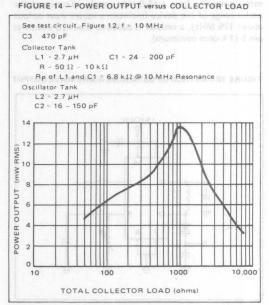


FIGURE 13 - POWER OUTPUT versus COLLECTOR LOAD



MECL III or MECL 10,000 digital levels. When \overline{C}_a is at a logic high level, Q0 will be at a logic high level provided that $V_1 > V_2$ (V_1 is more positive than V_2). $\overline{Q}0$ is the logic complement of Q0. When the clock input goes to a low logic level, the outputs are latched in their present state.

The MC1650 and the MC1651 are very

Assessment of the performance differences between the MC1650 and the MC1651 may be based upon the relative behaviors shown in Figures 4 and 7.

- t_{pd} = 3.5 ns typ (MC1650) = 3.0 ns typ (MC1651)
- Input Slew Rate = 350 V/μs (MC1650) = 500 V/μs (MC1651)
- Differential Input Voltage:
 5.0 V (-30°C to +85°C)
- Common Mode Range:

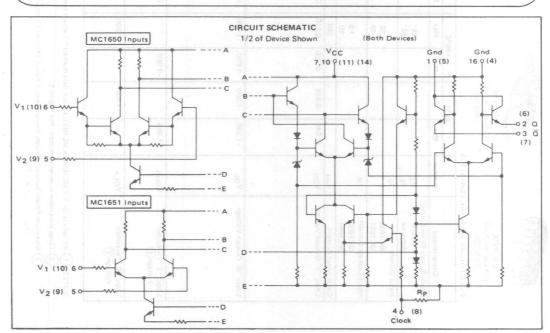
 -3.0 V to +2.5 V (-30°C to +85°C) (MC1651)
 -2.5 V to +3.0 V (-30°C to +85°C) (MC1650)
- Resolution: ≤ 20 mV (-30°C to +85°C)
- Drives 50 Ω lines

Number at end of terminal denotes pin number for L package (Case 620). Number in parenthesis denotes pin number for F package (Case 650).

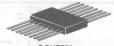
TRUTH TABLE

	111011111		
c	V ₁ , V ₂	Q0 _{n+1}	Q0 _{n+1}
Н	V ₁ >V ₂	Н	L
Н	V1 < V2	L	Н
L	φ φ	Q0 _n	ā0 _n

φ = Don't Care







F SUFFIX CERAMIC PACKAGE CASE 650

					TEST VO	LTAGE V	ALUES			1		
@ Test						(Volts)	100					
Temperature	VIHmax	VILmin	VIHAmin	VILAmax	V _{A1}	V _{A2}	V _A 3	VA4	V _{A5}	V _{A6}	VCC 3	VEE
	-0.875			-1515		-0.020				+5.0	-5.2	
+25°C	-0.810	-1.850	-1.095	-1.485	+0.020	-0.020	See Note 4)	+5.0	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	+0.020	-0.020	183537				+5.0	-5.2

ELECTRICAL CHARACTERISTICS

	3	-3	0°C	+2	5°C	+8	5°C	100	3 2 3		TEST VOLT	AGE APPL	IED TO	PINS	LISTE	DBEL	WC		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit	VIHmax	VILmin	VIHAmin	VILAmax	VA1	VA2	VA3	VA4	V _{A5}	VA6	Gnd
Power Supply Drain Current Positive Negative	ICC IE	3	Ļ.,		25° 55°		S S	mAdc	4,13	4,13	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	0,000	6,12 6,12	SHALINS	1 S 1 1	200			1,5,11, 1,5,11
Input Current MC1650 MC1651	lin				10 40	***	SIS S	μAdc	4	13	Owe p	ECT.	12	300	6	20			1,5,11
Input Leakage Current MC 1650 MC 1651	1 _R		Ĺ	STI-(71)	7.0	1 10 14	t I I	μAdc*	4	13	dustr. /	1 4 5 0 A	12	8	T TOTAL	MCOR	6		1,5,11,
Clock Input Current	linH		Land	1 6 6	350	191.	-	μAdc	4	13	0 5 %	F . P .	6,12	1 13 - 6	1 10 1	100			1,5,11,
Logic "1" Output Voltage	Voн	-1.045	-0.875	0.960	-0.810	-0.890	-0.700	Vdc	4,13	19 (a)1	Call de la Calledon d	ALE CT ALE	5,11	5,11 6,12	6,12 5,11	5,11 6,12	5.11	6.12	1,5,11, 1,6,12, 1,16 1,16 1,5,11, 1,6,12, 1,16
Logic "0" Output Voltage	VOL	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	4,13	(nso.)	W (13) (11) (114)	D (C) M	5,11 6,12	6,12 5,11	5,11	6,12 5,11	6,12 5,11		1,5,11, 1,6,12, 1,16 1,16 1,5,11, 1,6,12, 1,16
Logic "1" Threshold Voltage 2	VOHA	-1.065		-0.980		-0.910	Calvindad by	Vdc	200 A 200 A 8 - 090 A	13	4	4	6	6					1,5,10
Logic "0" Threshold Voltage 2	VOLA		-1.630		-1.600	A A A A A A A A A A A A A A A A A A A	-1.555	Vdc	And and and the	13	4	4	6	6					1,5,16

NOTES: 1) All data is for 1.2 MC1650 or MC1651, except data marked (*) which refers to the entire package.

2 These tests done in order indicated. See Figure 5.

3 Maximum Power Supply Voltages (beyond which device life may be impaired):
|VEE| + |VCC| ≥ 12 Vdc.

All Temperatures	V _A 3	VA4	V _{A5}	V _{A6}
MC1650	+3.000	+2.980	-2.500	-2.480
MC1651	+2.500	+2.480	-3.000	-2.980

	SWITCHING TEST VOLTAGE VALUES													
@ Test		(Volts)												
Temperature	V _{R1}	VR2 VR3	VX	VXX	v _{cc} 1	VEE 1								
-30°C	+2.000		+1.040	+2.00	+7.00	-3.20								
+25°C	+2.000	See Note 4	+1.110	+2.00	+7.00	-3.20								
+85°C	+2.000	MOTIVE -	+1.190	+2.00	+7.00	-3.20								

		-30	o°C	+25	5°C	+8	5°C		Conditions		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit	(See Figures 1-3)		
Switching Times Propagation Delay (50% to 50%) V-Input	t _{pd}	2.0	5.0	2.0	5.0	2.0	5.7	ns	V _{R1} to V ₂ , V _X to Clock, P ₁ to V ₁ , or, V _{R2} to V ₂ , V _X to Clock, P ₂ to V ₁ , or, V _{R3} to V ₂ , V _X to Clock, P ₃ to V ₁ .		
Clock 2		2.0	4.7	2.0	4.7	2.0	5.2		V_{R1} to V_2 , P_1 to V_1 and P_4 to Clock or, V_{R1} to V_1 , P_1 to V_2 and P_4 to Clock		
Clock Enable 3	tsetup			2.5				ns	Value Va Parto Va Parto Cloub		
Clock Aperture (3)	tap			1.5				ns	VR1 to V2, P1 to V1, P4 to Clock		
Rise Time (10% to 90%)	\ t+	1.0	3.5	1.0	3.5	1.0	3.8	ns	V V . V CI- 1 . D V		
Fall Time (10% to 90%)	t-	1.0	3.0	1.0	3.0	1.0	3.3	ns	VR1 to V2, VX to Clock, P1 to V1.		

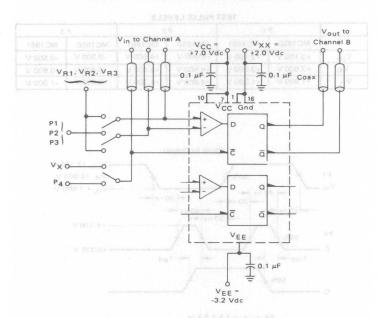
NOTES: 1 Maximum Power Supply Voltages (beyond which device life may be impaired $|V_{CC}| + |V_{EE}| \ge 12 \text{ Vdc}$.

(4) All Temperatures V_{R2} V_{R3}
MC1650 +4.900 -0.400
MC1651 +4.400 -0.900

2) Unused clock inputs may be tied to ground

3 See Figure 3

FIGURE 1 - SWITCHING TIME TEST CIRCUIT @ 25°C



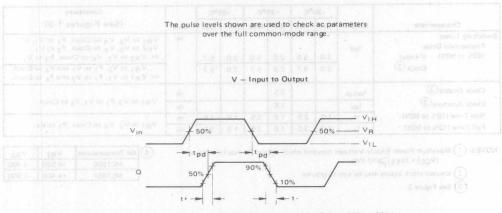
Note: All power supply and logic levels are shown shifted 2 volts positive.

50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable.

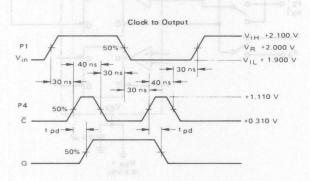
4





Test pulses: t₊, t₋ = 1.5 ±0.2 ns (10% to 90%) f = 5.0 MHz 50% Duty Cycle

TEST PULSE LEVELS MC1650 MC1651 MC1650 MC1651 MC1650 MC1651 +2.100 V +2.100 V +5.000 V +4.500 V -0.300 V -0.800 V VIH VR +2.000 V +2.000 V +4.900 V +4.400 V -0.400 V -0.900 V VIL +1.900 V +1.900 V +4.800 V +4.300 V -0.500 V -1.000 V



P4: t_+ , $t_- = 1.5 \pm 0.2$ ns.

FIGURE 3 - CLOCK ENABLE AND APERTURE TIME TEST CIRCUIT AND WAVEFORMS @ 25°C

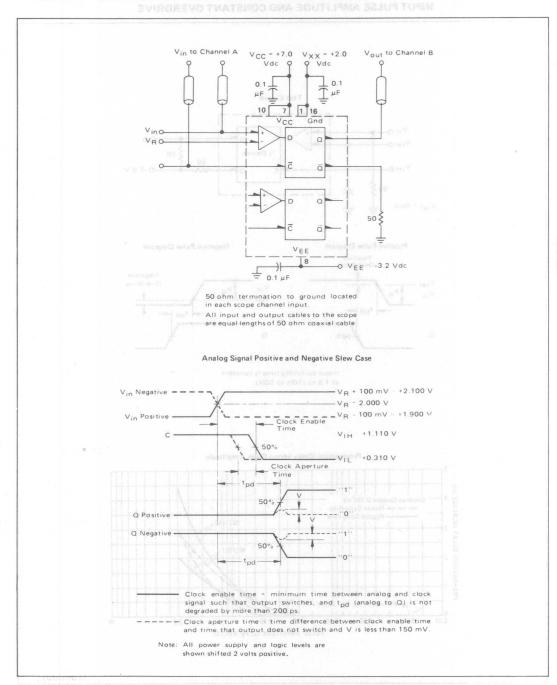
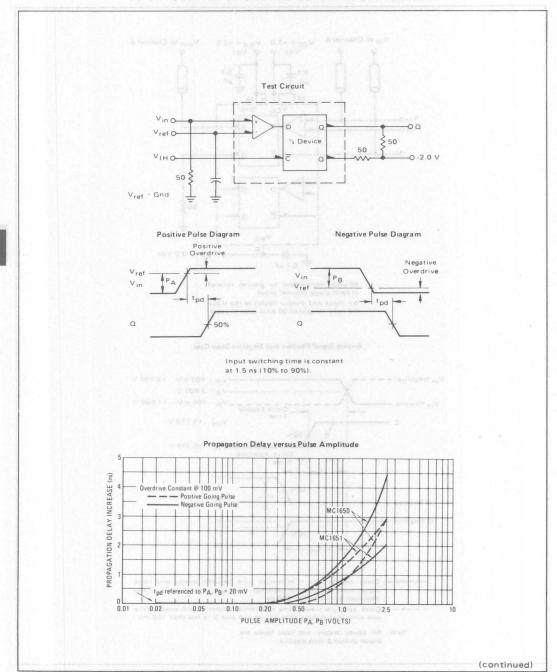


FIGURE 4 – PROPAGATION DELAY (tpd) versus



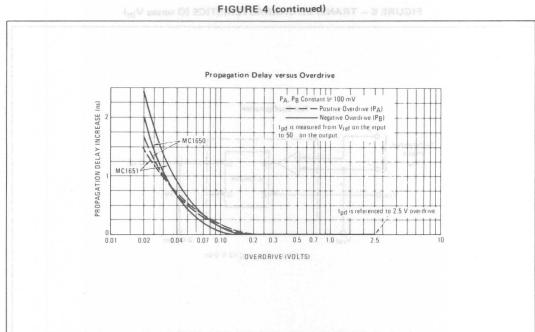


FIGURE 5 - LOGIC THRESHOLD TESTS (WAVEFORM SEQUENCE DIAGRAM)

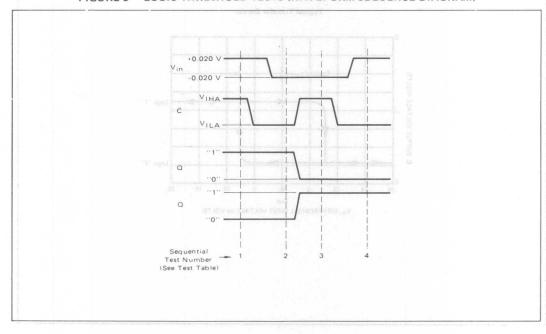
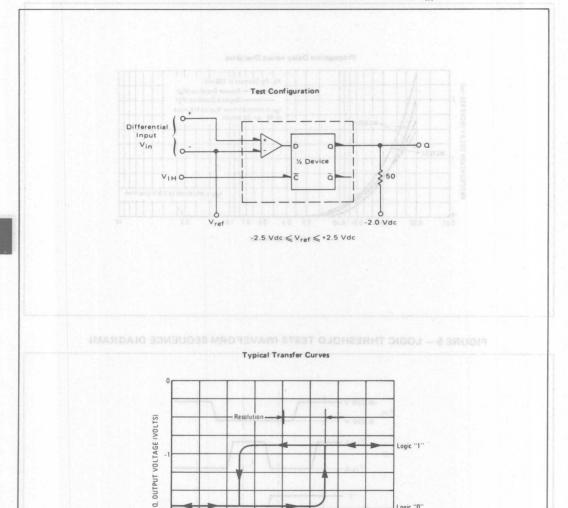


FIGURE 6 - TRANSFER CHARACTERISTICS (Q versus Vin)

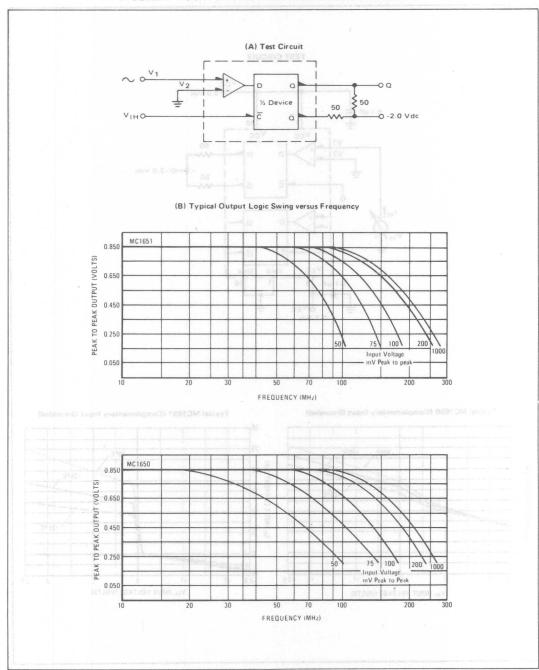




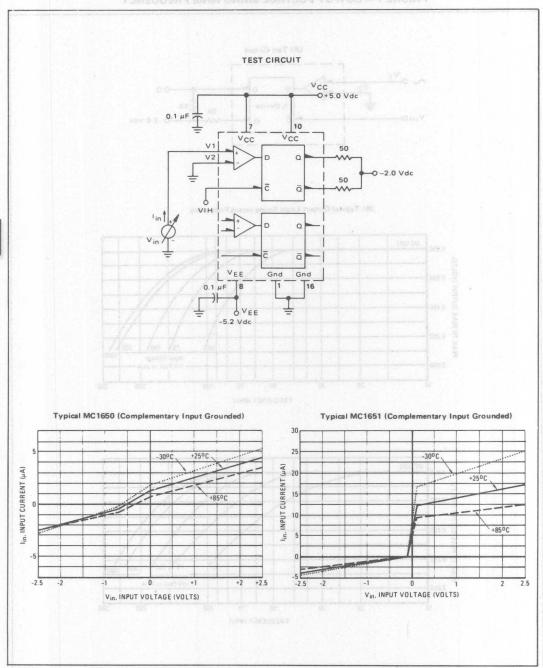
V_{ref}
V_{In}, DIFFERENTIAL INPUT VOLTAGE (m VOLTS)

Logic "0"

FIGURE 7 - OUTPUT VOLTAGE SWING versus FREQUENCY







MC1654

BINARY COUNTER

TRUTH TABLE

Am		-	INPU	TS		2 1		OUT	PUTS	
R	SO	S1	S2	S3	C1	C2	QO	01	Q2	Q3
1	0	0	0	0	Φ	Φ	0	0	0	0
0	1	1	1	1	φ	φ	1	1	1	1
0	0	0	0	0	00	Φ		No C	ount	
0	0	0	0	0	φ	1		No C	ount	
0	0	0	0	0			0	0	0	0
0	0	0	0	0			1	0	0	0
0	0	0	0	0			0	1	0	0
0	0	0	0	0	8.5		11	1 8	0	0
0	0	0	0	0			0	0	1	0
0	0	0	0	0	100		1	0	1	0
0	0	. 0	0	0			0	11	1	0
0	0	0	0	0			1	1	1	0
0	0	0	0	0			0	0	0	1
0	0	0	0	0			1	0	0	1
0	0	0	0	0			0	1	0	1
0	0	0	0	0			1	1	0	1
0	0	0	0	0			0	0	1	1
0	0	0	0	0			1	0	1	1
0	0	0	0	0	810	9 (93	0	1	1	01 V
0	0	0	0	0			1	1	1	1

 ϕ = Don't Care

VIH

Clock transition from VIL to VIH

may be applied to C1 or C2 or both

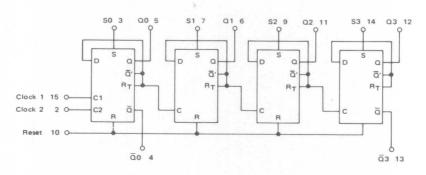
for same effect.

The MC1654 is a four-bit counter capable of divide-by-two, divide-by-four, divide-by-eight, or divide-by-16 functions. When used independently, the divide-by-16 section will toggle at 325 MHz typically. Clock inputs trigger on the positive-going edge of the Clock pulse.

Set and Reset inputs override the Clock, allowing asynchronous "set" or "clear." Individual Set and common Reset inputs are provided, as well as complementary outputs for the first and fourth bits. True outputs are available at all bits.

Power Dissipation = 750 mW typ f_{Tog} = 325 MHz typ





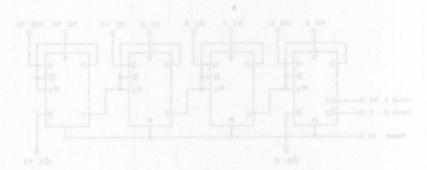
V_{CC} = 1, 16 V_{EE} = 8

	oT .	-30	o°C	+2	5°C	+8	5°C		
Characteristic Yd Mily Owl-yd	Symbol	Min	Max	Min	Max	Min	Max	Unit	
Power Supply Drain Current	IE	-	etu n ru	0 -	200	24-19	() —	mAdc	
Input Current sugal shoots will sugar x HM	linH	180	50 110	100 0	0 10	ES 23	18 10	mAdo	
Reset Set, Clock	ed am			7	0.60	7 T		0	
Switching Times Propagation Delay	tpd	0 0	0 0	10	111	0 0	0.0	ns	
Clock (Pin 2 or 15 to pins 4, 5) Set, Reset	tirer et	1.0	2.9	1.0	2.7	1.0	3.1 4.1	0	
Rise Time (10% to 90%)	t+	1.0	2.9	1.0	2.7	1.0	3.1	ns	
Fall Time (10% to 90%)	t-	1.0	2.8	1.0	2.6	1.0	3.0	ns	
Maximum Toggle Frequency	ftog	260	9-1	300	-	260	0 1	MHz	

For V_{OH}/V_{OL} testing reset all four flip-flops by applying R_{A1} to Reset and apply V_{ILmin} to Set inputs, or set all four flip-flops by applying R_{A1} simultaneously to all Set inputs and apply V_{ILmin} to Reset. For V_{OHA}/V_{OLA} testing follow the same procedure using P_{A2} and V_{ILAmax}.

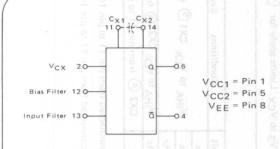
PA1 VIH PA2 VIHA

4



MC1658

VOLTAGE-CONTROLLED MULTIVIBRATOR



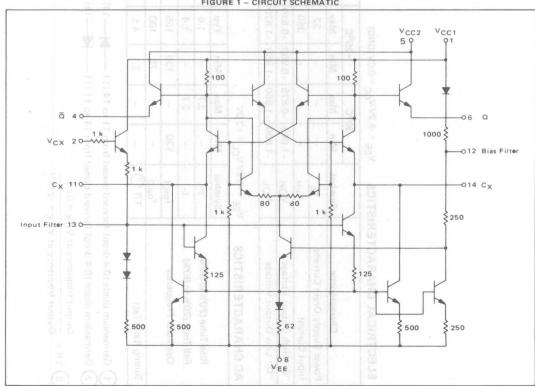
The MC1658 is a voltage-controlled multivibrator which provides appropriate level shifting to produce an output compatible with MECL III and MECL 10,000 logic levels. Frequency control is accomplished through the use of voltage-variable current sources which control the slew rate of a single external capacitor.

The bias filter may be used to help eliminate ripple on the output voltage levels at high frequencies and the input filter may be used to decouple noise from the analog input signal.









@ Test Temperature -30°C +25°C +85°C

T	EST VO	LTAGI	VALU
8.3		Vdc ±1	%
VIH	VIL	V3	VIHA
0.0	-2.0	-1.0	+2.0
0.0	-2.0	-1.0	+2.0
0.0	-2.0	-1.0	+2.0

ELECTRICAL CHARACTERISTICS

 $V_{EE} = -5.2 V_{CC} = 0.0 V (GND)$

		-30	o°C	+250		+85	5°C		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit	Conditions
Power Supply Drain Current	1E	-	-		32	+		mAdc	VIH to VCX Limit applies for 1 or
Input Current	linH	1			350	3 +	-	μAdc	VIH to VCX 1
"Q" High Output Voltage	Voн	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	V V
''Q'' Low Output Voltage	VOL	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	V ₃ to V _{CX} . Limits apply for (1) or (2)

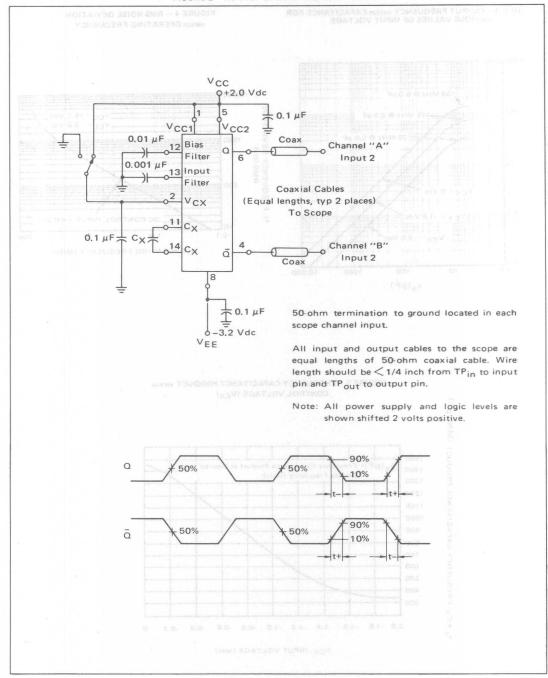
AC CHARACTERISTICS	$V_{EE} = -3.2V$	$V_{EE} = -3.2 \text{V} V_{CC} = +2.0 \text{V}$											
	Symbol	Min	Max	Min	Тур	Max	Min	Max	Unit	Conditions See Figure 2.			
Rise Time (20% to 80%)	t+	-	2.7	W-1	1.6	2.7	8	3.0	ns				
Fall Time (20% to 80%)	t-		2.7		1.4	2.7	844	3.0	ns	VIHA to VCX, CX1 5 from pin 11 to			
Oscillator Frequency	fosc1	130	-1	130	155	175	110	-	MHz				
	fosc2		- F	78	100	120	<u> </u>		MHz	VIHA to VCX, CX2 4 from pin 11 to			
Tuning Ratio Test	TR 3		-	3.1	4.5		-	-	_ 1	CX2 4 from pin 11 to pin 14.			

- (1) Germanium diode (0.4 drop) forward biased from 11 to 14 (11
- Germanium diode (0.4 drop) forward biased from 14 to 11 (11
- Output frequency at VCX = Gnd Output frequency at $V_{CX} = -2.0 \text{ V}$

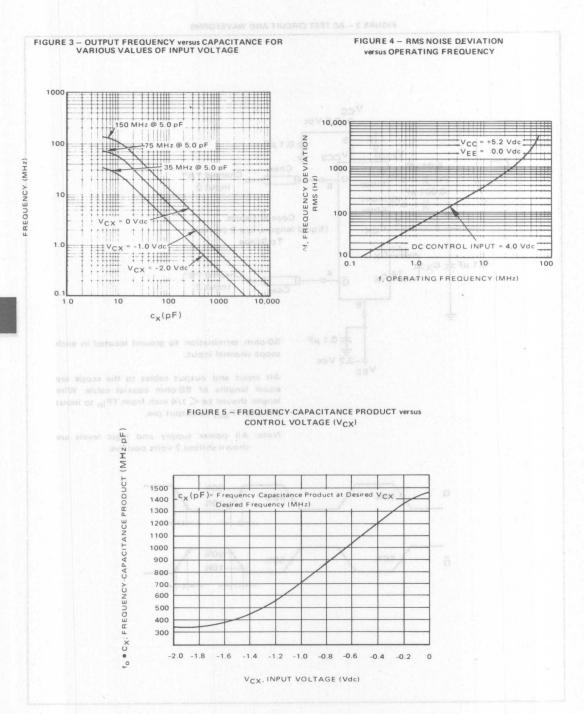
- 4 $C_{X1} = 5 \text{ pF}$ connected from pin 11 to pin 14. 5 $C_{X2} = 10 \text{ pF}$ connected from pin 11 to pin 14.

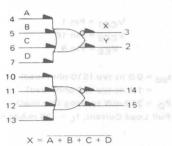
4-24

FIGURE 2 - AC TEST CIRCUIT AND WAVEFORMS









Y = A + B + C + D

VCC2 = Pin 16 VEE = Pin 8

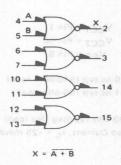
 $t_{pd} = 0.9 \text{ ns typ } (510\text{-ohm load})$ = 1.1 ns typ (50-ohm load)

PD = 120 mW typ/pkg (No load) Full Load Current, IL = -25 mAdc max



Numbers at ends of terminals denote pin numbers for Li package is drowning enough alarment to and to the

			+235°C							
						i lode	Syn			
ohve, m		-	88	-30	0°C	+2	5°C	sen Cumer	35°C	3.5%
	Character	istic	Symbo	Min	Max	Min	Max	Min	Max	Unit
Power	ower Supply Drain Current		t IE	-	+		28		rami Lun	mAdd
Input	nput Current		linH	_ a	1 40	-	350	velet	1 (15) (<u>80)</u> (1	μAdo
	ning Times opagation D	Delay		0.6	1.8	0.6	1.7 1.5	0.6	1.9 1.7	ns
Ris	Rise Time, Fall Time (10% to 90%)		t ⁺ ,t ⁻	0.6	2.2	0.6	2.1	0.6	2.3	ns



V_{CC1} = Pin 1 V_{CC2} = Pin 16 V_{EE} = Pin 8

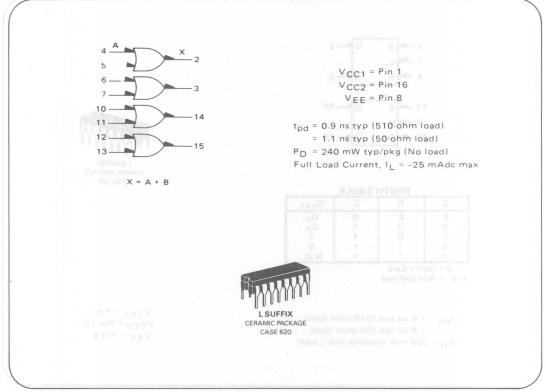
t_{pd} = 0.9 ns typ (510-ohm load) = 1.1 ns typ (50-ohm load)

 P_D = 240 mW typ/pkg (No load) Full Load Current, I_L = -25 mAdc max



Number at end of terminals denotes pin number of L package.

		-3	0°C	+2!	5°C	+8	5°C	
Characteristic	Symbol	Min	Max	Max	Max	Min	Max	Unit
Power Supply Drain Current	o°JE −		300E-		56		-	mAdc
Input Current	M linHul	- ×s	M + mil	n Joden	350	Sitar	92091 0 fJ	μAdc
Switching Times						am Curre	G vinces	ns
Propagation Delay	t-+	0.6	1.6	0.6	1.5	0.6	1.7	i monal
	t+-	0.6	1.8	0.6	1.7	0.6	1.9	2000
Rise Time, Fall Time (10% to 90%)	t ⁺ ,t ⁻	0.6	2.2	0.6	2.1	0.6	2.3	ns



Number at end of terminals denotes pin number of L package. It address any approach to the control of the contr

	II PERMIT	-3	o°C	+2	5°C	+8	5°C	
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Drain Current	-IE			-	56	J usto Ri	198 -	mAdd
Input Current	linH	1		1-1	350		e10 =	μAdd
Switching Times			1 200			patre	protective	ns
Propagation Delay	t ⁺⁺	0.6	1.6	0.6	1.5	0.6	2891:7	
	0.t E.	0.6	1.8	0.6	1.7	0.6	1.9	
Rise Time, Fall Time (10% to 90%)	t ⁺ ,t ⁻ 8	0.6	2.2	0.6	2.1	0.6	2.3	ns

4

	5 - S	0	- 2			
	7 - C			2		
	4 - R	0	2			
	8100	4	3			
	9.419	E.V				
	12 - S	0	-15		702-01	
	9 - C	awa an				
	13 - R					
	Folds galaxes					
	CARLO BARRIOR					
					I SHEELY	
					L SUFFIX CERAMIC PACKAGE	
	TRUTH	TABLE	Foll Load		CERAMIC PACKAGE	
S	TRUTH 1	TABLE C	Q _{n+1}		CERAMIC PACKAGE	
S	TRUTH 1	TABLE C 0	Q_{n+1}		CERAMIC PACKAGE	
S	TRUTH 1	TABLE C	Q _{n+1} Q _n Q _n		CERAMIC PACKAGE	
S	TRUTH 1	TABLE C 0 1	Q_{n+1}		CERAMIC PACKAGE	
S φ 0 1	TRUTH 1	TABLE C 0 1 1	Q _{n+1} Q _n Q _n 1		CERAMIC PACKAGE	
S φ 0 1 0 1 φ = De	TRUTH 1 R P O O 1 1 1 con't Care	TABLE C 0 1 1 1	Q _{n+1} Q _n Q _n 1		CERAMIC PACKAGE	
S φ 0 1 0 1 φ = De	R	TABLE C 0 1 1 1	Q _{n+1} Q _n Q _n 1		CERAMIC PACKAGE	
S φ 0 1 0 1 φ = De	TRUTH 1 R P O O 1 1 1 con't Care	TABLE C 0 1 1 1	Q _{n+1} Q _n Q _n 1		CERAMIC PACKAGE	
S φ 0 1 0 1 φ = De	TRUTH 1 R P O O 1 1 1 con't Care	TABLE C 0 1 1 1	Q _{n+1} Q _n Q _n 1 0 N.D.		CERAMIC PACKAGE CASE 620	
$\begin{cases} S \\ \phi \\ 0 \\ 1 \\ 0 \\ 1 \end{cases}$ $\phi = Dc$ $N.D. = Nc$	TRUTH 1 R 0 0 1 1 1 con't Care ot Defined	TABLE C 0 1 1 1 1 1	Q _{n+1} Q _n Q _n 1 0 N.D.		CERAMIC PACKAGE CASE 620 VCC1 = Pin 1	
S ϕ 0 1 0 1 0 N.D. = No	TRUTH 1 R \$\phi\$ 0 0 1 1 1 con't Care of Defined	TABLE C 0 1 1 1 1 1 510-ohm	Q _{n+1} Q _n Q _n 1 0 N.D.		CERAMIC PACKAGE CASE 620	

Number at end of terminal denotes pin number for L package to redmost the attended to the real statement to the real statement of th

				-3	0°C	+2	5°C	+8!	5°C	197-1
Characteri	stic		Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Drain C	urrent		ΙE	00-		-	55	-	_	mAdc
Input Current	RETVI	STORE .	linH	FREE	12	Sylvin		311	SHELBLIS	μAdc
Set, Reset				-	-	3-	370	m=0 r	rst-El v	асть за
Clock				-	-	dout	225	-	- 11	smuD in
Switching Times									29/71	ns
Propagation Delay			tpd	1 8.0		++3		V6	eC no	TBDBCOT*
Clock 8.0			8.7	1.0	2.7	1.0	2.5	1.1	2.8	
Set, Reset			2.2	1.0	2.5	1.1	2.3	1.1	2.7	ni Tani I
Rise Time (10% to	90%)		t+	8.0	2.8	0.8	2.5	0.9	2.9	ns
Fall Time (10% to	90%)		t-	0.5	2.4	0.5	2.2	0.5	2.6	ns

- 1.8 ns typ (50-ohm load) PD = 220 mW typ/pkg (No load)

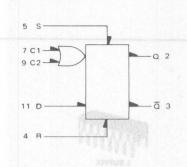
Number at end of terminal denotes pin number for L package

φ = Don't Care

φ

* *Output state not defined

					-30	0°C	+2	5°C	+8	5°C	2000
Character	istic			Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Drain C	urrent			ΙE	_	-	-	55	-	-	mAdc
Input Current				linH					29	mT ga	μAdc
Data, Set, Reset			7,5		507	-	-	370	str40 n	orregen	919
Clock			V		-	-	-	225	r.8 1 07)	antii .	8174
Switching Times	8.1	8.0	1.3	0.5	-1			(2000 -	r 8907	amiT.	ns
Propagation Delay				tpd	10.00						
Clock					1.0	2.7	1.0	2.5	1.1	2.8	195
Set, Reset				+	1.0	2.5	1.0	2.3	1.1	2.7	C 100
Rise Time (10% to	90%)			t+	0.8	2.8	0.9	2.5	0.9	2.9	ns
Fall Time (10% to	90%)			t-	0.5	2.4	0.5	2.2	0.5	2.6	ns



TRUTH TABLE

R	S	D	С	Q _{n+1}
L	Н	φ	φ	Н
н	L	φ	0	L
н	н	Φ	Φ	N.D.
L	L	L	L	an
L	L	L	5	L
L	L	L	н	Qn
L	L	н	L	Qn
L	L	н	5	н
L	L	н	H	an

φ = Don't Care
ND = Not Defined
C = C1 + C2

Master slave construction renders the MC1670 relatively insensitive to the shape of the clock waveform, since only the voltage levels at the clock inputs control the transfer of information from data input (D) to output.

When both clock inputs (C1 and C2) are in the low state, the data input affects only the "Master" portion of the flip flop. The data present in the "Master" is transferred to the "Slave" when clock inputs (C1 "OR" C2) are taken from a low to a high level. In other words, the output state of the flip flop changes on the positive transition of the clock pulse.

While either C1 "OR" C2 is in the high state, the "Master" (and data input) is disabled.

Asynchronous Set (S) and Reset (R) override Clock (C) and Data (D) inputs.

Power Dissipation = 220 mW typical (No Load) $f_{Tog} = 350 \text{ MHz typ}$



Number at end of terminal denotes pin number for L package

VCC1 = Pin 1

V_{CC2} = Pin 16 V_{EE} = Pin 8

		-3	0°C	+2!	5°C	+8!	5°C	-
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Drain Current	1E	-	-	-	48	-	-	mAde
Input Current Set, Reset	InH	_	1	-	550	_	-	μAdd
Clock State William Walk Com	Man Nex	fortery	3 -	-	250	97. 50 181	ID -	
BAData		司	-	-	270	OUTICE	videu8	Power
Switching Times Propagation Delay Rise Time (10% to 90%)	^t pd t+	1.0	2.7	1.1	2.5	1.1	2.9	ns
Fall Time (10% to 90%)			2.1	0.6				ns
Setup Time	t- ts"1"	0.5	-	0.4	1.9	0.6	2.3	ns
Hold Time	ts"0"	41		0.5 0.3 0.5	16015 d	11096	<u> 1980</u>	ns
Toggle Frequency	fTog	270	1-	300	120 <u>0</u> 10 (270	stoil)	MHz

FIGURE 1 - TOGGLE FREQUENCY WAVEFORMS

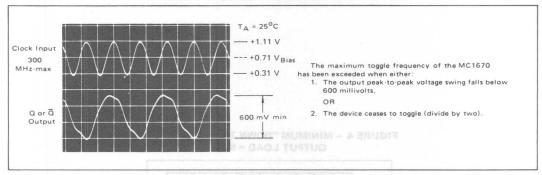


FIGURE 2 - MAXIMUM TOGGLE FREQUENCY (TYPICAL)

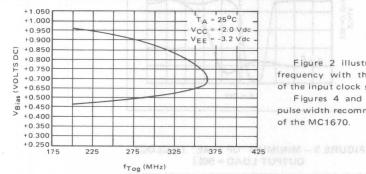
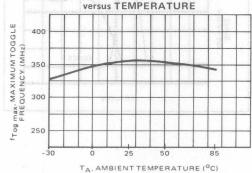


Figure 2 illustrates the variation in toggle frequency with the dc offset voltage (V_{Bias}) of the input clock signal.

Figures 4 and 5 illustrate minimum clock pulse width recommended for reliable operation of the MC1670.

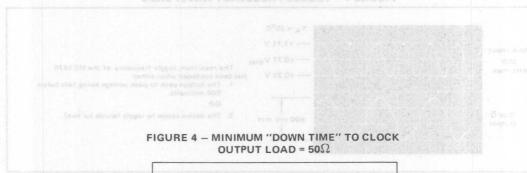
FIGURE 3 - TYPICAL MAXIMUM TOGGLE FREQUENCY



Temperature	-30°C	+25°C	+85°C
VBias	+0.660 Vdc	+0.710 Vdc	+0.765 Vdc

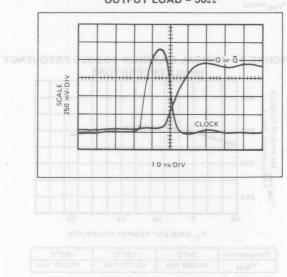
Note: All power supply and logic levels are shown shifted 2 volts positive.





SCALE SOON OF THE PROPERTY OF

FIGURE 5 – MINIMUM "UP TIME" TO CLOCK OUTPUT LOAD = 50Ω





3 X 2 13 A 14 6 B 15 7 B 15

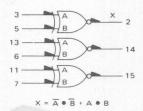
V_{CC1} = Pin 1 V_{CC2} = Pin 16 V_{EE} = Pin 8

t_{pd} = 1.1 ns typ (510-ohm load) = 1.3 ns typ (50-ohm load) P_D = 220 mW typ/pkg Full Load Current, I_L = -25 mAdc max L SUFFIX
CERAMIC PACKAGE
CASE 620

1.1 ns typ (510 ohm load) 1.3 ns typ (50 ohm load) 220 mW typ/pkg

Number at end of terminal denotes pin number for L package.

		25°C		-30	o°C	+2	5°C	+8!	5°C	
	Characte	ristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power	Supply Drain	Current	I _E	31	-	-	55	nisi()	ytanu.	mAdd
Input (Current		THE T						ingitus	μAdo
		A Inputs	linH	Mail	- 27	ugal A	350	-	-	
		B Inputs	linH	انطا	- 87	ndat 1	270	_	_	
Switch	ing Times							50	604.T 80	ns
Pro	pagation Dela		t++,t-+	4-1-4	2.0	иалт А	1.8	sig() r	2.3	
		A Inputs {	t+-,t	1	2.1	-	1.9	_	2.4	
		B Inputs {	t++,t-+	+-1+	2.5	uorti 8	2.3		2.8	
		S B Inputs {	t+-,t		2.5	-	2.3	-	2.8	
Ris	e Time (10% t	0 90%)	t+	封	2.7	_	2.5	1.02011	2.9	ns
Fall	Time (10% to	90%)	t-	=1	2.4	_	2.2	1035.1	2.6	ns



V_{CC1} = Pin 1 V_{CC2} = Pin 16 V_{EE} = Pin 8

 t_{pd} = 1.1 ns typ (510-ohm load) = 1.3 ns typ (50-ohm load) P_D = 220 mW typ/pkg Full Load Current, I_L = -25 mAdc max



Number at end of terminal denotes pin number for L package. The should not assess to minute to one or reducing

+25°C +85°C		-3	0°C	+2	5°C	+8	5°C	
Characteristic Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Drain Current	IE	101	E	-	55	niand	vigou:	mAdd
Input Current							11.8571	μAdd
A Inputs	linH	Hmil	- 27 U	onT.A	350	-	-	
B Inputs	linH	147.1	-ari	ant a	270	-	-	
Switching Times					Contract land	circ	wit on	ns
Propagation Delay A Inputs	t++,t-+	1-5,14	2.0	-	1.8	relation	2.3	
Thousand Thousand	t+-,t	T	2.1	HOLL A	1.9	-	2.4	
B Inputs {	t++,t-+		2.5	-	2.3	-	2.8	
B Inputs	t+-,t		2.5	ugal 8	2.3	-	2.8	
Rise Time (10% to 90%)	t+	Ŧ	2.7	-	2.5	1 2001	2.9	ns
Fall Time (10% to 90%)	t-	-	2.4	-	2.2	+ 2717	2.6	ns

The MC1678 is a four-bit counter capable of

divide-by-two, divide-by-five, or divide-by-10

functions. When used independently, the divideby two section will toggle at 350 MHz typically,

while the divide-by-five section will toggle at

325 MHz typically. Clock inputs trigger on the

allowing asynchronous "set" or "clear".

Individual Set and common Reset inputs are

Set and Reset inputs override the clock,

positive going edge of the clock pulse.

DC Output Loading Factor = 70 Power Dissipation = 750 mW typ

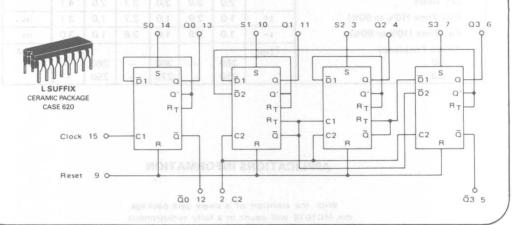
DC Input Loading Factor

provided, as well as complementary outputs

for the first and fourth bits. True outputs

Tog 350 MHz typ

are available at all bits.



BCD

(Clock connected to C1 and Q0 connected to C2)

and	40 00	illec ter	0 10 02	1
COUNT	00	Q1	Q2	Q3
0 1 2 3	LHLH	L H H	L	
4 5 6 7	L H L H	L H H	HHHH	LLLL
8 9	a L H	E	Ł	н

BI-QUINARY

(Clock connected to C2

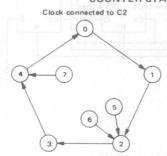
COUNT	Q1	Q2	Q3	00
0 1 2 3	LHLH	LLHH		L
4 5 6 7	LLHL	LLLH	HLLL	HHH
8	H	H	L	Н

	R	S	į

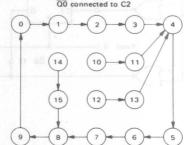
С	R	S	Q _{n+1}
0	L	L	Q _n
o o	н	L	L
0	L.	н	н
0	н	Н	ND

o = Don't Care ND = Not Defined

COUNTER STATE DIAGRAM - POSITIVE LOGIC



Q0 connected to C2

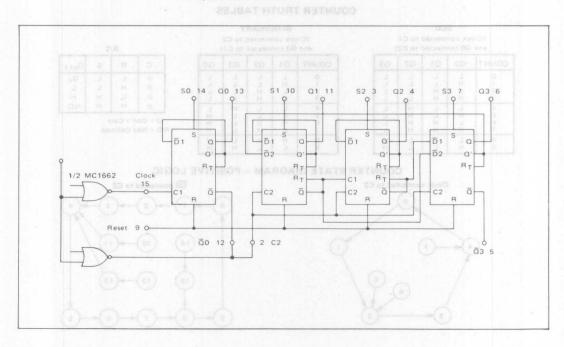


		-30°C		+25°C		+85°C			
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit	
Power Supply Drain Current	1E	-	-	-	200	-	-	mAdc	
Input Current Reset	linH	. 0	1 -yra-al		1.00	yd ab	wite o	mAdc	
C2 a sotos 7 embsou rupal 00	VS 816	_	ibiyib s rits y ngy	at 25 M	0.70		nett us on wellt		
Set, Clock		3	s s ig go	1 1. w 1	0.45	0771-9	d-o b ivi	b ent e	
Switching Times Propagation Delay	t _{pd}		di no n	eggini estu	o nonta	edr. Yo	picsity g edge	ns	
Clock to Q0, Q0		1.0	2.9	1.0	2.7	1.0	3.1		
C2 to Q1, Q2, Q3, Q3 Set, Reset		1.0	3.2	1.0	3.0	2.0	3.4		
Rise Time (10% to 90%)	t+	1.0	2.9	1.0	2.7	1.0	3.1	ns	
Fall Time (10% to 90%)	t- 9	1.0	2.8	1.0	2.6	1.0	3.0	ns	
Toggle Frequency	fTog	260		300		260	4	MHz	
Q3		250		275	rate	250	7 11		

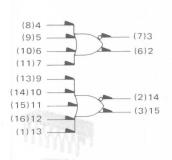
4

APPLICATIONS INFORMATION

With the addition of a single gate package, the MC1678 will count in a fully synchronous mode, as shown below.



DUAL 4-5-INPUT OR/NOR GATE



V_{CC1} = Pin 1(5) V_{CC2} = Pin 16(4) V_{EE} = Pin 8(12)

tpd = 0.8 ns typ
PD = 125 mW typ/pkg (No Load)
Output Rise and Fall Times
(20% to 80%) 1.1 ns

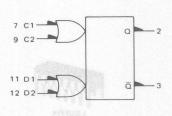




Number at end of terminal denotes pin number for L package

Number in parenthesis denotes pin number for F package

		-30°C		+25°C		+85°C		Trans.	
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit	
Power Supply Drain Current	1 _E	1-0	-	-	28	7000	-	mAdc	
Input Current	linH	-	-	-	350	Tann	0.57.21	μAdc	
Switching Times Propagation Delay	t _{pd}	0.5	1.5	0.5	1.3	0.5	1.5	ns	
Rise Time, Fall Time (20% to 80%)	t+, t-	0.5	1.6	0.5	1.4	0.5	1.6	ns	





TRUTH TABLE

С	D	Q _{n+1}
L	φ	an
н	Φ	Qn
	L	L
	Н	Н

C = C1 + C2 φ = Don't Care
D = D1 + D2

V_{CC1} = Pin 1 V_{CC2} = Pin 16 V_{EE} = Pin 8

 $P_D = 200 \text{ mW typ/pkg (No Load)}$ $f_{Tog} = 500 \text{ MHz min}$

Number at end of terminal denotes pin number for L package

		-30°C		+25°C			+8!	-	
Characteristic	Symbol	Min	Max	Min	10200	Max	Min	Max	Unit
Power Supply Drain Current	1 _E	80 <u>8.</u> 10	og <u>9</u> 10	16d <u>im</u>	Ve sie	59	o arzants	neuso i	mAdd
Input Current Pins 7,9	linH	1-	-	_		250	-	-	μAdo
Pins 11,12	a Care	-	-	_		270	-	-	
Switching Times		lodi		Min	Тур	Max			ns
Propagation Delay	tpd	ADIEN	TYS .		1.5		TENIO.		
Rise Time, Fall Time (10% to 90%)	t+,t-	1		-	1.3		100	na C fat	ns
Setup Time	t _{setup}	-	-	-	0.3		SOLUTE	9816374	ns
Hold Time	thold	1		-	0.3		-		
Toggle Frequency	fTog	500	-	500	540	1.0	500	R1 -	MHz

FIGURE 1 - TOGGLE FREQUENCY TEST CIRCUIT

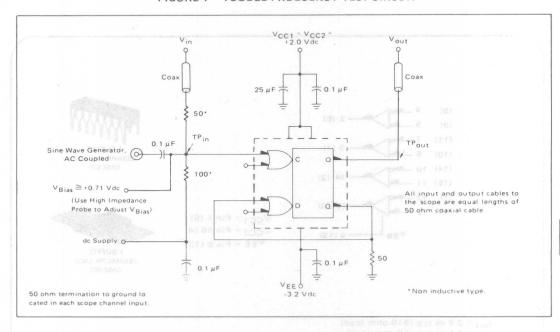
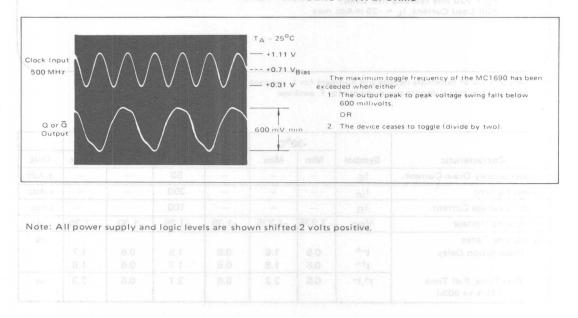
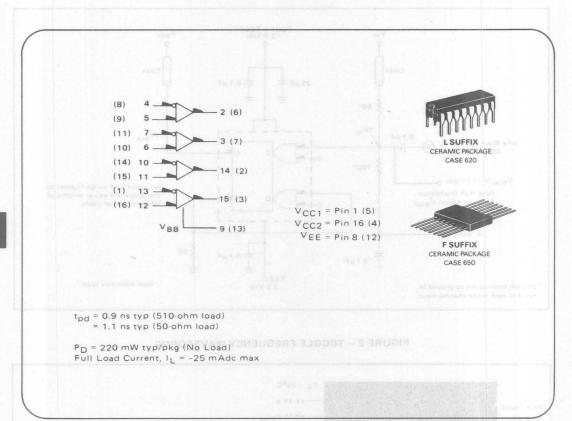


FIGURE 2 - TOGGLE FREQUENCY WAVEFORMS





Numbers at ends of terminals denote pin numbers for L package Numbers in parenthesis denote pin numbers for F package

Characteristic		-30°C		+25	o°C	+85		
	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Drain Current	ΙE				50			mAdd
Input Current	lin	-	-	-	250	-	-	μAdc
Input Leakage Current	1 _R	-	-		100	-	- 1	μAdc
Reference Voltage	V _{BB}	- 1.375	-1.275	-1.35	-1.25	-1.30	-1.20	Vdc
Switching Times Propagation Delay	t ⁻⁺ t ⁺⁻	0.6 0.6	1.6 1.8	0.6 0.6	1.5 1.7	0.6 0.6	1.7 1.9	ns
Rise Time, Fall Time (10% to 90%)	t+,t-	0.6	2.2	0.6	2.1	0.6	2.3	ns

APPLICATION INFORMATION

The MC1692 guad line receiver is used primarily to receive data from balanced twisted pair lines, as indicated in Figure 1. The line is driven with a MC1660 OR/NOR gate. The MC1660 is terminated with 50 ohm resistors to -2.0 volts. At the end of the twisted pair a 100 ohm termination resistor is placed across

the differential line receiver inputs of the MC1692. Illustrated in Figure 2 is the sending and receiving waveforms at a data rate of 400 megabits per second over an 18 foot twisted pair cable. The

waveform picture of Figure 3 shows a 5 nanosecond pulse being propagated down the 18 foot line. The delay time for the line is 1.68 ns/foot.

The MC1692 may also be applied as a high frequency schmitt trigger as illustrated in Figure 4. This circuit has been used in excess of 200 MHz. The MC1692 when loaded into 50 ohms will produce an output rising edge of about 1.5 nanoseconds.

MC1660

1/4 18 Ft MC1692 Twisted € 100 Pair 50 50 € \$ 50 V_{EE} = -5.2 Vdc Output Loading Factor = 70 VTT = - 2 V 0 V_{TT} = -2 V

FIGURE 1 - LINE DRIVER/RECEIVER

FIGURE 2 - 400 MBS WAVEFORMS

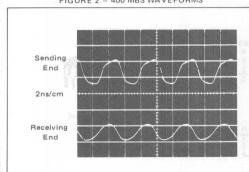
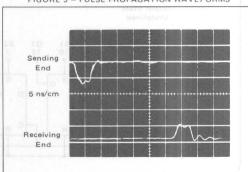
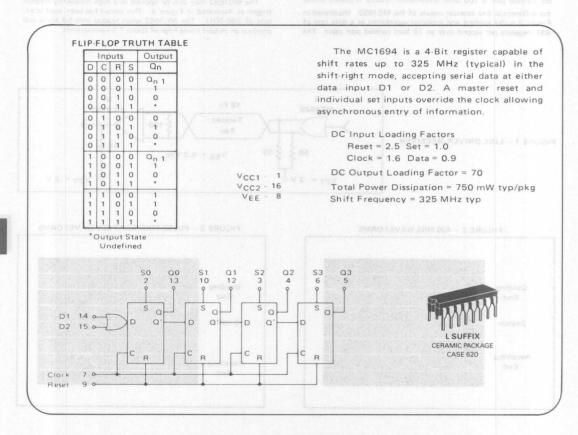


FIGURE 3 - PULSE PROPAGATION WAVEFORMS



VEE = -5.2 V 0.01 µF MC1692 \$50 MC1692 0.01 0.01 50 € μF ~~~ 500 -100 VTT = -2 V

FIGURE 4 - 200 MHz SCHMITT TRIGGER



		-30°C		+25°C		+85°C			
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit	
Power Supply Drain Current	1E	-	-	-	200	_	-	mAdd	
Input Current	linH				-			mAdd	
Pin 9		346	30	-	1.0	14.	-		
Pin 7		-	1	-	0.75	Der	-	17-4	
Pins 2,3,6,10		- 6	\- I	-	0.6	X-1:	-		
Pins 14,15	383	-	-	-	0.5	-	-		
Switching Times	1	7		1 3	9.1			ns	
Propagation Delay	tpd		-		-			41111	
Clock		1.0	3.2	1.0	3.0	1.0	3.4		
Set, Reset		2.0	3.9	2.0	3.7	2.0	4.1		
Rise Time (10% to 90%)	t+	1.0	2.9	1.0	2.7	1.0	3.1	ns	
Fall Time (10% to 90%)	t-	1.0	2.8	1.0	2.6	1.0	3.0	ns	
Shift Rate	THE RES	240	_	275	-	250	_	MHz	

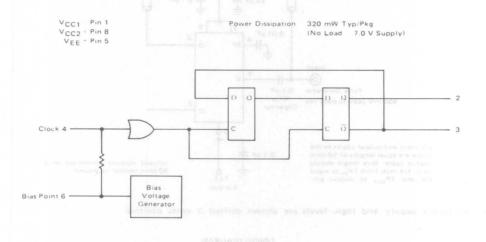
1-GHz DIVIDE-BY-FOUR

PRESCALER

The MC1697 is a divide-by-four gigahertz prescaler in an 8 pin package. The clock input requires an ac coupled driving signal of 800 mV amplitude (typical). The clock toggles two divide-by-two stages, and the complementary outputs (50% duty cycle) are taken from the second stage.

The complementary outputs are capable of driving 50-ohm lines

Pin 6 is available for connection of a decoupling capacitor to ground. This capacitor stabilizes the reference point which is internally coupled to the clock input.



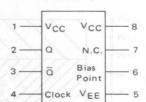
PIN ASSIGNMENT



P SUFFIX PLASTIC PACKAGE CASE 626



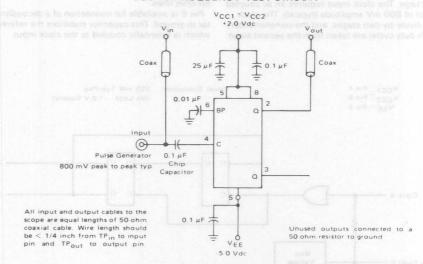
L SUFFIX CERAMIC PACKAGE CASE 693



ELECTRICAL CHARACTERISTICS

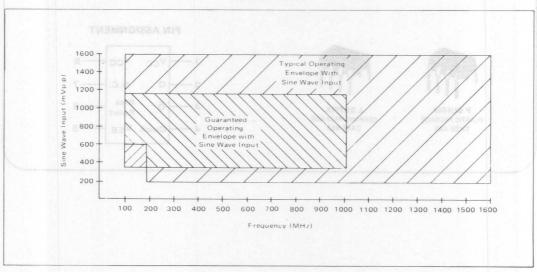
			3.48.60					
		0°C		+25°C		+75°C		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Drain Current	1E	-	-	-	57		-	mAdo
Toggle Frequency (high frequency operation)	f _{Tog}	1.0	-	1.0	-	1.0	-	GHz
Toggle Frequency (low frequency sine wave input)	f _{Tog}	-	-	-	100	-	-	MHz

COUNT FREQUENCY TEST CIRCUIT



Note: All power supply and logic levels are shown shifted 2 volts positive.

TIMING DIAGRAM



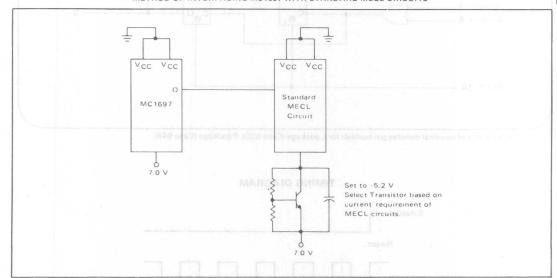
NELEI B∀♥ dialie-ey-four gellereitz counter

APPLICATION INFORMATION

XIPPUS : SOLVENS :

The MC1697 is a very high speed divide-by-four prescaler designed to operate on a nominal supply voltage of -7.0 volt. In some applications it may be necessary to interface the output of the MC1697 with other MECL circuits requiring a supply voltage of -5.2 volts. One method of interfacing the circuits is shown below. This configuration is adequate for frequencies up to 1 GHz over the temperature range of 0° to ±75°C. For best performance it is recommended that separate regulated supplies be used.

METHOD OF INTERFACING MC1697 WITH STANDARD MECL CIRCUITS



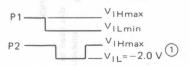
4-48

Q (7)

ELECTRICAL CHARACTERISTICS

		-3	0°C	+2	5°C	+8	5°C	9.2	2 2 2
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit	Conditions
Power Supply Drain Current	IE.	-		or by	57	5387	-	mAdc	All inputs and outputs open except Clock = V _{IHC} ≅ -4.0 Vdc
Input Current Reset Enable	linH		- 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1	1 10 Language 1	500 265			μAdc	VIHmax to Reset, VIL to Enable, VEE to Clock. VILmin to reset, VIHmax to Enable, VEE to Clock.
Logic "1" Output Voltage	VOH	-1.085	-0.875	-1.000	-0.810	-0.930	-0.700	Vdc	See Note 2 . Or, apply P1 to Reset and VIHmax
Logic "0" Output Voltage	VOL	-	-1.630	2 E	-1.600	-	-1.555	Vdc	to Enable
Toggle Frequency (high frequency operation)	fTog	1.0	\$-3 5	1.0	Toldia Toldia	1.0	-	GHz	VIL to Enable.
Toggle Frequency (low frequency sine wave input)	fTog	-	or opposite	state of	100	St. Design	-	MHz	See Test Circuit and Application Information on next page.

- 1 Enable input requires $V_{1L} = -2.0 \text{ V max}$.
- \bigcirc Reset counter by applying pulse P1 to pin 14, then toggle outputs by applying pulse P2 to pin 4 for 2 cycles. Hold power during pulse sequence. Hold clock input \bigcirc V_E.



TOGGLE FREQUENCY TEST CIRCUIT VCC1 = VCC2 Vout Vin +2.0 Vdc Coax 〒0.1 μF Coax 0.01 µF BP 0 Pulse Generator Input 800 mV peak to peak typ 0.1 MF Chip Capacitor a Note: All power supply and logic levels All input and output cables to the are shown shifted 2 volts positive. scope are equal lengths of 50-ohm coaxial cable. Wire length should Unused outputs connected to a be < 1/4 inch from TP_{in} to input 50-ohm resistor to ground. pin and TPout to output pin. VEE -5.0 Vdc

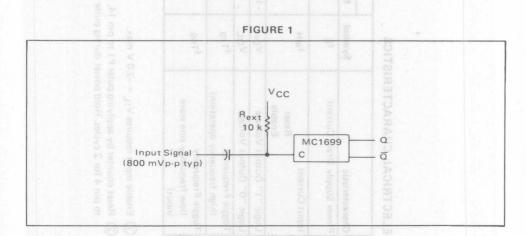
APPLICATION INFORMATION

The MC1699 is a very high speed divide-byfour counter intended for prescaler applications. The reset provides increased flexibility for counter and time measuring requirements.

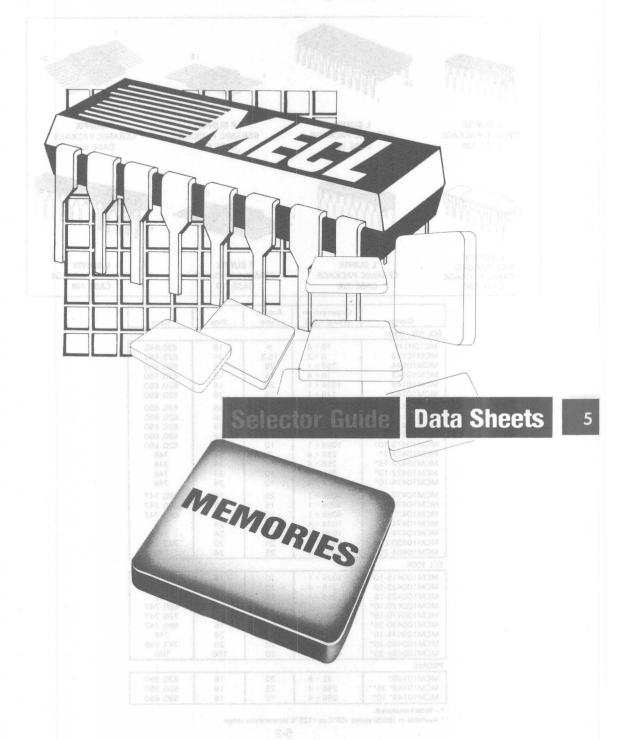
The clock input is designed to accept a capacitor-coupled sine wave signal for frequencies above 100 MHz. Below 100 MHz waveshaping is recommended to obtain good MECL III or MECL 10,000 edge speeds.

With a continuous input signal the clock can be capacitor-coupled with no problems. How-

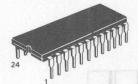
ever, if the clock is interrupted and the clock input floats to the bias point reference voltage, the counter may oscillate. To prevent this oscillation, an external resistor can be added as shown in Figure 1. This resistor is recommended only when the clock is interrupted and serves no useful function with a continuous signal. Also, this external resistor is not required when the enable input is used to gate the clock signal.



ECL Memories



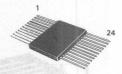
L SUFFIX CERAMIC PACKAGE CASE 620



L SUFFIX CERAMIC PACKAGE CASE 623



F SUFFIX CERAMIC PACKAGE CASE 650



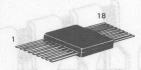
F SUFFIX CERAMIC PACKAGE CASE 652



L SUFFIX SIDE BRAISED CERAMIC PACKAGE CASE 680



L SUFFIX CERAMIC PACKAGE CASE 726



F SUFFIX CERAMIC PACKAGE CASE 747



L SUFFIX CERAMIC PACKAGE CASE 748

Device	Organization (Word × Bit)	Access Time	Pins	Case
ECL 10K, 10KH				
MC10H145	16 × 4	6	16	620,648
MCM10143	8 × 2	15.3	24	623, 652
MCM10144	256 × 1	26	16	620, 650
MCM10145	16 × 4	15	16	620, 650
MCM10146	1024 × 1	29	16	620, 650
MCM10147	128 × 1	15	16	620, 650
MCM10148	64 × 1	15	16	620, 650
MCM10152	256 × 1	15	16	620, 650
MCM10415-20	1024 × 1	20	16	620, 650
MCM10415-15	1024 × 1	15	16	620, 650
MCM10415-10*	1024 × 1	10	16	620, 650
MCM10422-7*	256 × 4	7	24	748
MCM10422-15*	256 × 4	15	24	748
MCM10422-10*	256 × 4	10	24	748
MCM10474-10*	1024 × 4	10	24	748
MCM10470-25*	4096 × 1	25	18	680, 747
MCM10470-15*	4096 × 1	15	18	680, 747
MCM10470-10*	4096 × 1	10	18	680, 747
MCM10474-25*	1024 × 4	25	24	748
MCM10474-15*	1024 × 4	15	24	748
MCM10480-25*	16384 × 1	25	20	747, 748
MCM10484-25*	4096 × 4	25	24	748
ECL 100K	504			
MCM100415-10*	1024 × 1	10	16	620, 650
MCM100422-10	256 × 4	10	24	652, 748
MCM100422-15	256 × 4	15	24	748
MCM100470-10*	4096 × 1	10	18	680, 747
MCM100470-15*	4096 × 1	15	18	726, 747
MCM100470-25*	4096 × 1	25	18	680, 747
MCM100474-15*	1024 × 4	15	24	748
MCM100480-20*	16384 × 1	20	20	747, 748
MCM100484-20*	4096 × 4	20	TBD	TBD
PROMS				
MCM10139*	32 + 8	20	16	620, 650
MCM10149* 25**	256 + 4	25	16	620, 650
MCM10149* 10*	256 + 4	10	16	620, 650

^{*-}To be introduced.

^{**} Available in 10500 series -55°C to +125°C temperature range.

MOTOROLA

256-BIT PROGRAMMABLE READ ONLY MEMORY (PROM)

The MCM10139 is a 256-bit programmable read only memory (PROM). The circuit is organized as 32 words of 8 bits. Prior to programming, all stored bits are at logic 0 (low) levels. The logic state of each bit can then be changed by on-chip programming circuitry. The MCM10139 has a single negative logic chip enable. When the chip is disabled $(\overline{\text{CS}} = \text{high})$, all outputs are forced to a logic 0 (low).

The MCM10139 is fully compatible with the MECL 10,000 logic family. It is designed for use in microprogramming, code conversion, logic simulation, and look-up table storage.

 P_D = 520 mW typ/pkg (No Load) t_{Access} = 15 ns typ (Address Inputs)

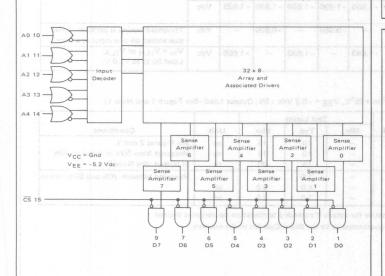
MECL

32 X 8 BIT PROGRAMMABLE READ-ONLY MEMORY

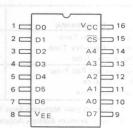




LOGIC DIAGRAM



PIN ASSIGNMENT



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5

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit	
Power Supply Voltage (V _{CC} = 0)	VEE	-8 to 0	Vdc	
Base Input Voltage (V _{CC} = 0)	Vin	0 to VEE	Vdc	
Output Source Current — Continuous — Surge	10	<50 <100	mAdc	DAR BURNMARE READ
Junction Operating Temperature	TJ	<165	°C	(MORS)
Storage Temperature Range	T _{stg}	-55 to +150	°C	

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS MADE AGE & A SET MADE AGE are exceeded.

ELECTRICAL CHARACTERISTICS

Test Temperature	DC Test Voltage Values (Volts)									
	VIHmax	VILmin	VIHAmin	VILAmax	VEE					
0°C	-0.840	-1.870	-1.145	-1.490	-5.2					
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2					
+75°C	-0.720	-1.830	-1.045	-1.450	-5.2					

Each MECL Memory circuit has been designed to meet the dc and ac specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

			MC	M10139	Test Li	nits			
		0	°C	+2!	5°C	+75	5°C		
DC Characteristics	Symbol	Min	Max	Min	Max	Min	Max	Unit	Conditions
Power Supply Drain Current	IEE	-	150	-	145	-	140	mAdc	Typ IEE @ 25°C = 100 mA. All out puts and inputs open. Measure pin 8
Input Current High	linH	-	265	-	265	-	265	μAdc	Test one input at a time, all other inputs are open. V _{in} = V _{IH} .
Input Current Low	linL	0.5		0.5	-	0.3	-	μAdc	Test one input at a time, all other inputs are open. V _{in} = V _{IL} .
Logic "1" Output Voltage	Vон	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	Vdc	Load 50 Ω to -2.0 V.
Logic "0" Output Voltage	VOL	-2.010	-1.665	-1.990	-1.650	-1.970	-1.625	Vdc	
Logic "1" Threshold Voltage	Vона	-1.020		-0.980	-	-0.920	-	Vdc	Threshold testing is performed and guaranteed on one input at a time.
Logic "0" Threshold Voltage	VOLA	-	-1.645	-	-1.630	-	-1.605	Vdc	$V_{in} = V_{ILH}$ or V_{ILA} . Load 50 Ω to -2.0 V .

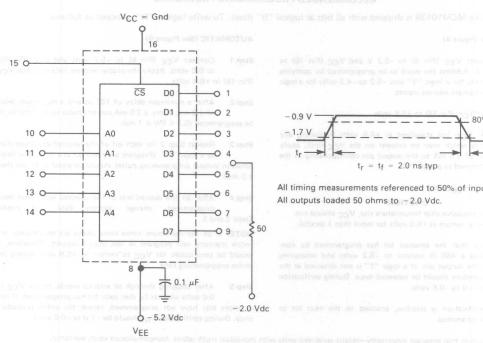
SWITCHING CHARACTERISTICS (T_A = 0° to +75°C, V_{EE} = -5.2 Vdc \pm 5%; Output Load—See Figure 1 and Note 1)

province-			Test Limit	s		
Characteristic	Symbol	Min	Тур	Max	Unit	Conditions
Chip Select Access Time	tACS	_10046	10	15	ns	See Figures 2 and 3.
Chip Select Recovery Time	tRCS	- 6	10	15	ns	Measured from 50% of input to 50%
Address Access Time	tAA	1-15	15	20	ns	of output. See Note 2.
Output Rise and Fall Time	tr, tf	- 1	3.0	151H(170A)	ns	Measured between 20% and 80% points
Input Capacitance	Cin	- 1	4.0	5.0	pF	
Output Capacitance	Cout		7.0	8.0	pF	

Notes: 1. Contact your Motorola Sales Representative for details if extended temperature operation is desired.

2. The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the memory.

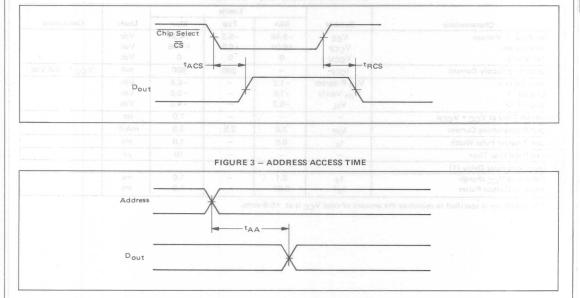
FIGURE 1 — SWITCHING TIME TEST CIRCUIT





All timing measurements referenced to 50% of input levels. All outputs loaded 50 ohms to -2.0 Vdc.

FIGURE 2 - CHIP SELECT ACCESS TIME



The MCM10139 is shipped with all bits at logical "0" (low). To write logical "1s", proceed as follows.

MANUAL (See Figure 4)

Step 1 Connect V_{EE} (Pin 8) to -5.2 V and V_{CC} (Pin 16) to 0.0 V. Address the word to be programmed by applying -1.2 to -0.6 volts for a logic "1" and -5.2 to -4.2 volts for a logic "0" to the appropriate address inputs.

Step 2 Raise V_{CC} (Pin 16) to +6.8 volts.

Step 3 After V_{CC} has stabilized at +6.8 volts (including any ringing which may be present on the V_{CC} line), apply a current pulse of 2.5 mA to the output pin corresponding to the bit to be programmed to a logic "1".

Step 4 Return V_{CC} to 0.0 Volts:

CAUTION TO SE ESCOPE ALLEGANDES

To prevent excessive chip temperature rise, V_{CC} should not be allowed to remain at +6.8 volts for more than 1 second.

Step 5 Verify that the selected bit has programmed by connecting a 460 Ω resistor to -5.2 volts and measuring the voltage at the output pin. If a logic "1" is not detected at the output, the procedure should be repeated once. During verification V_{1H} should be -1.0 to -0.6 volts.

Step 6 If verification is positive, proceed to the next bit to be programmed.

AUTOMATIC (See Figure 5)

Step 1 Connect V_{EE} (Pin 8) to -5.2 volts and V_{CC} (Pin 16) to 0.0 volts. Apply the proper address data and raise V_{CC} (Pin 16) to +6.8 volts.

Step 2 After a minimum delay of 100 μ s and a maximum delay of 1.0 ms, apply a 2.5 mA current pulse to the first bit to be programmed (0.1 \leq PW \leq 1 ms).

Step 3 Repeat Step 2 for each bit of the selected word specified as a logic "1". (Program only one bit at a time. The delay between output programming pulses should be equal to or less than 1.0 ms.)

Step 4 After all the desired bits of the selected word have been programmed, change address data and repeat Steps 2 and 3.

NOTE: If all the maximum times listed above are maintained, the entire memory will program in less than 1 second. Therefore, it would be permissible for V_{CC} to remain at +6.8 volts during the entire programming time.

Step 5 After stepping through all address words, return V_{CC} to 0.0 volts and verify that each bit has programmed. If one or more bits have not programmed, repeat the entire procedure once. During verification V_{TH} should be -1.0 to -0.6 volts.

*NOTE: For devices that program incorrectly-return serialized units with individual truth tables. Noncompliance voids warranty.

PROGRAMMING SPECIFICATIONS

			Limits			
Characteristic	Symbol	Min	Тур	Max	Units	Conditions
Power Supply Voltage	VEE	-5.46	-5.2	-4.94	Vdc	
To Program	VCCP	+6.04	+6.8	+7.56	Vdc	
To Verify	Vccv	0	0	0	Vdc	
Programming Supply Current	ICCP		200	600	mA	V _{CC} = +6.8 Vdc
Address Voltage	VIH Program	-1.2	N -	-0.6	Vdc	
Logical "1"	VIH Verify	-1.0	17 -	-0.6	Vdc	1 25 9 9 9
Logical "0"	VIL	-5.2		-4.2	Vdc	
Maximum Time at V _{CC} = V _{CCP}			_	1.0	sec	
Output Programming Current	IOP	2.0	2.5	3.0	mAdc	
Output Program Pulse Width	tp	0.5	- 1	1.0	ms	
Output Pulse Rise Time	-	-	-	10	μs	I Should be
Programming Pulse Delay (1)	Shell Scholan	E TRIULE	SHUGHT		III SELL	
Following V _{CC} change	t _d	0.1	-	1.0	ms	
Between Output Pulses	t _d 1	0.01	-	1.0	ms	

NOTE 1. Maximum is specified to minimize the amount of time V_{CC} is at +6.8 volts.

5

FIGURE 4 - MANUAL PROGRAMMING CIRCUIT

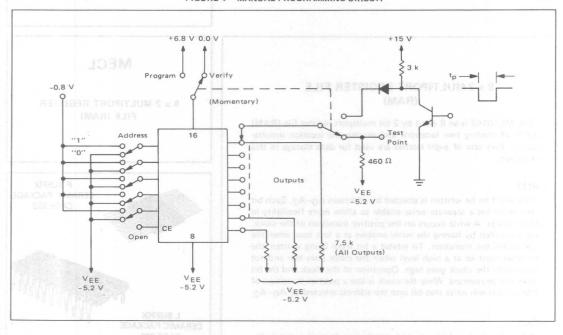
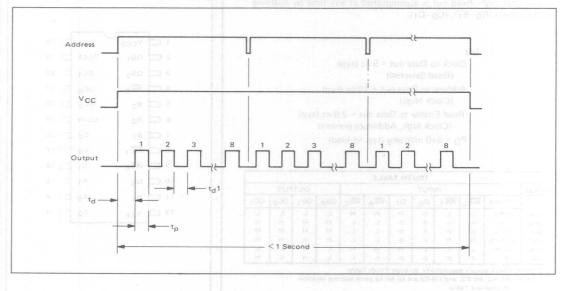


FIGURE 5 - AUTOMATIC PROGRAMMING CIRCUIT



F SUFFIX

PIN ASSIGNMENT

CASE 623

1 🗖	Vcco	Vcc	b	24
2 🗀	QB ₁	V _{CC1}		23
3 🖂	ΩВ0	QC ₁		22
4 🗆	REB	QC ₀		21
5 🖂	В2	REC		20
6 🖂	Во	Clock		19
7 🖂	В1	C ₂		18
8 🖂	WE ₁	C ₀	þ	17
9 🖂	WE 0	C ₁	Þ	16
10 🖂	Do	A 1		15
11 🖂	D ₁	A ₀		14
12 🖂	VEE	A ₂	þ	13

8 x 2 MULTIPORT REGISTER FILE (RAM)

The MC10143 is an 8 word by 2 bit multiport register file (RAM) capable of reading two locations and writing one location simultaneously. Two sets of eight latches are used for data storage in this LSI circuit.

WRITE

The word to be written is selected by addresses A₀-A₂. Each bit of the word has a separate write enable to allow more flexibility in system design. A write occurs on the positive transition of the clock. Data is enabled by having the write enables at a low level when the clock makes the transition. To inhibit a bit from being written, the bit enable must be at a high level when the clock goes low and not change until the clock goes high. Operation of the clock and the bit enables can be reversed. While the clock is low a positive transition of the bit enable will write that bit into the address selected by A₀-A₂.

READ

When the clock is high any two words may be read out simultaneously, as selected by addresses B_0-B_2 and C_0-C_2 , including the word written during the preceding half clock cycle. When the clock goes low the addressed data is stored in the slaves. Level changes on the read address lines have no effect on the output until the clock again goes high. Read out is accomplished at any time by enabling output gates (B_0-B_1) , (C_0-C_1) .

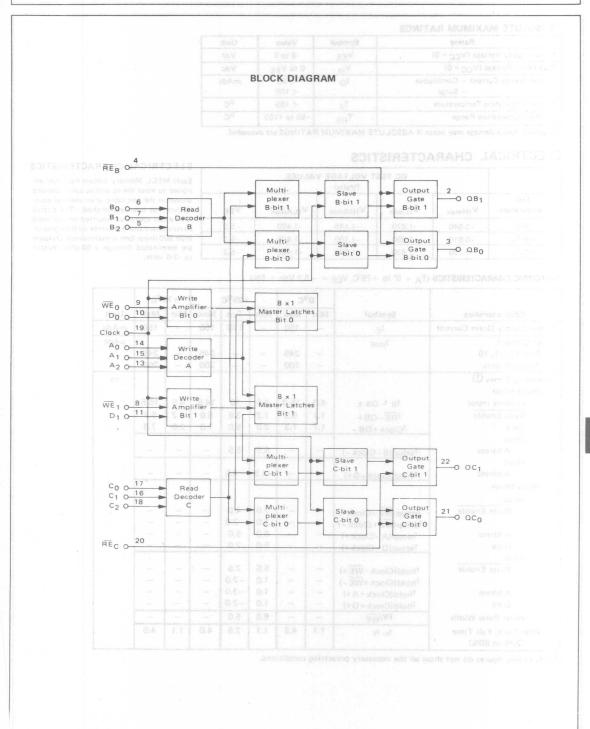
> tpd: Clock to Data out = 5 ns (typ) (Read Selected) Address to Data out = 10 ns (typ) (Clock High) Read Enable to Data out = 2.8 ns (typ) (Clock high, Addresses present) PD = 610 mW/pkg (typ no load)

				TRU	TH TA	ABLE						
*MODE INPUT									OUTPUT			
	**Clock	WEO	WE ₁	D ₀	D ₁	REB	REC	QB ₀	QB ₁	QC ₀	QC ₁	
Write	L→H	L	L	Н	Н	Н	н	L	L	L	L	
Read	н	0	0	ø	0	L	L	Н	н	н	Н	
Read	H→L	Ø.	Φ	0	0	L	L	Н	Н	H	Н	
Read	L→H→L	Н	Н	0	0	L	L	н	н	н	н	
Write	L→H	L	L	L	н	н	н	L	L	of !	L	
Read	н	φ'	Φ	Φ	Φ	L	L	L	н	L	н	

**Note: Clock occurs sequentially through Truth Table

*Note: A0-A2, B0-B2, and C0-C2 are all set to same address location throughout Table.

φ = Don't Care



ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (V _{CC} = 0)	VEE	-8 to 0	Vdc
Base Input Voltage (V _{CC} = 0)	Vin	0 to VEE	Vdc
Output Source Current — Continuous — Surge	10	< 50 < 100	mAdc
Junction Operating Temperature	TJ	< 165	°C
Storage Temperature Range	T _{stg}	-55 to +150	°C

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

ELECTRICAL CHARACTERISTICS

Test Temperature	. 1	DC TEST VOLTAGE VALUES (Volts)									
	V _{IHmax}	VILmin	VIHAmin	VILAmax	VEE						
0°C	-0.840	-1.870	-1.145	-1.490	-5.2						
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2						
+75°C	-0.720	-1.830	-1.045	-1.450	-5.2						

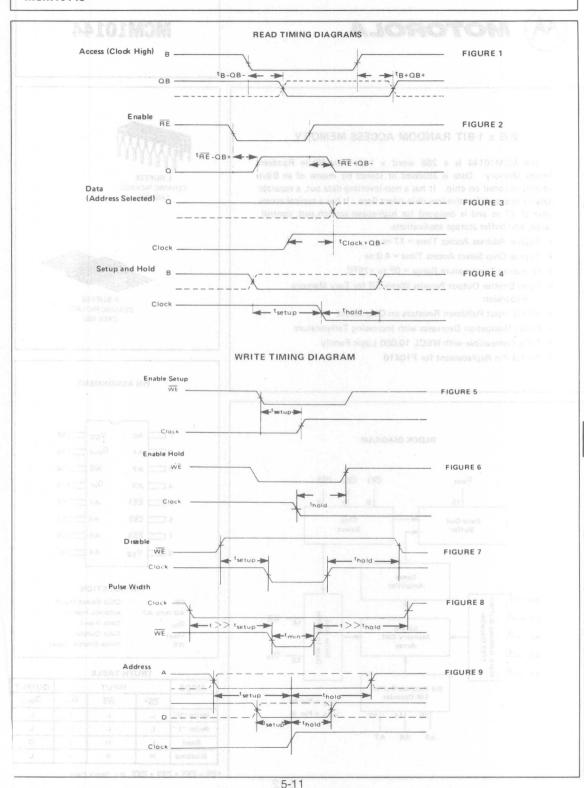
ELECTRICAL CHARACTERISTICS

Each MECL Memory circuit has been designed to meet the dc and ac specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

SWITCHING CHARACTERISTICS ($T_A = 0^{\circ}$ to $+75^{\circ}$ C, $V_{EE} = -5.2$ Vdc \pm 5%)

		0	°C		+25°C		+7	5°C	
Characteristics	Symbol	Min	Max	Min	Тур	Max	Min	Min Max	
Power Supply Drain Current	1 _E	1	150		118	150	-	150	mAde
Input Current	linH						400	21	μAdd
Pins 10, 11, 19		-	245	-	4.	245	550	245	45 1A
All other pins		-	200	-	+	200	-	200	40 SA
Switching Times ①									ns
Read Mode			1.6.6						
Address Input	tB ± QB ±	4.0	15.3	4.5	10	14.5	4.5	15.5	10 179
Read Enable	tRE-QB+	1.1	5.3	1.2	3.5	5.0	1.2	5.5	-0 . a
Data	tClock+QB-	1.7	7.3	2.0	5.0	7.0	2.0	7.6	
Setup		A VI							
Address	tsetup(B-Clock-)	-	-	8.5	5.5	-	-	-	
Hold	NAME OF THE OWNER.	H-45-10	10.4	ora P	71				
Address	thold(Clock - B+)	-		-1.5	-4.5	-	-	-	
Write Mode						b	199		-0.00
Setup		-	-	-	14	- an	Dec	40 81	-0 12
Write Enable	tsetup (WE - Clock +)	-	- 100	7.0	4.0	-	-	-	-0.83
	tsetup(WE+Clock-)	_	0	1.0	-2.0	-	-	-	
Address	tsetup(A -Clock+)	-	-	8.0	5.0	-	-	-	
Data	tsetup(D-Clock+)	_	-	5.0	2.0	_	-	- 10%	ec 381
Hold				1					
Write Enable	thold(Clock-WE+)	-	-	5.5	2.5	-	-	-	
	thold(Clock+WE-)	-	-	1.0	-2.0	-	-	-	7.4
Address	thold(Clock+A+)		-	1.0	-3.0	-	-	-	
Data	thold(Clock+D+)	-	-	1.0	-2.0	-	-	-	
Write Pulse Width	PWWE	-	-	8.0	5.0	-	-	-	
Rise Time, Fall Time (20% to 80%)	t _r , t _f	1.1	4.2	1.1	2.5	4.0	1.1	4.5	

1) AC timing figures do not show all the necessary presetting conditions.





MCM10144

256 x 1-BIT RANDOM ACCESS MEMORY

The MCM10144 is a 256 word x 1-bit Read/Write Random Access Memory. Data is accessed or stored by means of an 8-bit address decoded on chip. It has a non-inverting data out, a separate data in line and 3 active-low chip select lines. It has a typical access time of 17 ns and is designed for high-speed scratch pad, control, cache, and buffer storage applications.

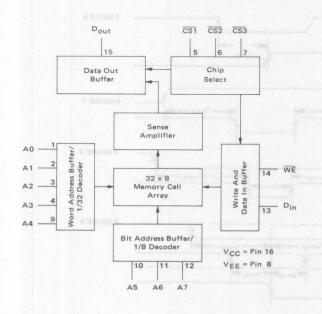
- Typical Address Access Time = 17 ns
- Typical Chip Select Access Time = 4.0 ns
- Operating Temperature Range = 0° to +75°C
- Open Emitter Output Permits Wired-OR for Easy Memory Expansion
- 50 kΩ Input Pulldown Resistors on Chip Select
- Power Dissipation Decreases with Increasing Temperature
- Fully Compatible with MECL 10,000 Logic Family
- Pin-for-Pin Replacement for F10410



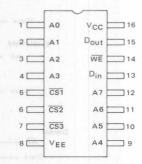


F SUFFIX CERAMIC PACKAGE CASE 650

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NOTATION

CS	
A0 thru A7	
Din	
Dout	

WE

Chip Select Input Address Inputs Data Input

Data Output Write Enable Input

TRUTH TABLE

MODE		OUTPUT		
	CS*	WE	Din	Dout
Write "0"	L	L	L	L
Write "1"	L	L	н	L
Read	L	Н	φ	a
Disabled	н	φ	φ	L

 $^{\circ}$ CS = $\overline{\text{CS1}}$ + $\overline{\text{CS2}}$ + $\overline{\text{CS3}}$ ϕ = Don't Care.

5

FUNCTIONAL DESCRIPTION:

The MCM10144 is a 256 word x 1-bit RAM. Bit selection is achieved by means of an 8-bit address A0 thru A7.

The active-low chip select allows memory expansion up to 2048 words. The fast chip select access time allows memory expansion without affecting system performance.

The operating mode of the RAM ($\overline{\text{CS}}$ inputs low) is controlled by the $\overline{\text{WE}}$ input. With $\overline{\text{WE}}$ low the chip is in the write mode—the output is low and the data present at D_{in} is stored at the selected address. With $\overline{\text{WE}}$ high the chip is in the read mode—the data state at the selected memory location is presented non-inverted at D_{OUT}.

ABSOLUTE MAXIMUM RATINGS

A Rating a en as = up	Symbol	Value	Unit
Power Supply Voltage (V _{CC} = 0)	VEE	-8 to 0	Vdc
Base Input Voltage (V _{CC} = 0)	Vin	0 to VEE	Vdc
Output Source Current — Continuous — Surge	10 01	< 50 < 100	mAdc
Junction Operating Temperature	TJ	< 165	°C
Storage Temperature Range 1 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4	T _{stg}	-55 to +150	°C

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

		DC TES	VOLTAGE (Volts)	VALUES	
Test Temperature	VIHmax	VILmin	VIHAmin	VILAmax	VEE
0°C	-0.840	-1.870	-1,145	-1.490	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+75°C	-0.720	-1.830	-1.045	-1.450	-5.2

ELECTRICAL CHARACTERISTICS

Each MECL Memory circuit has been designed to meet the dc and ac specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

		1 - X	1	MCM10144	Test Lim	its				
		0	°C	+2!	5°C	+75	5°C			
DC Characteristics	Symbol	Min	Max	Min	Max	Min	Max	Unit	Conditions	
Power Supply Drain Current	IEE	12-12-1 1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-	130	- v. <u>ē</u> .o+	125	-	120	mAdc	Typ IEE @ 25°C = 90 mA All outputs and inputs open. Measure pin 8.	
Input Current High	l _{in} H d an 0.5 =	h = h	220	- AF	220	-	220	μAdc	Test one input at a time, all other inputs are open. Vin = VIH.	
Input Current Low, and to all	a d _{in} ton	0.5	enna-mes	0.5	HA -	0.3	- 15 tuc	μAdc	Test one input at a time, all other inputs are open. Vin = VIL.	
Logic "1" Output Voltage	VOH	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	Vdc	Load 50 Ω to -2.0 V	
Logic ''0'' Output Voltage	VOL	-1.870	-1.665	-1.850	-1.650	-1.830	-1.625	Vdc	61	
Logic ''1'' Threshold Voltage	Vона	-1.020	-	-0.980	-	-0.920	1	Vdc	Threshold testing is performed and guaranteed on one input a	
Logic ''0'' Threshold Voltage	VOLA	-	-1.645	-	-1.630	-	-1.605	Vdc	a time. $V_{in} = V_{IHA}$ or V_{ILA} Load 50 Ω to -2.0 V .	

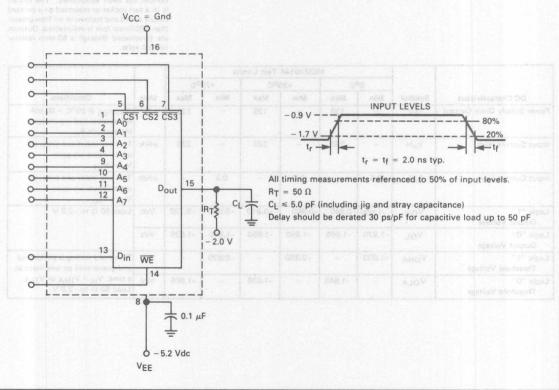
All decision of high contract of the state o	Service Pro-	ALTERNATIVE STATE	Test Limi	ts	William.	that K blow aga a steel of the John an	
Characteristic	Symbol	Symbol Min Ty		Max	Unit	Conditions	
Read Mode	1.39 100102	er till h		पूर्व नाव्यक्त	NA SXE	See Figures 2 and 3.	
Chip Select Access Time	TACS	2.0	4.0	10	ns	Measured from 50% of input to 50% of	
Chip Select Recovery Time	tRCS	2.0	4.0	10	ns	output. See Note 2.	
Address Access Time	tAA	7.0	17	26	ns		
Write Mode							
Write Pulse Width	tw	25	6.0	-	ns	twsA = 8.0 ns	
Data Setup Time Prior to Write	twsp	2.0	-3.0	-	ns	Measured at 50% of input to 50% of	
Data Hold Time After Write	tWHD	2.0	-3.0	-	ns	output.	
Address Setup Time Prior to Write	tWSA	8.0	0	4,767	ns	tw = 25 ns. See Figure 4.	
Address Hold Time After Write	tWHA	0.0	-4.0		ns	to supply Value of Vere # 01	
Chip Select Setup Time Prior to Write	twscs	2.0	-3.0	-	ns	10 - an V sparieV reant	
Chip Select Hold Time After Write	twhcs	2.0	-3.0	- 13	ns	A STATE OF THE PARTY OF THE PAR	
Write Disable Time	tws	2.5	5.0	10	ns	out Schies Burrint - Continues	
Write Recovery Time	twR	2.5	5.0	10	ns	apres -	
Rise and Fall Time	2					Measured between 20% and 80% points	
Output Rise and Fall Time	tr, tf	1.5	3.0	7.0	ns	When driven from Address inputs.	
Output Rise and Fall Time	tr, tf	1.5	3.0	5.0	ns	When driven from CS or WE inputs.	
Capacitance	-				-		
Input Capacitance	Cin	_	4.0	5.0	pF	17 50	
Output Capacitance	Cout	_	7.0	8.0	pF		

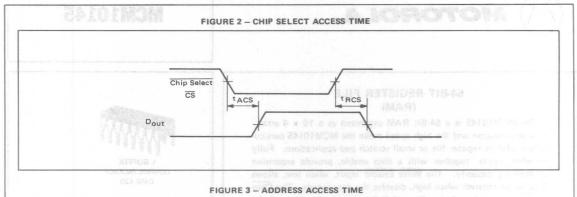
Notes: (1) Contact your Motorola Sales Representative for details if extended temperature operation is desired.

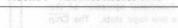
(2) The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.

(3) For proper use of MECL Memories in a system environment, consult: "MECL System Design Handbook."

FIGURE 1 — SWITCHING TIME TEST CIRCUIT







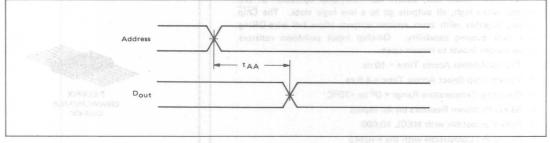
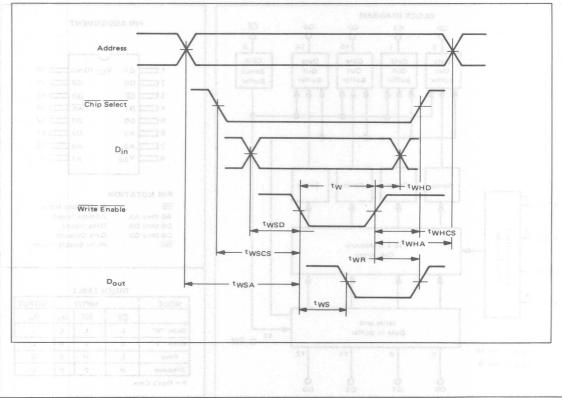


FIGURE 4 - WRITE MODE



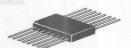
MCM10145

64-BIT REGISTER FILE (RAM)

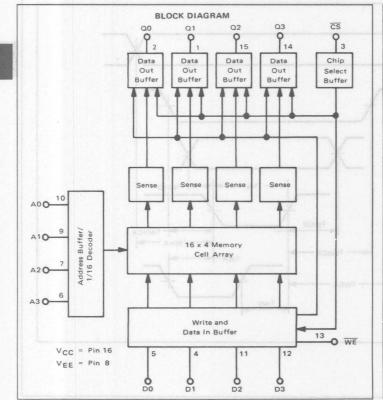
The MCM10145 is a 64-Bit RAM organized as a 16 x 4 array. This organization and the high speed make the MCM10145 particularly useful in register file or small scratch pad applications. Fully decoded inputs, together with a chip enable, provide expansion of memory capacity. The Write Enable input, when low, allows data to be entered; when high, disables the data inputs. The Chip Select input when low, allows full functional operation of the device; when high, all outputs go to a low logic state. The Chip Select, together with open emitter outputs allow full wire-ORing and data bussing capability. On-chip input pulldown resistors allow unused inputs to remain open.

- Typical Address Access Time = 10 ns
- Typical Chip Select Access Time = 4.5 ns
- Operating Temperature Range = 0° to +75°C
- 50 kΩ Pulldown Resistors on All Inputs
- Fully Compatible with MECL 10,000
- Pin-for-Pin Compatible with the F10145

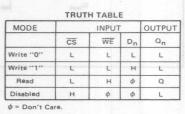




F SUFFIX CERAMIC PACKAGE CASE 650



PIN ASSIGNMENT VCC (Gnd) 01 2 [00 02 7 15 CS 03 7 14 D1 7 13 D3 12 A3 A0 10 7 A2 VEE 9 8 PIN NOTATION Chip Select Input A0 thru A3 Address Inputs D0 thru D3 Data Inputs Q0 thru Q3 Data Outputs WE Write Enable Input TRUTH TABLE



5

FUNCTIONAL DESCRIPTION:

The MCM10145 is a 16 word x 4-bit RAM. Bit selection is achieved by means of a 4-bit address A0 thru A3.

The active-low chip select allows memory expansion up to 32 words. The fast chip select access time allows memory expansion without affecting system performance.

The operating mode of the RAM (\overline{CS}) input low) is controlled by the \overline{WE} input. With \overline{WE} low the chip is in the write mode—the output is low and the data present at D_n is stored at the selected address. With \overline{WE} high the chip is in the read mode—the data state at the selected memory location is presented non-inverted at Q_n .

ABSOLUTE MAXIMUM RATINGS

712002012 111/1/1110111 11/111100			
Rating	Symbol	Value	Unit
Power Supply Voltage (V _{CC} = 0)	VEE	-8 to 0	Vdc
Base Input Voltage (V _{CC} = 0)	Vin	0 to VEE	Vdc
Output Source Current — Continuous — Surge	as 10 -	< 50 < 100	mAdc
Junction Operating Temperature	en TJ -	< 165	O OC MAN
Storage Temperature Range	T _{stg}	-55 to +150	°C

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

	DC TEST VOLTAGE VALUES (Volts)								
Test Temperature	VIHmax	VILmin	VIHAmin	VILAmax	VEE				
0°C	-0.840	-1.870	-1.145	-1.490	-5.2				
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2				
+75°C	-0.720	-1.830	-1.045	-1.450	-5.2				

ELECTRICAL CHARACTERISTICS

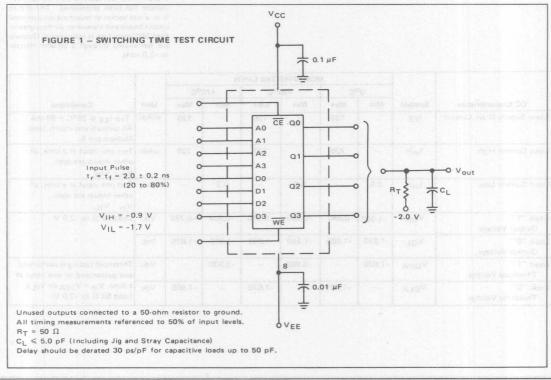
Each MECL Memory circuit has been designed to meet the dc and ac specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

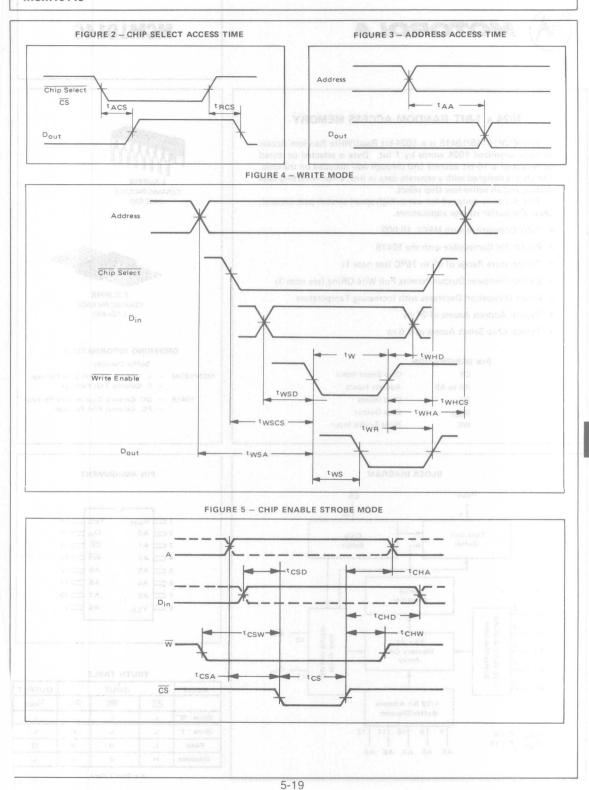
				VCM10145	Test Lim	its				
		0	°С	+2!	5°C	+7!	5°C			
DC Characteristics	Symbol	Min	Max	Min	Max	Min	Max	Unit	Conditions	
Power Supply Drain Current	IEE		130	- Foo!	125	-	120	m Adc	Typ IEE @ 25°C = 90 mA All outputs and inputs open. Measure pin 8.	
Input Current High	linH		220	70	220		220	μAdc	Test one input at a time, all other inputs are open. Vin = VIH.	
Input Current Low	link	0.5		0,5	- e - 29	0.3	0	μAdc	Test one input at a time, all other inputs are open. Vin VIL.	
Logic ''1'' Output Voltage	VOH	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	Vdc	Load 50 Ω to −2.0 V	
Logic ''0'' Output Voltage	VOL	-1.870	-1.665	-1.850	-1.650	-1.830	-1.625	Vdc		
Logic ''1'' Threshold Voltage	Vона	-1.020	-	-0.980	- 1	-0.920	-	Vdc	Threshold testing is performed and guaranteed on one input at	
Logic ''0'' Threshold Voltage	VOLA	-	-1.645	0 产	-1.630	-	-1.605	Vdc	a time. $V_{in} = V_{IHA}$ or V_{ILA} Load 50 Ω to -2.0 V .	

Chip Select Access Time	1	2.0	4.5	8.0	ns	Measured from 50% of input to 50% of
Chip Select Access Time	t ACS	2.0	5.0	8.0	ns	output. See Note 1.
Address Access Time	tRCS tAA	4.0	10	15	ns	the sid-A a to smean vid bevoince at a
Write Mode	Je byłnozi	t Davis		gu hoisne	dank a.te	The act veriew drift serest allows mean
Write Pulse Width	tw	8.0	_	ewo ll a er	ns	twsA = 5 ns
Data Setup Time Prior to Write	twsp	0	-6.0	son a mia	ns	Measured at 50% of input to 50% of
Data Hold Time After Write	tWHD	3.0	0	-	ns	output.
Address Setup Time Prior to Write	twsA	5.0	1.0	_	ns	tw = 8 ns. See Figure 4.
Address Hold Time After Write	tWHA	1.0	-3.0	-	ns	
Chip Select Setup Time Prior to Write	twscs	0	-5.0	-	ns	
Chip Select Hold Time After Write	twics	0	-6.0	-	ns	
Write Disable Time	tws	2.0	5.0	8.0	ns	
Write Recovery Time	twR	2.0	5.0	8.0	ns	SOLUTE MAXIMUM RATINGS
Chip Enable Strobe Mode	I fire	FILE	Walter	1 loon	-e I	anisoli
Data Setup Prior to Chip Select	tCSD	0	-6.0	-	ns	Guaranteed but not tested on standard
Write Enable Setup Prior to Chip Select	tCSW	0	-3.0	- 48	ns	product. See Figure 5.
Address Setup Prior to Chip Select	tCSA	0	-3.0	- 0	ns	bout Source Content - Continuous
Data Hold Time After Chip Select	tCHD	2.0	-1.0	-	ns	49/4/2
Write Enable Hold Time After Chip	tCHW	0	-6.0	- 11	ns	chian Cestating Terrocoture
Select	5					rage Temperature Range
Address Hold Time After Chip Select	tCHA	4.0	-1.0	l	ns	
Chip Select Minimum Pulse Width	tcs	18	12	PI-NE JANES	ns	COSSA fi resse and open ab talvio trisna
Rise and Fall Time			830	NV BOAT	20 V 12	Measured between 20% and 80% points.
Address to Output	t _r , t _f	1.5	3.0	7.0	ns	
CS to Output	tr, tf	1.5	3.0	5.0	ns	The state of the s
Capacitance		N I	Ramak JI	rome	MIN	minutes are summer and are compared
Input Capacitance	Cin	-	4.0	6.0	pF	0.55 - 0.550 - 2.500
Output Capacitance	Cout		5.0	8.0	pF	

Notes:

- 1. The maximum Address Access Time is guaranteed to be the worst-case bit in the memory.
- 2. For proper use of MECL Memories in a system environment, consult MECL System Design Handbook.





MCM10146

1024 x 1-BIT RANDOM ACCESS MEMORY

The MCM10146/10415 is a 1024-bit Read/Write Random Access Memory organized 1024 words by 1 bit. Data is selected or stored by means of a 10-bit address (A0 through A9) decoded on the chip. The chip is designed with a separate data in line, a non-inverting data output, and an active-low chip select.

This device is designed for use in high-speed scratch pad, control, cache and buffer storage applications.

- Fully Compatible with MECL 10,000
- Pin-for-Pin Compatible with the 10415
- Temperature Range of 0° to 75°C (see note 1)
- Emitter-Follower Output Permits Full Wire-ORing (see note 3)
- Power Dissipation Decreases with Increasing Temperature
- Typical Address Access of 24 ns
- Typical Chip Select Access of 4.0 ns

PIN DESIGNATION

CS A0 to A9 Chip Select Input

Din

Address Inputs Data Inputs

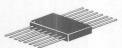
Dout

Data Output

Write Enable Input



CERAMIC PACKAGE CASE 620



FSUFFIX CERAMIC PACKAGE CASE 650

ORDERING INFORMATION

Suffix Denotes

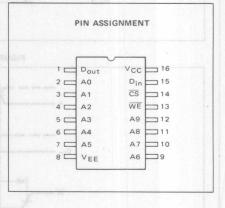
MCM10146 - L Ceramic Dual-in-Line Package

- F Ceramic Flat Package

10415 - DC Ceramic Dual-in-Line Package

- FC Ceramic Flat Package

BLOCK DIAGRAM Data Out Chip Buffer Select Amplifier 13 32 x 32 P. Q Memory Cell Write A 1/32 Wor Buffer/ Wol - Din 15 1/32 Bit Address Buffer/Decoder VEE = Pin 8 VCC = Pin 16 A5 A6 A7 A8 A9



TRUTH TABLE

MODE	25	OUTPUT		
	CS	WE	Din	Dout
Write "0"	L	L	L	L
Write "1"	L	L	н	L
Read	L	Н	φ	Q
Disabled	н	φ	Φ	L

 ϕ = Don't Care.

FUNCTIONAL DESCRIPTION: THE PROPERTY OF THE PR

This device is a 1024×1 -bit RAM. Bit selection is achieved by means of a 10-bit address, A0 to A9.

The active-low chip select is provided for memory expansion up to 2048 words.

The operating mode of the RAM (CS input low) is controlled by the \overline{WE} input. With \overline{WE} low, the chip is in the write mode, the output, $D_{out},$ is low and the data state present at D_{in} is stored at the selected address. With \overline{WE} high, the chip is in the read mode and the data stored at the selected memory location will be presented non-inverted at $D_{out}.$ (See Truth Table)

ABSOLUTE MAXIMUM RATINGS

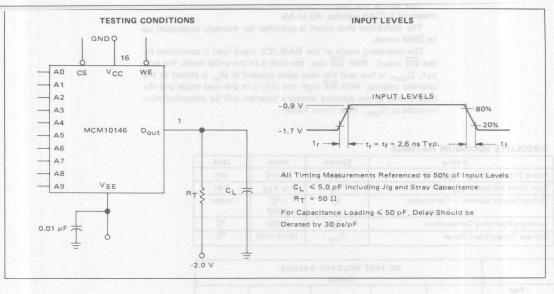
Rating	Symbol	Value	Unit
Power Supply Voltage (VCC = 0)	VEE	-8 to 0	Vdc
Base Input Voltage (VCC = 0)	Vin	0 to VEE	Vdc
Output Source Current — Continuous — Surge —	10	< 50 < 100	mAdc
Junction Operating Temperature	RewTJ) C. vo	< 165	°C
Storage Temperature Range	T _{stg}	-55 to +150	°C

		DC TES	(Volts)	VALUES	
Test Temperature	VIHmax	VILmin	VIHAmin	VILAmax	VEE
0°C	-0.840	-1.870	-1.145	-1.490	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+75°C	-0.720	-1.830	-1.045	-1,450	-5.2

ELECTRICAL CHARACTERISTICS

Each MECL Memory circuit has been designed to meet the dc and ac specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

			N N	1CM10146	Test Limi	ts	CHW		BROW SING A STOUT	
	2.744	00	0°C		+25°C		+75°C		Wigner Prior to We	
DC Characteristics	Symbol	Min	Max	Min	Max	Min	Max	Unit	Conditions	
Power Supply Drain Current	IEE	-	150		145	0.2	125	mAdc	Typ I _{EE} @ 25 ^o C = 100 mA All outputs and inputs open. Measure pin 8.	
Input Current High	I _{in} H	- prosta	220	07	220	8.5	220	μAdc	Test one input at a time, all other inputs are open. Vin = VIH.	
Input Current Low	morn newd	0.5	245 245	0.5	0.5	0.3	11.21	μAdc	Test one input at a time, all other inputs are open. Vin = VIL.	
Logic "1" Output Voltage	Vон	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	Vdc	Load 50 Ω to -2.0 V	
Logic ''0'' Output Voltage	VOL	-1.920	-1.665	-1.900	-1.650	-1.880	-1.625	Vdc		
Logic ''1'' Threshold Voltage	Vона	-1.020	renstif pro	-0.980	the Worse	-0.920	nemore a	Vdc	Threshold testing is performed and guaranteed on one input at	
Logic ''0'' Threshold Voltage	VOLA	FI regustion	-1.645	III _MED Jing:	-1.630	rebris 30	-1.605	Vdc	a time. $V_{in} = V_{IHA}$ or V_{ILA} . Load 50 Ω to -2.0 V .	



Guaranteed with $V_{FF} = -5.2 \text{ Vdc} \pm 5.0\%$, $T_{\Delta} = 0^{\circ}\text{C}$ to 75°C (see Note 1). Output Load see Figure 1.

		MCM	10146 Test	Limits					
Characteristic	Symbol	Min	Тур	Max	Unit	Conditions			
Read Mode Market Vision M. 103M 15	4 June	100	91797		0.90,	See Figures 2 and	3.		
Chip Select Access Time	tACS	2.0	4.0	7.0	ns	Measured at 50% of input to 50% of output.			
Chip Select Recovery Time	tRCS	2.0	4.0	7.0	ns	See Note 2.			
Address Access Time	tAA	8.0	24	29	ns				
Write Mode					THE SAME	See Figure 4.			
Write Pulse Width (To guarantee writing)	tW	25	20	-	ns	tWSA = 8.0 ns. Measured at 50%	of input to 50% of output.		
Data Setup Time Prior to Write	twsp	5.0	0	-	ns				
Data Hold Time After Write	twHD	5.0	0	eto mener	ns				
Address Setup Time Prior to Write	twsA	8.0	0		ns	t _W = 25 ns			
Address Hold Time After Write	tWHA	2.0	0	(ni#	ns	niff ledmy2			
Chip Select Setup Time Prior to Write	twscs	5.0	0	-	ns	1 30			
Chip Select Hold Time After Write	twhcs	5.0	0	- 1	ns				
Write Disable Time	tws	2.8	5.0	7.0	ns				
Write Recovery Time	twR	2.8	5.0	7.0	ns	that that	right the nuO to		
Rise and Fall Time						Measured between	20% and 80% points.		
Output Rise and Fall Time	tr, tf	1.5	2.5	4.0	ns	When driven from	CS or WE inputs.		
Output Rise and Fall Time	t _r , t _f	1.5	4.0	8.0	ns	When driven from	Address inputs.		
Capacitance						Measured with a p	oulse technique.		
Input Lead Capacitance	Cin	100 E	4.0	5.0	pF	000 t- 1 HOV			
Output Lead Capacitance	Cout	- 1	7.0	8.0	pF				

Notes:

- (1) Contact your Motorola Sales Representative for details if extended temperature operation is desired.
- (2) The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
- (3) For proper use of MECL Memories in a system environment, consult: "MECL System Design Handbook."
- (4) Typical limits are at $V_{EE} = -5.2 \text{ Vdc}$, $T_A = 25^{\circ}\text{C}$ and standard loading.

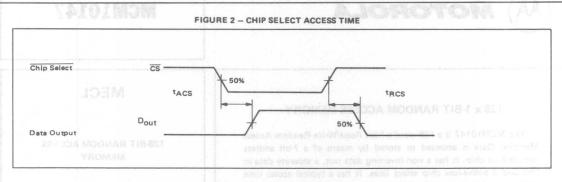


FIGURE 3 - ADDRESS ACCESS TIME TO DESIGN TO THE PROPERTY OF TH

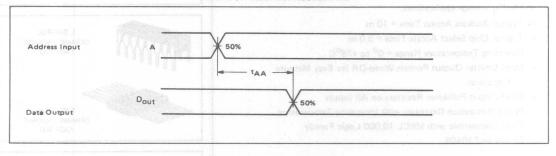
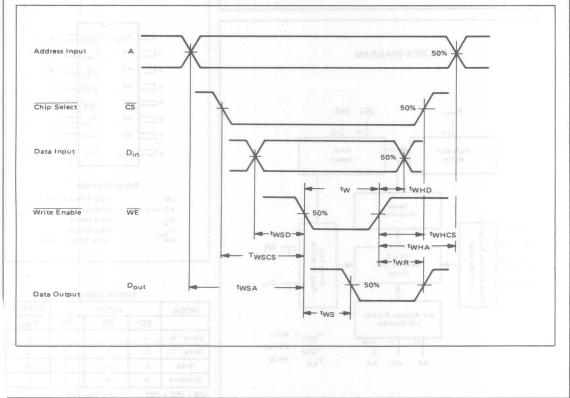


FIGURE 4 - WRITE STROBE MODE



MCM10147

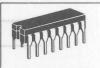
128 x 1-BIT RANDOM ACCESS MEMORY

The MCM10147 is a 128-word x 1-bit Read/Write Random Access Memory. Data is accessed or stored by means of a 7-bit address decoded on chip. It has a non-inverting data out, a separate data in line and 2 active-low chip select lines. It has a typical access time of 10 ns and is designed for high-speed scratch pads, control, cache, and buffer storage applications.

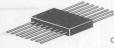
- Typical Address Access Time = 10 ns
- Typical Chip Select Access Time = 5.0 ns
- Operating Temperature Range = 0° to +75°C
- Open Emitter Output Permits Wired-OR for Easy Memory Expansion
- 50 kΩ Input Pulldown Resistors on All Inputs
- Power Dissipation Decreases with Increasing Temperature
- Fully Compatible with MECL 10,000 Logic Family
- · Similar to F10405.

MECL

128-BIT RANDOM ACCESS MEMORY

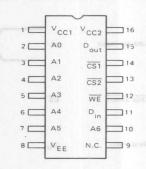


L SUFFIX CERAMIC PACKAGE CASE 620



F SUFFIX CERAMIC PACKAGE CASE 650

PIN ASSIGNMENT



PIN NOTATION

CS A0 thru A6 Din Dout WE Chip Select Input
Address Inputs
Data Input

Data Output Write Enable Input

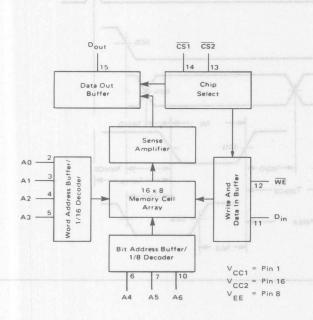
TRUTH TABLE

				and the second second
MODE		OUTPUT		
	₹S*	WE	Din	Dout
Write "0"	L	L	L	L
Write "1"	L	L	Н	L
Read	L	Н	φ	Q
Disabled	н	φ	φ	L

*CS = CS1 + CS2

 ϕ = Don't Care.

BLOCK DIAGRAM



5-24

5

FUNCTIONAL DESCRIPTION:

The MCM 10147 is a 128 word x 1-bit RAM. Bit selection is achieved by means of a 7-bit address A0 thru A6.

The active-low chip select allows memory expansion up to 512 words. The fast chip select access time allows memory expansion without affecting system performance.

The operating mode of the RAM ($\overline{\text{CS}}$ inputs low) is controlled by the $\overline{\text{WE}}$ input. With $\overline{\text{WE}}$ low the chip is in the write mode—the output is low and the data present at Din is stored at the selected address. With $\overline{\text{WE}}$ high the chip is in the read mode—the data state at the selected memory location is presented non-inverted at Dout.

ABSOLUTE MAXIMUM RATINGS

Rating #8 4n 0.6 = 44	Symbol	Value	Unit
Power Supply Voltage (VCC = 0)	VEE	-8 to 0	Vdc
Base Input Voltage (V _{CC} = 0)	Vin	0 to VEE	Vdc
Output Source Current — Continuous — Surge	10 0.8	< 50 < 100	mAdc
Junction Operating Temperature	TJ	< 165	°C
Storage Temperature Range	T _{stg} a.a	-55 to +150	°C

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

		DC TES	(Volts)	VALUES	
Test Temperature	V _{IHmax}	VILmin	VIHAmin	VILAmax	VEE
0°C	-0.840	-1.870	-1.145	-1.490	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+75°C	-0.720	-1.830	-1.045	1.450	-5.2

ELECTRICAL CHARACTERISTICS

Each MECL Memory circuit has been designed to meet the dc and ac specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

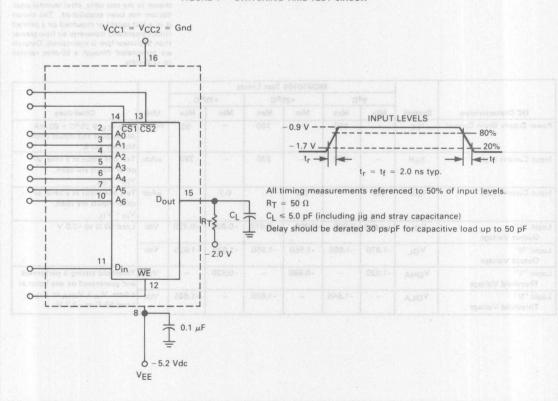
				MCM10144	Test Lim	its				
	Symbol	0	0°C		+25°C		5°C	- 1		
DC Characteristics		Min	Max	Min	Max	Min	Max	Unit	Conditions	
Power Supply Drain Current	IEE		105	V-2.0-	100	-	95	mAdc	Typ IEE @ 25°C = 80 mA All outputs and inputs open. Measure pin 8.	
Input Current High	I _{in} H ayi an 0.5	- H = 4	220	6- 1-	220	-	220	μAdc	Test one input at a time, all other inputs are open. Vin = VIH.	
Input Current Low	I _{in} L	0.5	nerratire electron	0.5	18 I	0.3	8= 11	μAdc	Test one input at a time, all other inputs are open. Vin = VIL.	
Logic "1" Output Voltage	Voн	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	Vdc	Load 50 Ω to -2.0 V	
Logic ''0'' Output Voltage	VOL	-1.870	-1.665	-1.850	-1.650	-1.830	-1.625	Vdc	111	
Logic ''1'' Threshold Voltage	Vона	-1.020	-	-0.980	-	-0.920	- L	Vdc	Threshold testing is performed and guaranteed on one input at	
Logic ''0'' Threshold Voltage	VOLA	-	-1.645	-	-1.630	-	-1.605	Vdc	a time. $V_{in} = V_{IHA}$ or V_{ILA} . Load 50 Ω to -2.0 V .	

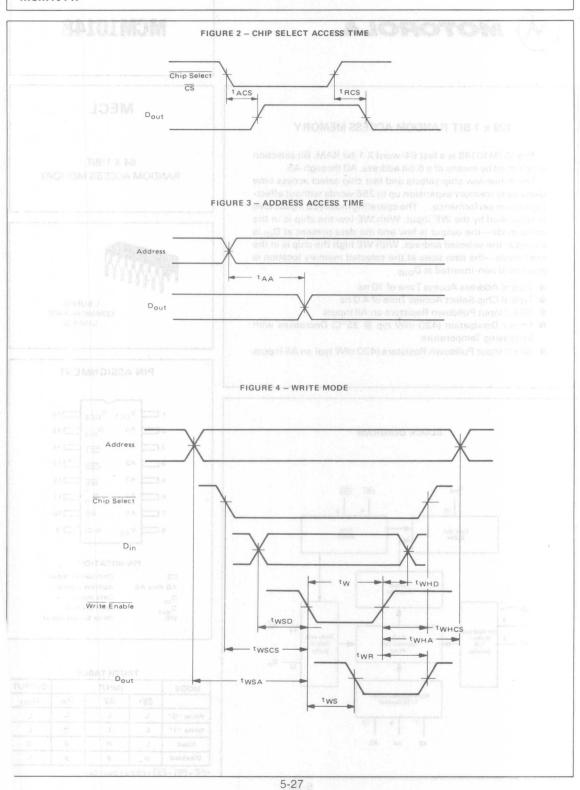
e made with the lost the chip is	by the W	agliouns	Test Limi	ts	MARI	DET K BROW BEST IS IT EASTER WITH MIT
Characteristic	Symbol	Min	Тур	Max	Unit	Conditions Conditions
Read Mode	to the cost of	a new t		QU GOISIS	MAKO YO	See Figures 2 and 3.
Chip Select Access Time	tACS	2.0	5.0	8.0	ns	Measured from 50% of input to 50% of
Chip Select Recovery Time	tRCS	2.0	5.0	8.0	ns	output. See Note 2.
Address Access Time	tAA	5.0	10	15	ns	
Write Mode			I STATE OF			
Write Pulse Width	tw	8.0	6.0	-	ns	tWSA = 4.0 ns
Data Setup Time Prior to Write	twsp	1.0	-5.0	-	ns	
Data Hold Time After Write	tWHD	3.0	-2.0	-	ns	SOLUTE MAXIMUM RATINOS
Address Setup Time Prior to Write	tWSA	4.0	0	-todas	ns	t _W = 8.0 ns. See Figure 4.
Address Hold Time After Write	tWHA	3.0	0	- 0.01	ns	er Supply Voltage (Voc = 0)
Chip Select Setup Time Prior to Write	twscs	1.0	-5.0		ns	
Chip Select Hold Time After Write	twhcs	1.0	-5.0	4	ns	(0 + 55V) sessio / ruani i
Write Disable Time	tws	2.0	5.0	8.0	ns	Measured at 50% of input to 50%
Write Recovery Time	twR	2.0	5.0	8.0	ns	of output.
Rise and Fall Time			2815	12		Measured between 20% and 80% points.
Output Rise and Fall Time	tr, tf	1.5	3.0	5.0	ns	nge Tanigeratura Punga
Capacitance	parents		5.32911	LO LELANIN	5.60 271	and the state of the state of the state of
Input Capacitance	Cin		4.0	5.0	pF	00 78
Output Capacitance	Cout	_	7.0	8.0	pF	

(2) The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.

(3) For proper use of MECL Memories in a system environment, consult: "MECL System Design Handbook."

FIGURE 1 — SWITCHING TIME TEST CIRCUIT





MCM10148

128 x 1-BIT RANDOM ACCESS MEMORY

The MCM10148 is a fast 64-word X 1-bit RAM. Bit selection is achieved by means of a 6-bit address, A0 through A5.

The active-low chip selects and fast chip select access time allow easy memory expansion up to 256 words without affecting system performance. The operating mode (CS inputs low) is controlled by the WE input. With WE low the chip is in the write mode—the output is low and the data present at $D_{\mbox{\scriptsize in}}$ is stored at the selected address. With WE high the chip is in the read mode—the data state at the selected memory location is presented non-inverted at $D_{\mbox{\scriptsize out}}$.

- Typical Address Access Time of 10 ns
- Typical Chip Select Access Time of 4.0 ns
- 50 kΩ Input Pulldown Resistors on All Inputs
- Power Dissipation (420 mW typ @ 25°C) Decreases with Increasing Temperature
- 50 kΩ Input Pulldown Resistors (420 mW typ) on All Inputs

MECL

64 X 1-BIT RANDOM ACCESS MEMORY



L SUFFIX CERAMIC PACKAGE CASE 620

PIN ASSIGNMENT



PIN NOTATION

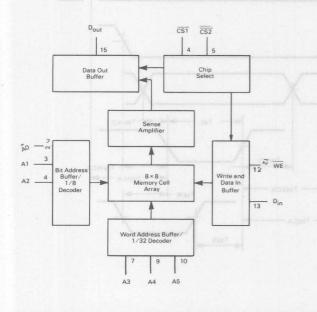
CS Chip Select Input
A0 thru A6 Address Inputs
Din Data Input
Dout Data Output
WE Write Enable Input

TRUTH TABLE

MODE		OUTPUT		
	cs∗	WE	Din	Dout
Write "0"	L	L	L	L
Write "1"	L	L	н	L
Read	L	Н	φ	a
Disabled	н	φ	Φ	L

 $^{\circ}\overline{\text{CS}} = \overline{\text{CS1}} + \overline{\text{CS2}} + \overline{\text{CS3}} \phi = \text{Don't Care}$

BLOCK DIAGRAM



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ELECTRICAL CHARACTERISTICS

	0°C		+25°C		+75°C			
Characteristics	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Drain Current	IEE		105	-	100	74-13	95	mAdc
Input Current High	linH	1-	220	_	220	_	220	μAdc

^{-55°}C and +125°C test values apply to MC105xx devices only.

SWITCHING CHARACTERISTICS (Note 1)

	grammang	MCM	10148	ed ned	med ald if sen	
Characteristics	Symbol	T _A = 0 to +75°C, V _{EE} = -5.2 Vdc ±5%		Unit	Conditions	
		Min	Max	II) O pigo	a or bacard out	
Read Mode Chip Select Access Time Chip Select Recovery Time	tACS tRCS	_	7.5 7.5	ns	Measured from 50% of input to 50% of output. See Note 2.	
Address Access time	tAA	MUMI anti	15	HEDDA 321	W Typical Auton	
Write Mode	THE PHONE WAS	F-12 (1) 2-1		ns	tWSA = 5.0 ns	
Write Pulse Width	tw	8.0	MARKET SERV	Print Intelled	Measured at 50% of input	
Data Setup Time Prior to Write	twsp	3.0	_		to 50% of output.	
Data Hold Time After Write	tWHD	2.0	Nesizurs of	nunching s	tw = 8.0 ns.	
Address Setup Time Prior to Write	tWSA	5.0	G gyr Win S	Ad) mous	& Power Dissin	
Address Hold Time After Write	tWHA	3.0	sing Tempe	recondintal	Occreases N	
Chip Select Setup Time Prior to Write	twscs	3.0	-			
Chip Select Hold Time After Write	twhcs	0	-			
Write Disable Time	tws	2.0	7.5			
Write Recovery Time	tWR	2.0	7.5			
Rise and Fall Time	t _r , t _f	1.5	5.0	ns	Measured between 20% and 80% points.	
Capacitance Input Capacitance	C _{in}		5.0	pF	Measured with a pulse technique.	
Output Capacitance	Cout	_	8.0		technique.	

NOTES: 1. Test circuit characteristics: $R_T = 50\Omega$, MCM10148.

 $C_L \leqslant 5.0$ pF (including jig and stray capacitance)

Delay should be derated 30 ps/pF for capacitive load up to 50 pF.

2. The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.

3. For proper use of MECL Memories in a system environment, consult MECL System Design Handbook.

*To be determined; contact your Motorola representative for up-to-date information.



MCM10149*10 MCM10149*25

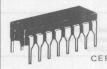
256 x 4-BIT PROGRAMMABLE READ-ONLY MEMORY

This device is a 256-word x 4-bit field programmable read only memory (PROM). Prior to programming, all stored bits are at logic 1 (high) levels. The logic state of each bit can then be changed by on-chip programming circuitry. The memory has a single negative logic chip enable. When the chip is disabled $(\overline{CS} = high)$, all outputs are forced to a logic 0 (low).

- Typical Address Access Time of 7.0 ns (MCM10149*10)
 20 ns (MCM10149*25)
- Typical Chip Select Access Time of 2.5 ns (MCM10149*10) 8.0 ns (MCM10149*25)
- ullet 50 k Ω Input Pulldown Resistors on All Inputs
- Power Dissipation (540 mW typ @ 25°C)
 Decreases with Increasing Temperature

MECL

1024-BIT PROGRAMMABLE READ-ONLY MEMORY



L SUFFIX
CERAMIC PACKAGE
CASE 620

F SUFFIX
CERAMIC PACKAGE
CASE 650



PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	0°C		+25°C		+75°C		SHIPS :
		Min	Max	Min	Max	Min	Max	Unit
Power Supply Drain Current	1EE	-	155	-	150	-	145	mAdd
Input Current High	linH	2 -	265		265	7	265	μAdc

.55°C and +125°C test values apply to MC105xx devices only.

Forcing Function	Parameter	0°C	25°C①	75°C ^①	
V _{IHmax} =	VOHmax	-0.840	-0.810	-0.720	
	VOHmin	-1.000	-0.960	-0.900	
SOLUV ROLL	VOHAmin	-1.020	-0.980	-0.920	
VIHAmin		-1.130	-1.105	-1.045	
VILAmax		-1.490	-1.475	-1.450	
	VOLAmax	-1.645	-1.630	-1.605	
	VOLmax	-1.665	-1.650	-1.625	
VILmin I	VOLmin	-1.870	-1.850	-1.830	
VILmin	NLmin	0.5	0.5	0.3	

NOTES: ① 0-75°C temperature range, 5011 to -2.0V.

SWITCHING CHARACTERISTICS (Note 1)

	emi T yel	MCM10149*25 T _A = 0 to +75°C, V _{EE} = -5.2 Vdc ±5%		MCM10149*10 T _A = 0 to 75°C, V _{EE} = -5.2 Vdc ±5%				
	Symbol							mego war, o paparec
Characteristics		Min	Max	Min	Тур.	Max	Unit	Conditions
Read Mode Chip Select Access Time Chip Select Recovery Time Address Access Time	tACS tRCS	2.0 2.0 7.0	10 10 25	am de sons	- - -	5.0 5.0 10	ns	Measured from 50% of input to 50% of output. See Note 1.
Rise and Fall Time	t _r , t _f	1.5	7.0	*	2.0	-42 Egg/	ns	Measured between 20% and 80% points.
Capacitance Input Capacitance Output Capacitance	C _{in}	- -	5.0 8.0	_	-	5.0 8.0	pF	Measured with a pulse technique.

NOTES: 1. Test circuit characteristics: $R_T = 50 \Omega$, MCM10149;

C_L ≤ 5.0 pF (including jig and stray capacitance)

Delay should be derated 30 ps/pF for capacitive load up to 50 pF

- 2. The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
- 3. For proper use of MECL Memories in a system environment, consult MECL System Design Handbook.
- 4. VCP = VCC = Gnd for normal operation.

*To be determined; contact your Motorola representative for up-to-date information.

PROGRAMMING THE MCM10149 To The State of the

During programming of the MCM 10149, input pins 7, 9, and 10 are addressed with standard MECL 10K logic levels. However, during programming input pins 2, 3, 4, 5, and 6 are addressed with 0 V \leq V $_{IH}$ \leq +0.25 V and V $_{EE}$ \leq V $_{IL}$ \leq -3.0 V. It should be stressed that this deviation from standard input levels is required only during the programming mode. During normal operation, standard MECL 10,000 input levels must be used.

With these requirements met, and with V_{CP} = V_{CC} =

0 V and V_{EE} = -5.2 V \pm 5%, the address is set up. After a minimum of 100 ns delay, V_{CP} (pin 1) is ramped up to + 12 V \pm 0.5 V (total voltage V_{CP} to V_{EE} is now 17.2 V, + 12 V - [-5.2 V]). The rise time of this V_{CP} voltage pulse should be in the 1 - 10 μ s range, while its pulse width (t_{W1}) should be greater than 100 μ s but less than 1 ms. The V_{CP} supply current at + 12 V will be approximately 525 mA while current drain from V_{CC} will be approximately 175 mA. A current limit should therefore be

set on both of these supplies. The current limit on the V $_{CP}$ supply should be set at 700 mA while the V $_{CC}$ supply should be limited to 250 mA. It should be noted that the V $_{EE}$ supply must be capable of sinking the combined current of the V $_{CC}$ and V $_{CP}$ supplies while maintaining a voltage of $-5.2~{\rm V}\pm5\%$.

Coincident with, or at some delay after the V_{CP} pulse has reached its 100% level, the desired bit to be fused can be selected. This is done by taking the corresponding output pin to a voltage of $\pm 2.85 \text{ V} \pm 5\%$. It is to be noted that only one bit is to be fused at a time. The other three unselected outputs should remain terminated through their 50 ohm load resistor to $\pm 2.0 \text{ V}$. Current into the selected output is 5 mA maximum.

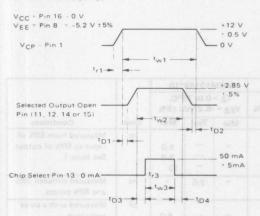
After the bit select pulse has been applied to the appropriate output, the fusing current is sourced out of the chip select pin 13. The 0% to 100% rise time of this current pulse should be 250 ns max. It pulse width should be greater than 100 μ s. Pulse magnitude is 50 mA \pm 5.0 mA. The voltage clamp on this current source is to be - 6.0 V.

After the fusing current source has returned 0 mA, the bit select pulse is returned to it initial level, i.e., the output is returned through its load to $-2.0\,\mathrm{V}$. Thereafter, $\mathrm{V_{CP}}$ is returned to 0 V. Strobing of the outputs to determine success in programming should occur no sooner than 100 ns after $\mathrm{V_{CP}}$ has returned to 0 V. The remaining bits are programmed in a similar fashion.

† NOTE: For devices that program incorrectly, return serialized units with individual truth tables. Non compliance voids warranty.

PROGRAMMING SPECIFICATIONS

The following timing diagrams and fusing information represent programming specifications for the MCM10149.

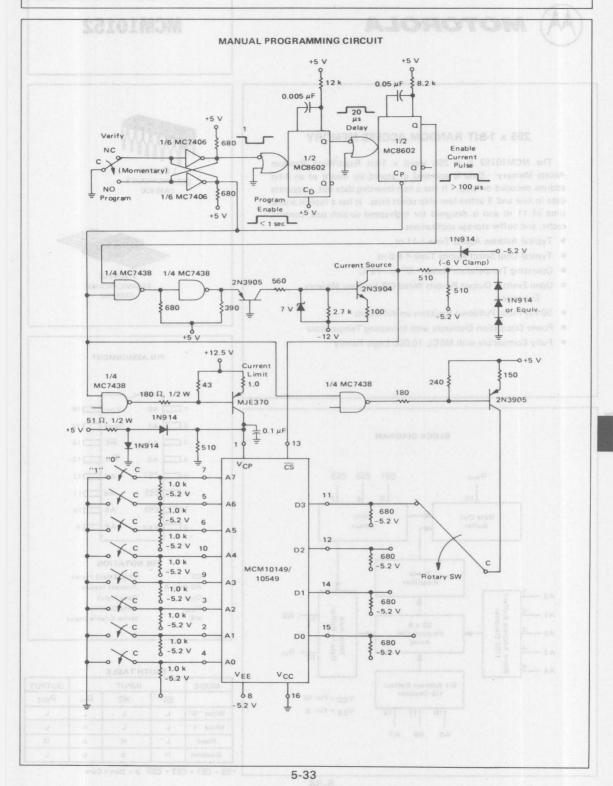


The timing diagram is shown for programming one bit. Note that only one bit is blown at a time. All addressing must be done 100 ns prior to the beginning of the V_{CP} pulse, i.e., $V_{CP} = 0$ V. Likewise, strobing of the outputs to determine success in programming should occur no sooner than 100 ns after V_{CP} returns to 0 V.

Note that the fusing current is defined as a positive current out of the chip select, pin 13. A programming duty cycle of \leq 15% is to be observed.

Definitions and values of timing symbols are

E.	a.0 a.0	
Symbol	Definition	Value
t _{r1}	Rise Time, Programming Voltage	≥ 1 μs
tw1	Pulse Width, Programming Voltage	≥ 100 μs < 1 ms
^t D1	Delay Time, Programming Voltage Pulse to Bit Select Pulse	≥ 0
tw2	Pulse Width, Bit Select	≥ 100 μs
t _{D2}	Delay Time, Bit Select Pulse to Programming Voltage Pulse	Program ≥ 0 qui j
t _{D3}	Delay Time, Bit Select Pulse to Programming Current Pulse	≥ 1 μs
t _{r3}	Rise Time, Programming Current Pulse	250 ns max
t _{w3}	Pulse Width, Programming Current Pulse	≥ 100 μs
tD4	Delay Time, Programming Current Pulse to Bit Select Pulse	





MCM10152

256 x 1-BIT RANDOM ACCESS MEMORY

The MCM10152 is a 256 word x 1-bit Read/Write Random Access Memory. Data is accessed or stored by means of an 8-bit address decoded on chip. It has a non-inverting data out, a separate data in line and 3 active-low chip select lines. It has a typical access time of 11 ns and is designed for high-speed scratch pad, control, cache, and buffer storage applications.

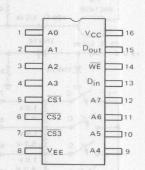
- Typical Address Access Time = 11 ns
- Typical Chip Select Access Time = 4.0 ns
- Operating Temperature Range = 0° to +75°C
- Open Emitter Output Permits Wired-OR for Easy Memory Expansion
- 50 kΩ Input Pulldown Resistors on All Inputs
- Power Dissipation Decreases with Increasing Temperature
- Fully Compatible with MECL 10,000 Logic Family





F SUFFIX CERAMIC PACKAGE CASE 650

PIN ASSIGNMENT



PIN NOTATION

CS Chip Select Input
A0 thru A7 Address Inputs
Din Data Input
Dout Data Output
WE Write Enable Input

TRUTH TABLE

MODE		OUTPUT		
	cs*	WE	Din	Dout
Write "0"	L	L	L	L
Write "1"	L	Ľ	Н	L
Read	L	Н	φ	Q
Disabled	н	φ	φ	L

* $\overline{\text{CS}} = \overline{\text{CS1}} + \overline{\text{CS2}} + \overline{\text{CS3}} \phi = \text{Don't Care.}$

BLOCK DIAGRAM Dout CS1 CS2 CS3 Data Out Chip Buffer Select Sense Amplifier Idress Buffe Decoder And 14 32 x 8 Memory Cell Write A d Addr 1/32 D Array Bit Address Buffer/ 1/8 Decoder VCC = Pin 16 VEE = Pin 8 A5 A6 A7

FUNCTIONAL DESCRIPTION:

The MCM10152 is a 256 word x 1-bit RAM. Bit selection is achieved by means of an 8-bit address A0 thru A7.

The active-low chip select allows memory expansion up to 2048 words. The fast chip select access time allows memory expansion without affecting system performance.

The operating mode of the RAM ($\overline{\text{CS}}$ inputs low) is controlled by the $\overline{\text{WE}}$ input. With $\overline{\text{WE}}$ low the chip is in the write mode—the output is low and the data present at Din is stored at the selected address. With $\overline{\text{WE}}$ high the chip is in the read mode—the data state at the selected memory location is presented non-inverted at Dout.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (VCC = 0)	VEE	-8 to 0	Vdc
Base Input Voltage (VCC = 0)	Vin	0 to VEE	Vdc
Output Source Current — Continuous — Surge	10	< 50 < 100	mAdc
Junction Operating Temperature	TJ	< 165	°C
Storage Temperature Range	T _{stg}	-55 to +150	°C

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

	DC TEST VOLTAGE VALUES								
			(Volts)						
Test Temperature	V _{IHmax}	VILmin	VIHAmin	VILAmax	VEE				
0°C	-0.840	-1.870	-1.145	-1.490	-5.2				
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2				
+75°C	-0.720	-1.830	-1.045	-1.450	-5.2				

ELECTRICAL CHARACTERISTICS

Each MECL Memory circuit has been designed to meet the dc and ac specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

			٨	ICM10152	Test Limi	ts		-		
		0°C		+25	+25°C		5°C			
DC Characteristics	Symbol	Min	Max	Min	Max	Min	Max	Unit	Conditions	
Power Supply Drain Current	IEE		135	MT.	130	-	125	mAdc	Typ IEE @ 25°C = 110 mA All outputs and inputs open. Measure pin 8.	
Input Current High	I _{in} H	F = 4	220	-	220	-	220	μAdc	Test one input at a time, all other inputs are open. Vin = VIH.	
Input Current Low	I _{in} L agas yam	0.5	gaibuloni	0.5	10年	0.3	100	μAdc	Test one input at a time, all other inputs are open. Vin = VIL.	
Logic "1" Output Voltage	Voн	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	Vdc	Load 50 Ω to -2.0 V	
Logic ''0'' Output Voltage	VOL	-1.870	-1.665	-1.850	-1.650	-1.830	-1.625	Vdc		
Logic "1" Threshold Voltage	Vона	-1.020	-	-0.980	-	-0.920		Vdc	Threshold testing is performed and guaranteed on one input at	
Logic ''0'' Threshold Voltage	VOLA	-	-1.645	-	-1.630	-	-1.605	Vdc	a time. $V_{in} = V_{IHA}$ or V_{ILA} Load 50 Ω to -2.0 V .	

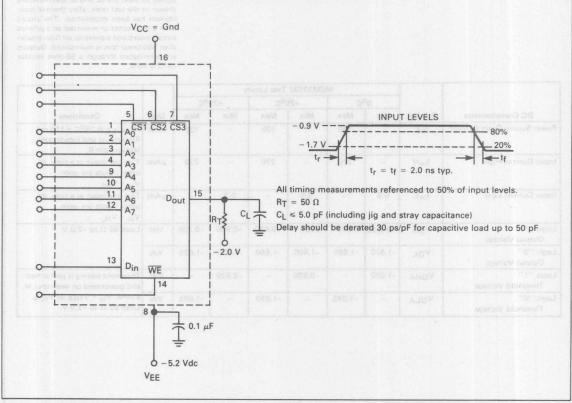
SWITCHING CHARACTERISTICS (TA = 0° to +75°C, VEE = -5.2 Vdc ± 5%; Output Load see Figure 1; see Note 1 & 3.1

with act was TW hilly topol BW	ed by the	Hostona.	Test Limit	S	MARI	The MCM 10152 is a 256 worst v 1.6	
Characteristic	Symbol	Min	Тур	Max	Unit	Conditions Conditions	
Read Mode	tie besteater	O to		ni opiami	ten vers	See Figures 2 and 3.	
Chip Select Access Time	tACS	2.0	4.0	7.5	ns	Measured from 50% of input to 50% of	
Chip Select Recovery Time	tRCS	2.0	4.0	7.5	ns	output. See Note 2.	
Address Access Time	tAA	7.0	11	15	ns	As full pause thouthat updated ye aroun	
Write Mode			1				
Write Pulse Width	tw	10	6.0	-	ns	twsA = 5.0 ns	
Data Setup Time Prior to Write	twsp	2.0	-3.0	-	ns	Measured at 50% of input to 50% of	
Data Hold Time After Write	tWHD	2.0	-2.0	-	ns	output. A G AR HAR WARE STEEL STEEL	
Address Setup Time Prior to Write	twsA	5.0	3.0	-	ns	tw = 10 ns. See Figure 4.	
Address Hold Time After Write	tWHA	3.0	0	aumy	ns	PRINCE OF THE PR	
Chip Select Setup Time Prior to Write	twscs	2.0	-3.0	-93V	ns	10 = 30 V Latertary y fodus neve	
Chip Select Hold Time After Write	tWHCS	2.0	-3.0		ns	to + 55V) squiteV might see	
Write Disable Time	tws	2.5	5.0	7.5	ns	utnut Special Currient - Constitueous	
Write Recovery Time	twR	2.5	5.0	7.5	ns	6010E -	
Rise and Fall Time	39		81			Measured between 20% and 80% points.	
Output Rise and Fall Time	tr, tf	1.5	3.0	5.0	ns	anne 18 on stanger on T. sounds	
Capacitance	Line						
Input Capacitance	Cin	BUSTER BAR	4.0	5.0	pF	DEED IT succes from against prevent if ABSC	
Output Capacitance	Cout	_	7.0	8.0	pF	100	

Notes: (1) Contact your Motorola Sales Representative for details if extended temperature operation is desired.

- (2) The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
- (3) For proper use of MECL Memories in a system environment, consult: "MECL System Design Handbook."

FIGURE 1 — SWITCHING TIME TEST CIRCUIT



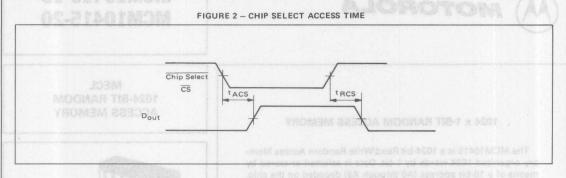


FIGURE 3 - ADDRESS ACCESS TIME

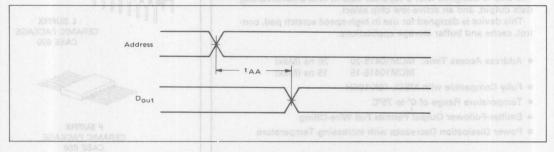
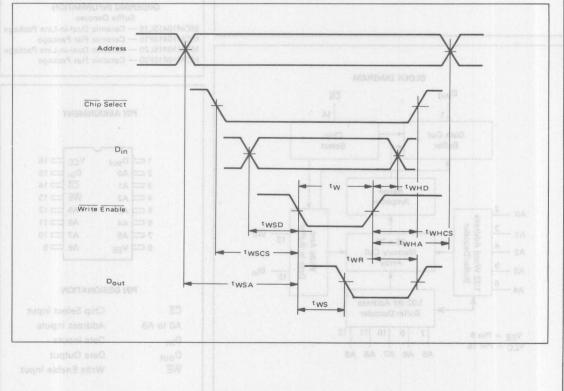


FIGURE 4 - WRITE MODE





MCM10415-15 MCM10415-20

MECL 1024-BIT RANDOM

ACCESS MEMORY



L SUFFIX CERAMIC PACKAGE **CASE 620**



F SUFFIX CERAMIC PACKAGE CASE 650

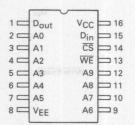
ORDERING INFORMATION

Suffix Denotes

MCM10415L15 — Ceramic Dual-in-Line Package MCM10415F15 — Ceramic Flat Package MCM10415L20 — Ceramic Dual-in-Line Package

MCM10415F20 — Ceramic Flat Package

PIN ASSIGNMENT



PIN DESIGNATION

CS	Chip Select Input
A0 to A9	Address Inputs
Din	Data Inputs
Dout	Data Output
WE	Write Enable Input

. 1024 x 1-BIT RANDOM ACCESS MEMORY

The MCM10415 is a 1024-bit Read/Write Random Access Memory organized 1024 words by 1 bit. Data is selected or stored by means of a 10-bit address (A0 through A9) decoded on the chip. The chip is designed with a separate data in line, a noninverting data output, and an active-low chip select.

This device is designed for use in high-speed scratch pad, control, cache and buffer storage applications.

• Address Access Time: MCM10415-20

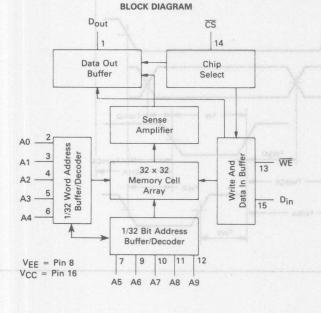
20 ns (Max) MCM10415-15 15 ns (Max)

Fully Compatible with MECL 10K/10KH

• Temperature Range of 0° to 75°C

• Emitter-Follower Output Permits Full Wire-ORing

• Power Dissipation Decreases with Increasing Temperature



5

FUNCTIONAL DESCRIPTION:

This device is a 1024 x 1-bit RAM. Bit selection is achieved by means of a 10-bit address, A0 to A9.

The active-low chip select is provided for memory expansion up to 2048 words.

The operating mode of the RAM (CS input low) is controlled by the \overline{WE} input. With \overline{WE} low, the chip is in the write mode, the output, D_{out} , is low and the data state present at D_{in} is stored at the selected address. With \overline{WE} high, the chip is in the read mode and the data stored at the selected memory location will be presented noninverted at D_{out} . (See Truth Table)

TRUTH TABLE

MODE		OUTPUT		
20A	CS	WE	Din	Dout
Write "0"	L	ankir y	seg-La	netez L ico
Write "1"	L	L 9/	Heat	A neglect A
Read	L	Н	φ	Q
Disabled	Н	φ	φ	way Pala

 $\phi = Don't Care.$

ABSOLUTE MAXIMUM RATINGS

Co-dinor Rating The William	Symbol	Value	Unit
Power Supply Voltage (V _{CC} = 0)	VEE	-8 to 0	Vdc
Base Input Voltage (V _{CC} = 0)	-Vin	0 to VEE	Vdc
Output Source Current — Continuous — Surge	- lo 0.5	<50 <100	mAdc
Junction Operating Temperature	TJ	<165	°C
Storage Temperature Range	T _{stg}	-55 to +150	°C

arugai isabbil	most revisib r	DC TE	ST VOLTAGE \ (Volts)	/ALUES	11.01
Test Temperature	VIHmax	V _{ILmin}	VIHAmin	VILAmax	VEE
0°C	-0.840	- 1.870	0.6-1.145	-1.490	- 5.2
+ 25°C	-0.810	- 1.850	-1.105	- 1.475	- 5.2
+ 75°C	-0.720	-1.830	-1.045	- 1.450	-5.2

ELECTRICAL CHARACTERISTICS

Each MECL Memory circuit has been designed to meet the dc and ac specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

	3.45	MCM10415 Test Limits							D DANKERT	
		0°C		+25°C		+75°C			ocwa .	
DC Characteristics	Symbol	Min	Max	Min	Max	Min	Max	Unit	Conditions	
Power Supply Drain Current	IEE	-	150	-	145	-	125	mAdc	Typ IEE @ 25°C = 100 mA All outputs and inputs open Measure Pin 8.	
Input Current High	linH	J41 <u>/11</u>	220	V e.c	220	-	220	μAdc	Test one input at a time, all other inputs are open. Vin = VIH.	
Input Current Low (CS only) Input Curent Low (All Others)	linL	0.5 - 50	J+T	0.5 - 50	_	0.3 -50	-	μAdc	Test one input at a time, all other inputs are open. $V_{in} \ = \ V_{IL}.$	
Logic "1" Output Voltage	Vон	- 1.000	-0.840	-0.960	-0.810	-0.900	-0.720	Vdc	Load 50 Ω to -2.0 V	
Logic "0" ed bluedê ye Output Voltage	VOL	-1.870	- 1.665	- 1.850	- 1.650	-1.830	- 1.625	Vdc		
Logic "1" Threshold Voltage	VOHA	-1.020	-	-0.980	_	-0.920	-	Vdc	Threshold testing is performed and guaranteed on one input at a time. Vin = VIHA or VILA. Load 50 Ω to -2.0 V.	
Logic "0" Threshold Voltage	VOLA	-	- 1.645		-1.630	- v	- 1.605	Vdc		

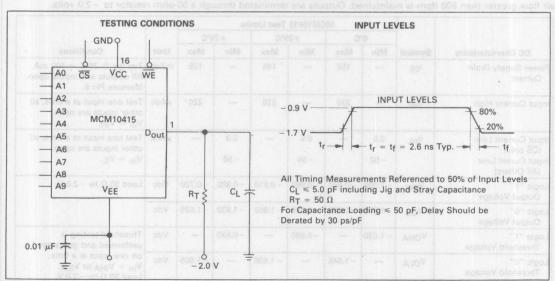
Guaranteed with $V_{FF} = -5.2 \text{ Vdc} \pm 5.0\%$, $T_{A} = 0^{\circ}\text{C}$ to 75°C (see Note 1). Output Load see Figure 1.

			MCM1	0415-20	MCM1	0415-15		SAMPHINA POR LACADOR MAIS
Characteristic		Symbol	Min	Max	Min	Max	Unit	Conditions
Read Mode		BODWI	F-Sale	138		eA or I	iA ,ea	See Figures 2 and 3.
Chip Select Access Time		tACS	-	8.0	VENE	7.0	ns	Measured at 50% of input to 50% of output.
Chip Select Recovery Time		tRCS	_	8.0	24-1V	7.0	ns	See Note 2.
Address Access Time		tAA	_	20	n i a i e	15	ns	ntrolled by the WE input. With W
Write Mode		book			desa	ed) bas	avrol 6	See Figure 4.
Write Pulse Width		tw	14	_	12	108 081	ns	twsA = 3.0 ns — MCM10415-20
(To guarantee writing)					SIBD	mir bna	BERTH	twsA = 2.0 ns - MCM10415-15
					-670	ard Illian	nones	Measured at 50% of input to 50% of
				14 15 1		, (eld	all mu	output.
Data Setup Time Prior to Wr	ite	tWSD	3.0	-	2.0	-	ns	EDWITAR MUNICAM STUDIES
Data Hold Time After Write		tWHD	3.0	_	1.0	-	ns	
Address Setup Time Prior to	Write	tWSA	3.0	eds v	2.0	di yen	ns	$t_W = 14 \text{ ns} - MCM10415-20$
Addison Hold Time Africa March		aby.	3.0	37.8-	10	aV .		tw = 12 ns — MCM10415-15
Address Hold Time After Wr		tWHA		-	1.0	100	ns	
Chip Select Setup Time Prior		twscs	3.0	((L)	2.0	iV-	ns	lasa Input Voltage (VCC = 0)
Chip Select Hold Time After	Write	twhcs	3.0	Han -	1.0	01-	ns	Jugur Scurce Carrent — Cominuous
Write Disable Time		tws	-	8.0	-	7.0	ns	agiu8
Write Recovery Time		twR	_	8.0	_	7.0	ns	
Rise and Fall Time		3	084	55 10				Measured between 20% and 80%
		-	Exten	AND DEL		100	1	points.
Output Rise and Fall Time		tr, tf	1.5	4.0	1.5	4.0	ns	When driven from CS or WE inputs.
Output Rise and Fall Time		tr, tf	1.5	8.0	1.5	8.0	ns	When driven from Address inputs.
Capacitance					1833	(45)		Measured with a pulse technique.
								See Note 4.
Input Lead Capacitance		Cin	3082	5.0	simi	5.0	pF	Temperature Villiana Va
Output Lead Capacitance				8.0	145	8.0	pF	- 0889- 30
Output Lead Capacitance		Cout		0.0	271	0.0	br	The state of the s

Notes:

- (1) Contact your Motorola Sales Representative for details if extended temperature operation is desired.
- (2) The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
- (3) For proper use of MECL Memories in a System environment, consult: "MECL System Design Handbook."
- (4) Typical ratings are 3.0 pF for Cin and 5.0 pF for Cout-

FIGURE 1 — SWITCHING TEST CIRCUIT AND WAVEFORMS



5

256 x 4-BIT RANDOM ACCESS MEMORY

The MCM10422 is a high-speed 1024-bit Read/Write RAM organized 256 words by 4 bits, designed for high speed scratch pad, control, cache, and buffer storage applications. Four independent active-low Block Selects permit use in 1024 x 1 and 512 x 2-bit applications. It has full address decoding on chip, separate data inputs, noninverting data outputs, and an active-low Write Enable.

- Address Access Time:
 MCM10422L15 15 ns (Max)
 MCM10422L10 10 ns (Max)
- Polyimide Die Protection
- Fully Compatible with MECL 10K and 10KH
- Operating Temperature Range 0°C to 75°C
- Four Independent Block Selects
- Emitter-Follower Outputs Permits Full Wire-OR'ing
- Standard 24-Pin, 400 Mil Wide, Dual In-Line Package

MECLATARINO SO

256 x 4-BIT RANDOM ACCESS MEMORY



CERAMIC PACKAGE CASE 797-01

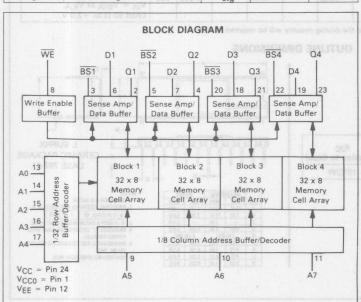
ORDERING INFORMATION

Suffix Denotes

MCM10422L10 — Ceramic Dual-in-Line Package MCM10422L15 — Ceramic Dual-in-Line Package

ABSOLUTE MAXIMUM RATINGS

ABSOLUTE WIAKIIVIUW KATII	103	4 73	90	300	
V 0.5 - Rating back	bbV	027.0	Symbol	Value	Unit
Power Supply Voltage ($V_{CC} = 0$)			VEE	-8 to 0	Vdc
Base Input Voltage ($V_{CC} = 0$)	shy	888.1	Vin	0 to VEE	Vdc
Output Source Current	other d	-	10	< 50	mAdo
Junction Operating Temperature			TJ	< 165	°C
Storage Temperature Range	State	208.1	T _{sta}	-65 to +150	°C



PIN ASSIGNMENT VCC = 24 1 = 7 VCCO 04 = 23 2 - 01 BS4 = 22 3 - BS1 4 - 02 03 - 21 BS3 ___ 20 5 - BS2 6 C D1 D4 19 7 D2 D3 18 A4 - 17 8 WE A3 16 9 A5 10 A6 A2 15 11 A7 A1 14 12 T VEE A0 13 PIN DESIGNATION

BS1	_	BS4	Block Select Inputs
A0	-	A7	Address Inputs
101	Din		Data Inputs
pl.3	Qout		Data Outputs
	WE		Write Enable Input

TRUTH TABLE

MODE		INPUT						
	BSn	WE	Din	Qout				
Write "0"	L	L	L	L				
Write "1"	L	L	Н	L				
Read	L	Н	φ	Q				
Block Disabled	н	φ	φ	L				

FUNCTIONAL DESCRIPTION:

This device is a 256 x 4-bit RAM. Word selection is achieved by means of an 8-bit address, A0-A7.

The operating mode of each block (\overline{BS}_n input low) is controlled by the \overline{WE} input. With \overline{WE} low, the block is in the write mode, the output Ω_{out} is low and the data state present at D_{jn} is stored at the selected address in block n. With \overline{WE} high, the block is in the read mode and the data stored at the selected memory location will be presented non-inverted at Ω_{out} .

The independent, active-low Block Selects and the wire-OR capability of the emitter-follower outputs permit use as a 1024 x 1 or 512 x 2-bit RAM. For example, for use as a 1024 x 1-bit RAM tie all D_{in} inputs together to form a single D_{in} , wire-OR the Q_{out} lines together to form a single Q_{out} line, and drive the Block Selects with a 1-of-4 low decoder.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Test Temperature		DC TES	(Volts)	ALUES	to high a
	ViHmax	V _{ILmin}	VIHAmin	VILAmax	VEE
0°C	- 0.840	- 1.870	- 1.145	-1.490	-5.2
+ 25°C	-0.810	- 1.850	- 1.105	- 1.475	-5.2
+75°C	- 0.720	- 1.830	- 1.045	- 1.450	- 5.2

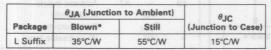
ELECTRICAL CHARACTERISTICS

Each MECL Memory circuit has been designed to meet the dc and ac specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

	dimen		MC	M10422	Test Lim	its				
		0°C		+25°C		+75°C		110	Polysonide Die Protesti	
DC Characteristics	Symbol	Min	Max	Min	Max	Min	Max	Unit	Conditions	
Power Supply Drain Current	IEE		200	-	195	-	185	mAdc	All outputs and inputs open. Measure Pin 12.	
Input Current High	linH	-	220	- 0	220	en <u>V</u> II. soiJ-pla	220	μAdc	Test one input at a time, all other inputs are open. Vin = VIH(max)	
Input Current Low (Block Selects)	linL	0.5		0.5		0.5		μAdc	Test one input at a time, all other inputs are open.	
Input Current Low*	linL	-50	_	-50	_	- 50	-	μAdc	Vin = VIL(min)	
Logic "1" Output Voltage	VOH	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	Vdc	Load 50 Ω to -2.0 V	
Logic "0" Output Voltage	VOL	-1.870	-1.665	- 1.850	- 1.650	- 1.830	- 1.625	Vdc	(b = 30x) albuyan andur	
Logic "1" Threshold Voltage	Vона	-1.020	7	-0.980		-0.920	-	Vdc	Threshold testing is performed and guaranteed	
Logic "0" Threshold Voltage	VOLA		-1.645	021 -	-1.630	<u>-</u> ₹	- 1.605	Vdc	on one input at a time. $V_{in} = V_{IHA}$ or V_{ILA} . Load 50 Ω to -2.0 V.	

*Minimum limit equals the maximum negative current the driving circuitry will be required to sink.

OUTLINE DIMENSIONS



*500 linear ft. per minute blown air.

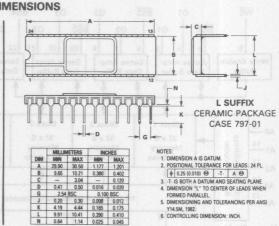
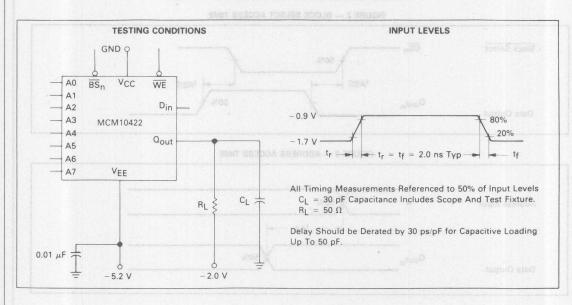


FIGURE 1 — SWITCHING TEST CIRCUIT AND WAVEFORMS



AC OPERATING CONDITIONS AND CHARACTERISTICS

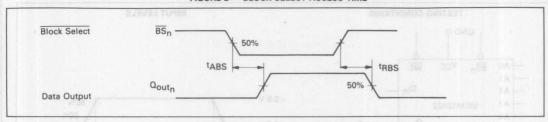
Guaranteed with V_{FF} = -5.2 Vdc $\pm 5.0\%$, T_A = 0°C to 75°C (see Note 1). Output Load see Figure 1.

		MCM1	0422L15	MCM1	0422L10			
Characteristic	Symbol	Min	Max	Min	Max	Unit	Conditions	
Read Mode					Description of the last	Name	See Figures 2 and 3.	
Block Select Access Time	tABS	_	6.0	_	5.0	ns	Measured at 50% of input	
Block Select Recovery Time	tRBS	_	6.0	_	5.0	ns	to 50% of output.	
Address Access Time	tAA	_	15	-	10	ns	See Note 1.	
Write Mode					1		See Figure 4.	
Write Pulse Width	tw	10	_	7.0	_	ns	twsA = 2.0 ns MCM10422L15	
(To guarantee writing)	and the second			200000			twsA = 1.0 ns MCM10422L10	
				W			Measured at 50% of input	
							to 50% of output.	
Data Setup Time Prior to Write	twsp	1.0		1.0	-	ns	to 50 % of output.	
Data Hold Time After Write	twhD	4.0	_	2.0	_	ns		
Address Setup Time Prior to Write	twsa	2.0	_	1.0	_	ns	tw = 10 ns MCM10422L15	
	,,,,,	19					tw = 7.0 ns MCM10422L10	
Address Hold Time After Write	twha	3.0		2.0		ns	tw = 7.0 iis ivicivi 10422L10	
Block Select Setup Time Prior to Write	twsss	2.0	_	1.0		ns		
Block Select Hold Time After Write	twhes	3.0	G214/7 -	2.0		ns		
Write Disable Time	tws	_	5.0	_	5.0	ns		
Write Recovery Time	twR	jour	9.0	8W 4	9.0	ns		
Rise and Fall Time	7***	Annual I	TYP	ICAL			Measured between 20% and 80%	
Output Rise and Fall Time	tr, tf	1	2	.0		ns	points.	
Capacitance	ed l		TYP	ICAL			Measured with a pulse technique	
Input Lead Capacitance	Cin	VI In	5	.0		pF		
Output Lead Capacitance	Cout			.0		pF		

Notes:

- (1) The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
- (2) For proper use of MECL Memories in a system environment, consult: "MECL System Design Handbook."

FIGURE 2 — BLOCK SELECT ACCESS TIME



er I an 0.2 and FIGURE 3 — ADDRESS ACCESS TIME

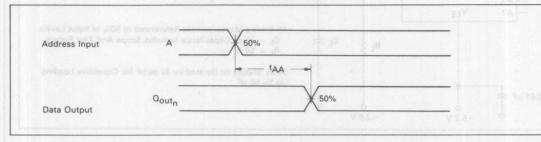
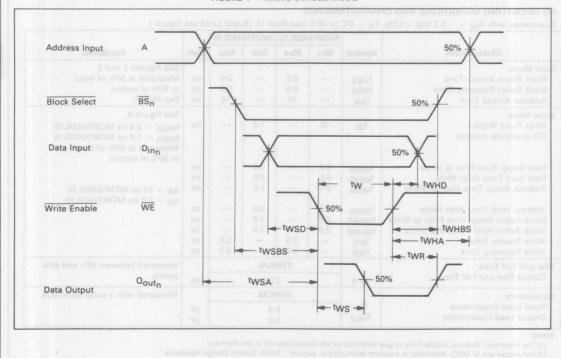


FIGURE 4 — WRITE STROBE MODE



5



Advance Information

4096 x 1-BIT RANDOM ACCESS MEMORY

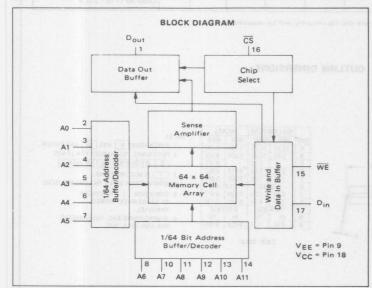
The MCM10470 is a 4096-bit Read/Write RAM organized for 4096 words by 1 bit. Data is selected or stored by means of a 12-bit address (A0 through A11) decoded on the chip. The chip is designed with a separate data-in line, a noninverting data output, and an active-low chip select.

This device is designed for use in high-speed scratch pad, control, cache and buffer storage applications.

- Fully Compatible with MECL 10K/10KH
- Pin-for-Pin Compatible with the Industry's Standard 10470
- Temperature Range of 0° to 75°C
- Emitter-Follower Output Permits Full Wire-ORing
- Power Dissipation Decreases with Increasing Temperature
- Address Access Time: MCM10470*25 25 ns (Max)
 MCM10470*15 15 ns (Max)

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (V _{CC} = 0)	VEE	-8.0 to 0	Vdc
Base Input Voltage (V _{CC} = 0)	Vin	0 to VEE	Vdc
Output Source Current	10	-30	mAdc
Junction Operating Temperature	TJ	≤ 165	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C



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This document contains information on a new product Specifications and information herein are subject to change without notice.

MCM10470*15 MCM10470*25

MECL

4096 x 1-BIT RANDOM ACCESS MEMORY

F SUFFIX CERAMIC PACKAGE CASE 747-01





L SUFFIX CERAMIC PACKAGE CASE 680-06

ORDERING INFORMATION

Suffix Denotes

- *MCM10470L15—Ceramic Dual-in-Line Package
- *MCM10470F15—Ceramic Flat Package
- *MCM10470L25—Ceramic Dual-in-Line Package
 *MCM10470F25—Ceramic Flat Package

PIN ASSIGNMENT

	A CONTRACTOR OF THE PARTY OF TH	- A - A - A - A - A - A - A - A - A - A	
1 =	Dout	VCC	18
2 =	A0	Din	17
3 =	A1	CS	16
4 ==	A2	WE	15
5 =	A3	A11	14
6 =	A4	A10	= 13
7 ==	A5	A9	- 12
8 =	A6	A8	= 11
9 =	VEE	A7	1 0

PIN DESIGNATION

CS Chip Select

A0-A11 Address Inputs

WE Write Enable

D_{in} Data Input

Dout Data Output

TRUTH TABLE

MODE		INPUT		OUTPUT
	CS	WE	Din	Dout
Write "0"	L	L	L	-)L
Write "1"	L	L	н	L
Read	L	н	φ	Q
Disabled	н	φ	Φ	L

The active-low chip select is provided for memory expansion. The operating mode of the RAM ($\overline{\text{CS}}$ input low) is controlled by the $\overline{\text{WE}}$ input. With $\overline{\text{WE}}$ low, the chip is in the write mode, the output, Ω_{out} , is low and the data state present at D_{in} is stored at the selected address. With $\overline{\text{WE}}$ high, the chip is in the read mode and the data stored at the selected memory location will be presented noninverted at Ω_{out} . (See Truth Table)

DC OPERATING CONDITIONS AND CHARACTERISTICS

	A ACCEDS A	DC TES	VALUES		
Test Temperature	VIHmax	VILmin	VIHAmin	VILAmax	VEE
0°C	-0.840	-1.870	-1.145	-1.490	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+75°C	-0.720	-1.830	-1.045	-1.450	-5.2

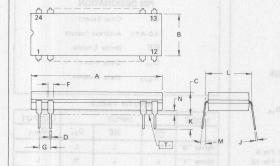
ELECTRICAL CHARACTERISTICS

Each MECL Memory circuit has been designed to meet the dc and ac specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

				MCM10474	Test Limit	S			Little companios vilias e
		00	C	+2	5°C	+75	5°C		* Pin-for-Pin Compatible
DC Characteristics	Symbol	Min	Max	Min	Max	Min	Max	Unit	Conditions
Power Supply Drain Current	IEE		200		195	AO any	185	mAdc	All outputs and inputs open.
				974	taraqma	easing	ioni rilita		Measure Pin 12.
Input Current High	linH		220		220	25 (10	220	μAdc	Test one input at a time, all
	HE11016	et es gare			pade	an al	8170116		other inputs are open. Vin VIH(max)-
Input Current Low Chip Select	linL	0.5		0.5		0.3		µАdc	Test one input at a time, all other inputs are open.
Input Current Low*	linL	-50		-50		-50		μAdc	V _{in} V _{IL} (min).
Logic ''1'' Output Voltage	Voн	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	Vdc	Load 50 11 to -2.0 V
Logic ''0'' Output Voltage	VOL	-1.870	-1.665	-1.850	-1.650	-1.830	-1.625	Vdc	(0 - pgV) spulav tuam
Logic ''1'' Threshold Voltage	Vона	-1.020		-0.980	881 a	-0.920		Vdc	Threshold testing is performed and guaranteed on one input at
Logic ''0'' Threshold Voltage	VOLA		-1.645	ja / 13	-1.630	[3]p	-1.605	Vdc	a time. V _{IN} V _{IHA} or V _{ILA} . Load 50 Ω to -2.0 V.

* Minimum limit equals the maximum negative current the driving circuitry will be required to sink and 3000 in

OUTLINE DIMENSIONS



	MILLIM	ETERS	INCHES				
DIM	MIN	MAX	MIN	MAX			
Α	29.21	31.75	1.150	1.250			
В	9.40	10.16	0.370	0.400			
C	- 20	5.72		0 225			
D	0.38	0.56	0.015	0.022			
F	1.27	1.65	0.050	0.065			
G	2.5	BSC	0.10	BSC			
J	0.20	0.30	0.008	0.012			
K	2.54	4.32	0.100	0.170			
L	10.16	BSC	0.40	BSC			
M	00	150	00	150			
N	0.51	1.27	0.020	0.050			

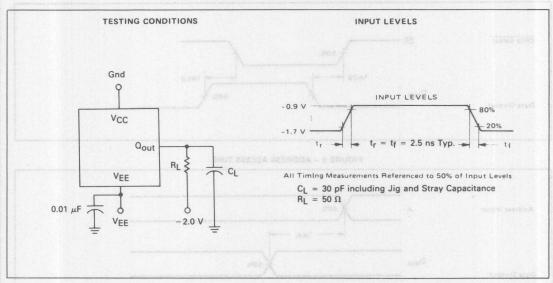
CASE 748-01

NOTEC

- 1. DIMENSIONS A AND B ARE DATUM.
- 2. POSITIONAL TOLERANCES FOR LEADS:

 (b) Ø 0.25 (0.010) 🔞 T A 🔞 B 🔞
- 3. T. IS SEATING PLANE.
 4. DIMENSIONS A AND B INCLUDE MENISCUS.
- 5. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
- 6. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

5



AC OPERATING CONDITIONS AND CHARACTERISTICS

Guaranteed with VEE = -5.2 Vdc ± 5.0%, TA = 0°C to 75°C (see Note 1). Output Load see Figure 1.

	eranco sens	MCM10	470*25	MCM10	470*15			
Characteristic	Symbol	Min	Max	Min	Max	Unit	Conditions	
Read Mode						1	See Figures 2 and 3.	
							Measured at 50% of input to 50% o	
Chip Select Access Time	tACS	-	10	_	8.0	ns	output.	
Chip Select Recovery Time	tRCS	-	10	_	8.0	ns		
Address Access Time	tAA	-	25	_	15	ns	Taine gard	
Write Mode						VSI	See Figure 4.	
Write Pulse Width	tw	25	_	15	-	ns	tWSA = 3.0 ns MCM10470*25	
(To guarantee writing)		-			Contract of		tWSA = 3.0 ns MCM10470*15	
				100			Measured at 50% of input to 50%	
Data Setup Time Prior to Write	twsp	5.0	-	2.0	-	ns	of output.	
Data Hold Time After Write	tWHD	5.0	-	2.0	Andrew Comments	ns	tw = 25 ns MCM10470*25	
Address Setup Time Prior to Write	tWSA	8.0	-	3.0	_	ns	tw = 15 ns MCM10470*15	
Address Hold Time After Write	tWHA	5.0	-	2.0		ns		
Chip Select Setup Time Prior to Write	twscs	5.0	1	2.0	-	ns		
Chip Select Hold Time After Write	tWHCS	5.0	-	2.0	- 1	ns	alizenzi se est	
Write Disable Time	tws	-	10	-	8.0	ns		
Write Recovery Time	twR	-	15	1 1 1 2 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	8.0	ns		
Rise and Fall Time			Тур	ical			Measured between 20% and 80%	
Output Rise and Fall Time	tr, tf		2	.5		ns	points.	
Capacitance	F. J. C.	/	Тур	ical			Measured with a pulse technique.	
Input Lead Capacitance	Cin		4	.0	evi?	pF	Supplement Dank	
Output Lead Capacitance	Cout			.0		pF		

Notes:

- (1) The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
- (2) For proper use of MECL Memories in a system environment, consult: "MECL System Design Handbook."

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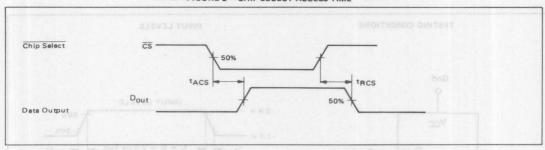


FIGURE 3 - ADDRESS ACCESS TIME

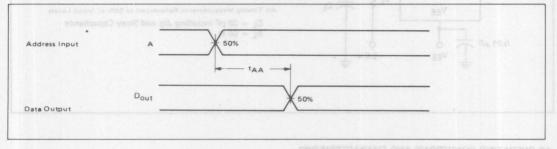
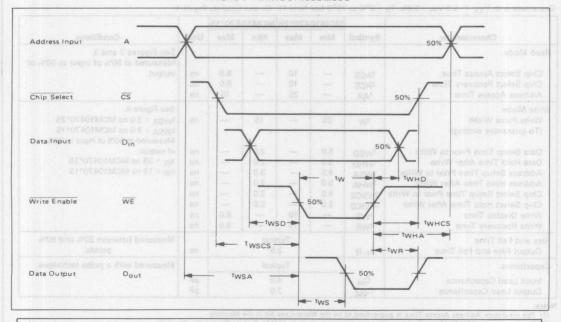


FIGURE 4 - WRITE STROBE MODE



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MCM10474*15 MCM10474*25

Advance Information

1024 x 4-BIT RANDOM ACCESS MEMORY

The MCM10474 is a 4096-bit Read/Write RAM organized for 1024 words by 4 bits. Data is selected or stored by means of a 10-bit address (A0 through A9) decoded on the chip. The chip is designed with 4 separate data-in lines, 4 noninverting data outputs, and an active-low chip select.

This device is designed for use in high-speed scratch pad, control, cache and buffer storage applications.

- Fully Compatible with MECL 10K/10KH
- Pin-for-Pin Compatible with the Industry's Standard 10474
- Temperature Range of 0° to 75°C
- Emitter-Follower Output Permits Full Wire-ORing
- Power Dissipation Decreases with Increasing Temperature
- Address Access Time:

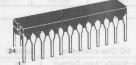
MCM10474*25 25 ns (Max) MCM10474*15 15 ns (Max)

• Chip Select Access Time: MCM10474*25 10 ns (Max) MCM10474*15 8.0 ns (Max)

MECI

1024 x 4 BIT RANDOM ACCESS MEMORY

> L SUFFIX CERAMIC PACKAGE CASE 748-01



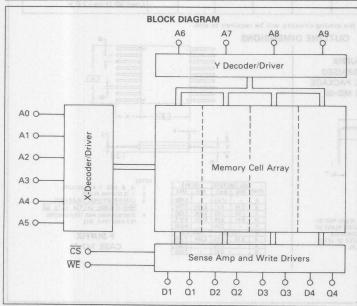
ORDERING INFORMATION

Suffix Denotes

*MCM10474L15—Ceramic Dual-in-Line Package *MCM10474L25—Ceramic Dual-in-Line Package

ARSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (V _{CC} = 0)	VEE	-8.0 to 0	Vdc
Base Input Voltage (V _{CC} = 0)	V _{in}	0 to VEE	Vdc
Output Source Current	10	<50	mAdo
Junction Operating Temperature	TJ	≤ 165	°C
Storage Temperature Range	T _{stq}	-65 to +150	°C



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This document contains information on a new product. Specifications and information herein are subject to change without notice.

5-49

PIN ASSIGNMENT Vcco VCC 24 2 _ 03 02 7 23 3 ⊏ 04 01 □ 22 4 AO D4 ⊐ 21 5 A1 D3 □ 20 6 A2 D2 ____ 19 7 A3 D1 CS **17** 8 A4 9 A5 WE □ 16 10 - NC □ 15 A9

PIN DESIGNATION

14

□ 13

A8

A7

11 A6

12 VEE

CS Chip Select
A0-A9 Address Inputs

WE Write Enable

Din Data Input

Qout Data Output

TRUTH TABLE

MODE		OUTPUT		
STAB NUMERA L POSNEM	CS	WE	Din	Dout
Write "0"	L	L	L	L
Write "1"	L	L	н	L
Read	L	Н	Φ	DO
Disabled	н	0	0	L

FUNCTIONAL DESCRIPTION:

This device is a 4096×1 -bit RAM. Bit selection is achieved by means of a 12-bit address, A0 to A11.

The active-low chip select is provided for memory expansion.

The operating mode of the RAM (CS input low) is controlled by the WE input. With WE low, the chip is in the write mode, the output, Dout, is low and the data state present at Din is stored at the selected address. With WE high, the chip is in the read mode and the data stored at the selected memory location will be presented non-inverted at Dout. (See Truth Table)

DC OPERATING CONDITIONS AND CHARACTERISTICS

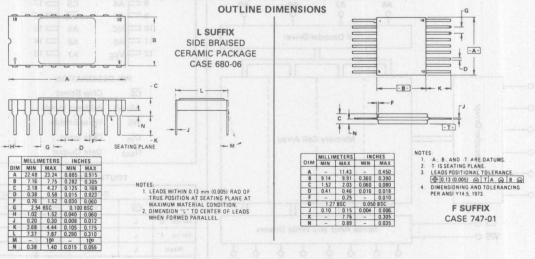
	DC TEST VOLTAGE VALUES (Volts)								
Test Temperature	VIHmax	VILmin	VIHAmin	VILAmax	VEE				
0°C	-0.840	-1.870	-1.145	-1.490	-5.2				
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2				
+75°C	-0.720	-1.830	-1.045	-1.450	-5.2				

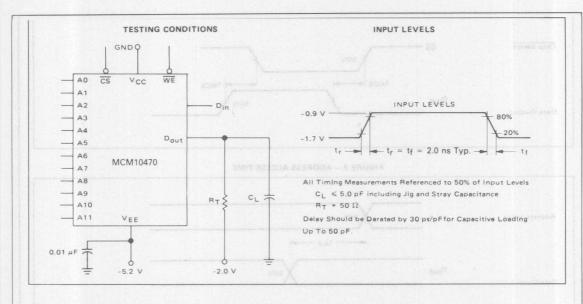
ELECTRICAL CHARACTERISTICS

Each MECL Memory circuit has been designed to meet the dc and ac specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 Ifpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

			M	ICM10470	Test Lim	its	Honi sai	LESSIN S	网络岛屿市岛区 的第三国际主席 華	
		0°C		+25°C		+75°C		of 10.1	* Temperature Bange d	
DC Characteristics	Symbol	Min	Max	Min	Max	Min /	Max	Unit	Conditions	
Power Supply Drain Current MCM10470 MCM10470A	lee 3080	=	205 205	<u>e</u> Tyte	200 200	crea <u>s</u> ing 28-25	190 190	mAdc	All outputs and inputs open. Measure Pin 9.	
Input Current High	linH so	MONA" DADRA"	220	-	220	15_16 25_16 15_8.0	220	μAdc	Test one input at a time, all other inputs are open. Vin = VIH(max).	
Input Current Low Chip Select	linL	0.5		0.5	-	0.3	-	μAdc	Test one input at a time, all other inputs are open.	
Input Current Low*	linL	-50	-	-50	and the	-50		μAdc	Vin = VIL(min).	
Logic "1" Output Voltage	VOH	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	Vdc	Load 50 Ω to -2.0 V	
Logic "O" Output Voltage	VOL	-1.870	-1.665	-1.850	-1.650	-1.830	-1.625	Vdc	(D = 25V) egallo Vatati e	
Logic "1" Threshold Voltage	VOHA	-1.020	7.0	-0.980	88T a	-0.920		Vdc	Threshold testing is performed and guaranteed on one input at	
Logic "0" Threshold Voltage	VOLA	-	-1.645	-[03	-1.630	- 82	-1.605	Vdc	a time. $V_{in} = V_{iHA}$ or V_{iLA} . Load 50 Ω to -2.0 V .	

* Minimum limit equals the maximum negative current the driving circuitry will be required to sink.





AC OPERATING CONDITIONS AND CHARACTERISTICS

Guaranteed with $V_{FF} = -5.2 \text{ Vdc} \pm 5.0\%$, $T_A = 0^{\circ}\text{C}$ (see Note 1). Output Load see Figure 1.

		MCM10	0474*25	MCM10	474*15			
Characteristic	Symbol	Min	Max	Min	Max	Unit	Conditions	
Read Mode							See Figures 2 and 3.	
Chip Select Access Time	tACS	_	10	_	8.0	ns	Measured at 50% of input to 50%	
Chip Select Recovery Time	tRCS	-	10	-	8.0	ns	of output.	
Address Access Time	tAA	-	25		15	ns	See Note 2.	
Write Mode		The Park	ET LET	3 × 1	4		See Figure 4.	
Write Pulse Width	tw	25	-	15	-	ns	twsa = 8.0 ns MCM10474*25	
(To guarantee writing)					1		tWSA = 3.0 ns MCM10474*15	
			E-4 To		A		Measured at 50% of input to 50%	
		-	-		and i		of output.	
Data Setup Time Prior to Write	tWSD	2.0	-	2.0 —		ns	t _W = 25 ns MCM10474*25	
Data Hold Time After Write	tWHD	2.0	-	2.0	_	ns	t _W = 15 ns MCM10474*15	
Address Setup Time Prior to Write	tWSA	3.0	-	3.0	-	ns	and the second	
Address Hold Time After Write	tWHA	2.0	_	2.0	-	ns		
Chip Select Setup Time Prior to Write	twscs	2.0	-	2.0	_	ns		
Chip Select Hold Time After Write	twhcs	2.0	-	2.0	-	ns		
Write Disable Time	tws		10	-	8.0	ns	NAME OF THE PARTY	
Write Recovery Time	tWR	-	10	_	8.0	ns		
Rise and Fall Time	None		Тур	oical			Measured between 20% and 80%	
Output Rise and Fall Time	t _r , t _f		2	.0		ns	points.	
Capacitance		processor	Тур	oical		11.14	Measured with a pulse technique.	
Input Lead Capacitance	Cin		3	.0		pF	son Control Cons	
Output Lead Capacitance	Cout			.0	eW-	pF		

- (1) Contact your Motorola Sales Representative for details if extended temperature operation is desired.
 (2) The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
- (3) For proper use of MECL Memories in a system environment, consult: "MECL System Design Handbook."

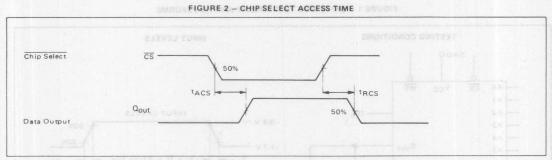
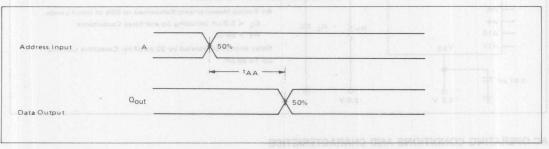
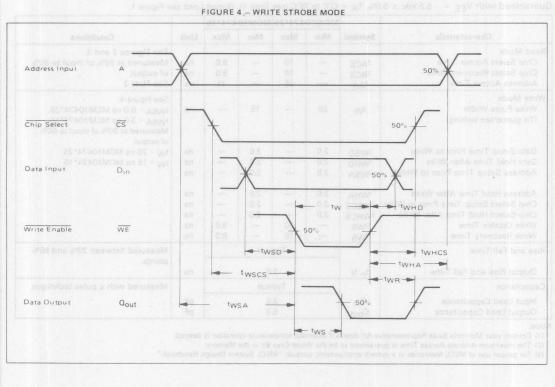
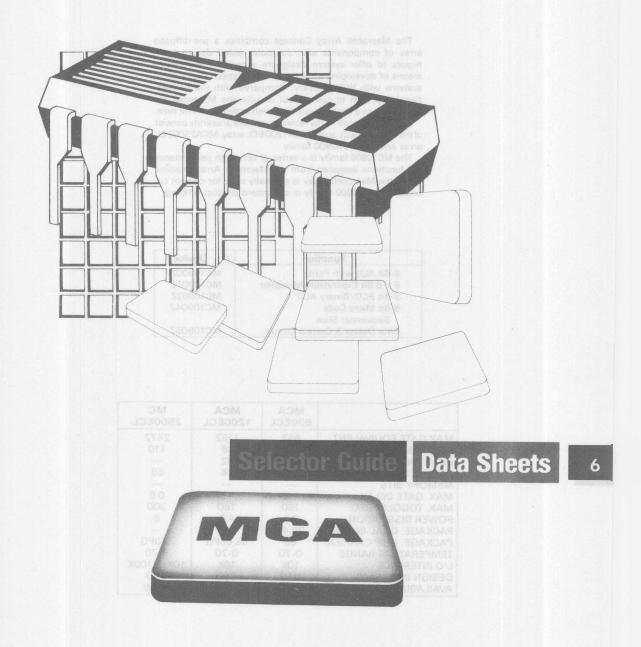


FIGURE 3 - ADDRESS ACCESS TIME





MECL Macrocell Array INTEGRATED CIRCUITS



MECL Macrocell Array INTEGRATED CIRCUITS

The Macrocell Array Concept combines a pre-diffused array of components with computer aided design techniques to offer system designers a rapid, cost-effective means of developing semi-custom high-speed digital logic systems with VLSI circuitry. Compared with the conventional approach to custom LSI circuits, the Macrocell approach offers a tremendous reduction in development time.

MECL Macrocell Array family members presently consist of the MCA600 ECL array, MCA1200 ECL array, MCA2500ECL array and the MC10900 family.

The MC10900 family is a series of very high performance LSI functions designed from the Macrocell Array product. While the Macrocell Array is normally used for custom circuits, the MC10900 family is a standard product offering.

Function	Device
8-Bit ALU with Parity	MC10900Z
8 × 8 Bit Expandable Multiplier	MC10901Z
8-Bit BCD/Binary ALU	MC10902Z
8-Bit Micro Code	MC10904Z
Sequencer Slice	
Error Detect & Correct Circuit	MC10905Z

	MCA 600ECL	MCA 1200ECL	MC 2500ECL
MAX GATE EQUIVALENT	652	1192	2472
MAJOR MACROCELLS	24	48	110
INPUT/INTERFACE CELLS	25	32	_
OUTPUT MACROCELLS	18	26	68
MEMORY BITS	_	_	
MAX. GATE DELAY	1.2	1.2	0.5
MAX. TOGGLE FREQ.	160	160	300
POWER DISSIPATION	2.2	4.0	8
PACKAGE: DUAL-IN-LINE	28,40	经验	-
PACKAGE: CHIP CARRIER	68	63,68PG	149PG
TEMPERATURE RANGE	0-70	0-70	0-70
I/O INTERFACE	10K	10K	10KH/100K
DESIGN INTERFACE	CAD	CAD	CAD
AVAILABILITY	NOW	NOW	NOW

Advance Information

8-BIT PARITY ALU SLICE

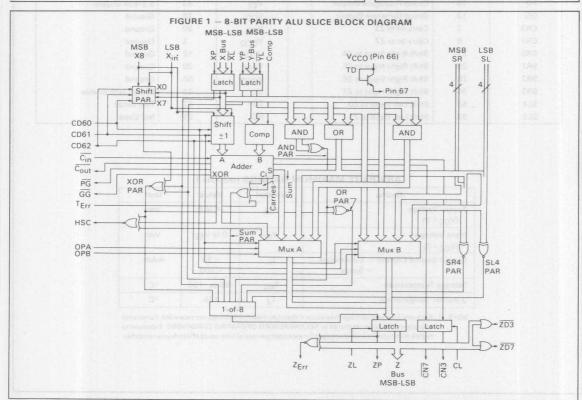
The MC10900 8-Bit Parity ALU Slice is an LSI building block for digital processors. This circuit performs the necessary logic and arithmetic functions required to execute the various machine instructions. Each part is 8-bits wide and is "sliced" parallel to data flow. The MC10900 is fully expandable to larger word lengths by connecting circuits in parallel.

The 8-Bit Parity ALU Slice as shown in the block diagram contains logic functions, shift network, arithmetic logic, input-output latches, and parity detect logic in a single bipolar circuit. Six select lines and four latch lines are used to control all operations within the part.

- Two Input Data Ports
- Internal Lookahead Carry with Propagate and Generate Outputs
- Status Outputs: Carryout, Zero Detect, Parity Error Detect, Internal Carry Signal for Overflow Detect
- Each Port Is 8-Bits Wide and the Circuit Can be Operated in Parallel to Form Any Word Size in Increments of 4 Bits.
- Single-Bit and 4-Bit Shift Operations
- The Parity Bit Is Generated with Separate Internal Logic for Each ALU Operation.

MECL-LSI 8-BIT PARITY ALU SLICE





PIN ASSIGNMENTS

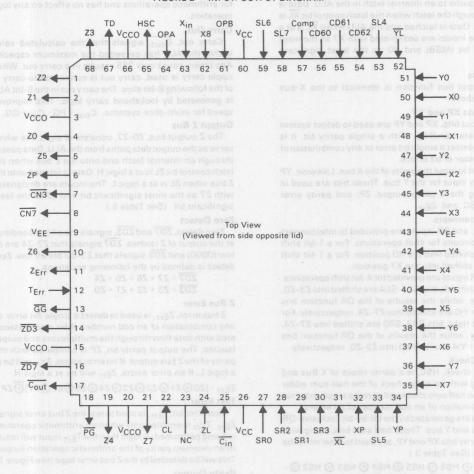
Pin Name	Pin Number	Description	Pin Name	Pin Number	Description
X0	50	Input Bus — LSB Input	SL6	59	Shift Left Input to Z2
X1	48	Input Bus	SL7	58	Shift Left Input to Z3
X2	46	Input Bus	ZO	4	Output Bus — LSB Output
X3	44	Input Bus	Z1	2	Output Bus
X4	41	Input Bus	Z2	UJA YTHRAS	Output Bus
X5	39	Input Bus	Z3	68	Output Bus
X6	37	Input Bus	Z4	19	Output Bus
X7	35	Input Bus — MSB Input	Z5	5	Output Bus
X8	62	Shift Interconnect — MSB	76	10	Output Bus
XL	31	X Latch Enable	77	21	Output Bus — MSB Output
XP	32	X Input Parity	ZD3	14 letti	Zero Detect
Xin	63	Shift Interconnect — LSB	ZD7	16	Zero Detect
YO	51	Input Bus — LSB Input	metic qZ cic. The	6	Parity Output
Y1	49	Input Bus	Lucas ZL found a	24	Z Latch Enable
Y2	47	Input Bus	ZErr	OP 01 111 915	Bus Error Detect Output
Y3	45	Input Bus	TErr	12	Test Error Detect Input
Y4	42	Input Bus	Comp	57	Control Input Complement
Y5	40	Input Bus	CD60	56	Control Input
Y6	38	Input Bus	CD61	55	Control Input
Y7	36	Input Bus — MSB Input	CD62	54	Control Input
YL	52	Y Latch Enable	Hec	65	Half Sum Check Output
YP	34	Y Input Parity	OPA	64	Control Input
Cin	25	Carry Input	OPB STE	61, 61	Control Input
Cout	17	Carry Output	VEE	9	-5.2-Volt Supply
PG	18	Group Propagate Output	VEE	43	-5.2-Volt Supply
GG	13	Group Generate Output	Vcc	26	Ground
CN3	7	Carry-In to Z3	Vcc	20	Ground
CN7	8	Carry-In to Z7	Vcco	3	Ground
SRO	27	Shift Right Input to Z4	Vcco	15	Ground
SR1	29	Shift Right Input to Z5	Vcco	20	Ground
SR2	28	Shift Right Input to Z6	Vcco	66	Ground
SR3	30	Shift Right Input to Z7	CL	22	Carry Latch Enable
SL4	53	Shift Left Input to ZO	TD	67	Test Diode
SL5	33	Shift Left Input to Z1	NC	23	Not Used

ABSOLUTE MAXIMUM BATINGS (see Note 1)

Rating	Symbol	Value	Unit
Supply Voltage (V _{CC} = 0)	VEE	-8 to 0	Vdc
Input Voltage (V _{CC} = 0)	Vin	0 to VEE	Vdc
Output Source Current — Continuous — Surge	lo	<30 <100	mAdc
Storage Temperature	T _{stg}	-55 to +150	°C
Junction Temperature	TJ	165	°C

NOTE 1. Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.





ARCHITECTURAL DESCRIPTION

The MECL LSI 8-Bit Parity ALU Slice is a member of the M10900 family utilizing the MECL 10,000 Macrocell Array. The parity ALU slice has the capability of performing logic operations and binary arithmetic on combinations of one and two variables, X Bus and Y Bus. Single- bit data paths \overline{C}_{in} , \overline{C}_{out} , X_{in} , and X8 and four-bit data paths SL and SR are used to interconnect parallel MC10900s for larger word lengths. These data bits allow for arithmetic and shift operations on larger word lengths. Group propagate and group generate outputs can be used in conjunction with external lookahead carry logic for faster system operation. Two zero detect bits signal the all low condition of bits Z7–Z4 or Z3–Z0 of the Z output bus. Carry signals generated within the

adder of the ALU, $\overline{\text{CN3}}$ and $\overline{\text{CN7}}$, are made available as outputs for determining overflow conditions. The circuit also contains two parity error signals which continuously checks data flow within the 8-bit ALU slice.

Data enters the ALU through the X Bus and Y Bus and exits through the Z bus. Each port is 9 bits wide consisting of 8 data bits, 1 odd parity bit, and a 9-bit latch. X and Y input data is routed to four logic networks which generate a 1-bit shift right or left of X, a complement of Y, a logic OR of X and Y, and a logical AND of X and Y. The adder network generates the arithmatic sum and the logical Exclusive-OR from the outputs of the shift and complement logic. Two 1-of-4 multiplexors select the data path to the Z output bus.

NOTE: All truth tables are expressed in positive logic.

6

Input X Bus

The X input bus consists of eight bits which serve as input data paths to an internal latch in the ALU. Data is passed through the latch when the latch control bit \overline{XL} is at a logic L. Data is latched into the ALU when \overline{XL} is at a logic H. The inputs are designated with X7 as the most significant bit (MSB) and X0 as the least significant bit (LSB).

Input Y Bus

The Y input bus function is identical to the X bus described above.

Parity Inputs XP and YP

Parity input bits, XP and YP are used to detect system errors in data handling. With a single parity bit, it is possible to detect a single bit error or any combination of an odd number of bit errors.

XP is used to input the parity of the X bus. Likewise, YP is the parity input for the Y bus. These bits are used in determining the Z parity output, ZP, and parity error signals, HSC and Z_{Err} .

Shift Interconnects

 X_{in} , X8, SL, and SR inputs are provided to interconnect 8-bit slice circuits for shift operations. For a 1-bit shift left, X_{in} is shifted into the X0 position. For a 1-bit shift right, X8 is shifted into the X7 position.

SL and SR inputs are provided for 4-bit shift operations. For a 4-bit shift left, bits SL7–SL4 are shifted into Z3–Z0, respectively, while the results of the OR function bits (X+Y)3-(X+Y)0 are shifted into Z7–Z4, respectively. For a 4-bit shift right, bits SR3–SR0 are shifted into Z7–Z4, respectively, while the results of the OR function bits (X+Y)7-(X+Y)4, are shifted into Z3–Z0, respectively.

Half Sum Check

Half sum check, HSC, is a parity check of X Bus and Y Bus along with an error check of the half sum adder network. The half sum check will detect a single-bit error or any combination of an odd number of bit errors.

Half sums are generated by the bit-by-bit Exclusive-OR of the X bus and Y bus. These half sum bits, along with the input parity bits XP and YP, are used to determine the error check. (See Table 3.)

 $\begin{array}{c} \mathsf{HSC} = \mathsf{HS7} \bigoplus \mathsf{HS6} \bigoplus \mathsf{HS5} \bigoplus \mathsf{HS4} \bigoplus \mathsf{HS3} \bigoplus \mathsf{HS2} \bigoplus :: \\ \mathsf{HS1} \bigoplus \mathsf{HS0} \bigoplus \mathsf{XP} \bigoplus \mathsf{YP} \bigoplus \mathsf{Shift} \; \mathsf{PAR} \end{array}$

Carry Signals

Carry Signals, $\overline{\text{CN3}}$ and $\overline{\text{CN7}}$, can be used to detect system overflow. Overflow detects when the maximum system word or byte value has been exceeded. In a system, only the overflow from the 8-bit slice operating on the most significant bits of the data word is used.

Overflow can be detected by the Exclusive-OR of the carry out and carry in of the most significant bit in a system, in an eight-bit increment system (, 16, 24, ...) overflow can be generated by the Exclusive-OR of signals $\overline{C_{out}}$ and $\overline{CN7}$:

$OF = \overline{C_{out}} \oplus \overline{CN7}$

In a four-bit increment system (4, 12, 20 . . .) overflow can be generated by the Exclusive-NOR of signals Z4 and $\overline{CN3}$: OF = $\overline{Z4}$ $\overline{\bigcirc}$ $\overline{CN3}$

Z4 is in effect the carry out of the 8-bit slice ALU operating in a 4-bit slice mode.

Carry In

Carry in, $\overline{C_{in}}$, is used to interconnect 8-bit slice circuits in a system. For ripple carry, carry in is connected to

carry out of the preceding 8-bit slice. Carry in is only used for arithmetic operations and has no effect on any logic operation.

Carry Out

Carry out, $\overline{C_{Out}}$, signals that the calculated value within the ALU has exceeded the maximum capacity. Any binary count over 255 results in a carry out. When ripple carry is used, carry out is connected to carry in of the following 8-bit slice. The carry out in the 8-bit ALU is generated by lookahead carry logic. This improves speed for multi-slice systems. $C_{Out} = PG \cdot C_{in} + GG$.

The Z output bus, ZO–Z7, consists of eight bits which serve as the output data paths from the ALU. Data passes through an internal latch and onto the Z bus when the latch control bit ZL is at a logic H. Data is latched onto the Z bus when ZL is at a logic L. The inputs are designated with Z7 as the most significant bit and ZO as the least

Zero Detect

Output Z Bus

Zero detect, $\overline{ZD7}$ and $\overline{ZD3}$, signals the all low condition at the output of Z latches. $\overline{ZD7}$ signals that Z7–Z4 are all low (0000) and $\overline{ZD3}$ signals that Z3–Z0 are all low. Zero detect is defined by the following equations:

 $\overline{ZD7}$ = Z7 + Z6 + Z5 + Z4 $\overline{ZD3}$ = Z3 + Z2 + Z1 + Z0

significant bit. (See Table 5.)

Z Bus Error

Z bus error, Z $_{Err}$, is used to detect a single-bit error or any combination of an odd number of bit errors associated with data flow through the multiplexors and output latches. The output parity bit, ZP is compared with the parity of the Z bus output. If no error exists, Z $_{Err}$ will be at a logic L. If an error exists, Z $_{Err}$ will be at a logic H.

 $Z_{Err} = [Z0 \oplus Z1 \oplus Z2 \oplus Z3 \oplus Z4 \oplus Z5 \oplus Z6 \oplus Z7] \overline{\oplus} ZP$ Test Error

Test error bit, T_{Err} , is used to test the Z bus error signal, Z_{Err} . T_{Err} is enabled only when an arithmetic operation is being performed. A logic H on the T_{Err} input will result in an incorrect parity of the arithmetic operation output. This will be detected by the Z bus error logic (see Figure 1).

Parity Output

Parity output, ZP, is used to output the parity of the Z bus. ZP is generated independently of the Z bus, which adds another level of system error check. (See Tables 2, 3, 5.)

Group Propagate and Group Generate

The group propagate, PG, and group generate, GG, outputs are used in conjuction with external lookahead carry logic for faster system operation. Using this technique, the carry in signals to the 8-bit slice circuits are generated faster than with ripple carry.

PG = P7 · P5 · P3 · P1

 $GG = G7 + P7 \cdot G5 + P7 \cdot P5 \cdot G3 + P7 \cdot P5 \cdot P3 \cdot G1$ Where $P_i = (A_i \oplus B_i) \cdot (A_{i-1} \oplus B_{i-1})$

 $G_i = A_i \cdot B_i + (A_i + B_i) \cdot (A_{i-1} \cdot B_{i-1})$ A is the output of the one-bit shifter and

B is the output of the complementer going to the adder.

(See Figure 1.)

Test Diode

A test diode, TD, is connected to Pin 67 for use in testing the junction temperature. Pin 66 is connected to the anode and Pin 67 is the cathode.

SELECT LINE OPERATION

One-Bit Shift Select

Control inputs CD60, CD61, and CD62 are used to give the MECL 8-bit slice a one-bit shift left or a one bit shift right. A logic L on CD62 results in a 1-bit shift left whereas a logic H results in a 1-bit shift right operation. When CD60 is held at a logic L or CD61 is held at a logic H, no shift operation is performed. Table 1 illustrates the 1-bit shift operation. During a SL, the Xin input is shifted into the LSB of the adder. During a SR the X8 input is shifted into the MSB of the adder.

TABLE 1

CD60	CD61	CD62	Operation
L	X	X	No Shift
×	Н	X	No Shift
Н	L	L	1 Bit Shift Left, XSL
Н	L	Н	1 Bit Shift Right, XSR

Mux B Select

Control inputs CD60, CD61, and CD62 are used to select the data path to the ALU output latch. When CD61 is held at a logic H, Mux B is enabled. CD60 and CD62 select ALU functions pass X, pass Y, shift left 4 bits or shift right 4 bits.

TABLE 2

				ZP
L	×	×	Not Enabled	See Table 3
Н	L	L	Pass X	XP
Н	L	Н	Pass Y	YP
Н	Н	L	Shift Left 4 Bits	SL4 PAR
Н	Н	н	Shift Right 4 Bits	SR4 PAR

SL4 PAR = [SL4 + SL5 + SL6 + SL7] +

 $[(X4 + Y4) \oplus (X5 + Y5) \oplus (X6 + Y6) \oplus (X7 + Y7)]$

Mux A Select

Control inputs OPA, OPB, and CD61 are used to select the data path to the ALU output latch. When CD61 is held at a logic L, Mux A is enabled, OPA and OPB select ALU functions Sum, XOR, X+Y, or X · Y (see Figure 1).

TABLE 3

CD61	OPA	ОРВ	Function	ZP
Н	X	×	Not Enabled	See Table 2
L	L	L	Sum	Sum PAR
L	L	н	XOR	XOR PAR
L	H	L	X·Y	AND PAR
L	Н	н	X + Y	OR PAR

XOR PAR = (Shift PAR) ⊕ [XP ⊕ YP] where Shift PAR = [X7 ⊕ X_{in}) · CD62 + (X8 ⊕ X0)

CD62] · CD60 · CD61

AND PAR = $[(X0 \cdot Y0) \oplus (X1 \cdot Y1) \oplus (X2 \cdot Y2) \oplus ...$ (X3 · Y3)] ⊕ [(X4 · Y4) ⊕ (X5 · Y5) ⊕ ∴

(X6 · Y6) ⊕ (X7 · Y7)]

OR PAR = [AND PAR) (XOR PAR) Sum PAR = $C_{in} \oplus C1 \oplus C2 \oplus C3 \oplus C4 \oplus C5 \oplus$ C6 ⊕ C7 ⊕ T_{Err} ⊕ (XOR PAR)

where c_i is the carry-in for generating bit Z_i for i = 1 to 7.

Complement Y Select

Control input Comp inhibits or enables the complement operation. When Comp is at a logic L, Y data is passed. When Comp is at a logic H, Y is complemented.

TABLE 4

Comp	Operation
C III	Pass Y
н	Complement Y

TABLE 5

CD61	CD60	CD62	OPA	OPB	Comp	Function	ZP
L	L	X	L	L	L	X Plus Y Plus C _{in}	Sum PAR
L	L	X	L.	L	Н	X Plus Y Plus Cin	Sum PAR
L	L	X	L	Н	L	X⊕Y	XOR PAR
U	L	X	L	Н	Н	x⊕Ÿ	XOR PAR
L	Н	L	L	L	L	XSL Plus Y Plus Cin	Sum PAR
L	Н	L	L	L	H S	XSL Plus Y Plus Cin	Sum PAR
L	Н	L	L	Н	E L	XSL (+) Y	XOR PAR
	Н	L	L	Н	Н	XSL⊕Ÿ	XOR PAR
L	Н	Н	L	L	L	XSR Plus Y Plus Cin	Sum PAR
L	Н	Н	L	L	Н	XSR Plus Y Plus Cin	Sum PAR
L	Н	Н	L	Н	L	XSR (+) Y	XOR PAR
L	Н	Н	L	н	н	XSR ⊕ ₹	XOR PAR
L	X	X e	Н	L	X	X-Y	AND PAR
L	X	X	Н	Н	X	X + Y	OR PAR
н	L	L	X	X	X	X	XP
Н	L	Н	X	X	X	Y	YP
Н	Н	L	X	X	X	Shift Left 4 Bits (2)	SL4 PAR
Н	Н	Н	X	X	X	Shift Right 4 Bits (1)	SR4 PAR

(1)The most significant 4 bits of X OR Y are shifted into the least significant 4 bits. The 4 most significant bits are replaced with SR3-SR0 inputs

(2) The least significant 4 bits of X OR Y are shifted into the most significant 4 bits. The 4 least significant bits are replaced with SL7-SL4 inputs + Logical Exclusive-OR

+ Logical Inclusive-OR · Logical AND

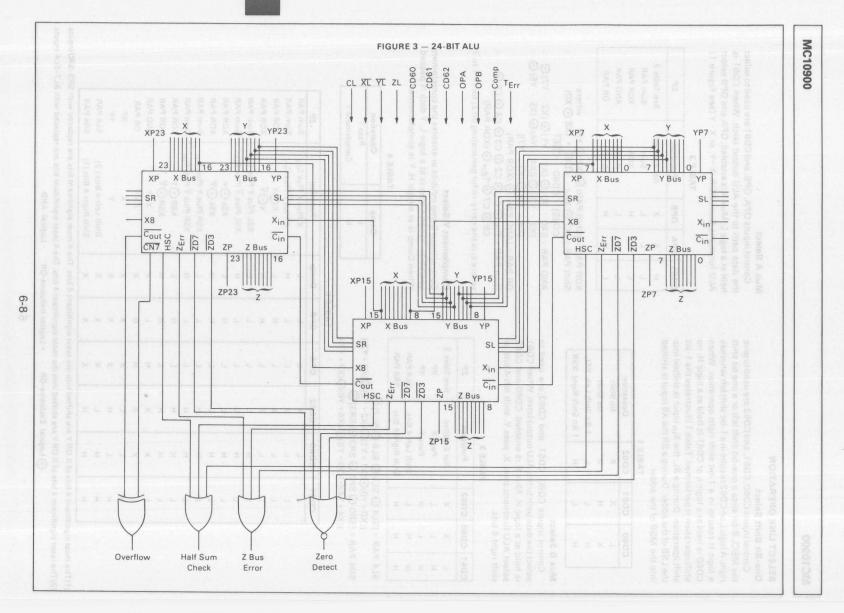


TABLE 6 - RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit	
Supply Voltage (V _{CC} = 0 Volts)	VEE	-4.68 to -5.72	Vdc	
Operating Temperature (Functional)	TA	0 to +70	°c	
Output Drive	-	50 Ω to -2.0 Vdc	-	
Junction Temperature	TJ	130 max	°C	

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the do specifications shown in the test table (Table 7), after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board with heat sink and transverse air flow greater than 1000 linear fpm is maintained. Outputs are terminated through a 50-ohm transistor to -2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs tested in the same manner.

TABLE 7 — ELECTRICAL CHARACTERISTICS

	Test Voltage Values										
@ Test	Volts										
Temperature	VIH max	VIL min	VIHA min	VILA max	VEE						
0°C	-0.840	-1.95	-1.145	-1.490	-5.2						
+25°C	-0.810	-1.95	-1.105	-1.475	-5.2						
+70°C	-0.730	-1.95	-1.050	-1.450	-5.2						

													3.35	D. L. P. Co.		
\$ b b	- a	5 5	12	8 8	N	IC10900	Test Limits	161			= 1		3 7	3 2 5 5		(Vcco)
Characteristics	Symbol	Pin Under	0	c		+25°C		+70)°C		Ø m	Voltage Applie	ed to Pins List	ed Below:		(VCC)
		Test	Min	Max	Min	Тур	Max	Min	Max	Unit	VIH max	VIL min	VIHA min	VILA max	VEE	Gnd
Power Supply Drain Current —	IEE	9, 43	514	855	514	685	855	514	855	mAdc	101	_	100	0.00 P	9, 43	3, 15, 20 26, 60, 66
Input Current CD61, XL, YL, ZL, Cin, OPA	linH	55		600	1-	-	600	- 8	600	μAdc	-	-	Moto Date A 30	A Service of the serv	crus s	HAR
All Others	linL	50 50	0.5	250 —	0.5	Ξ	250 —	0.5	250		50 —	_ 50	300 0	1 2 2 3	1910	300
Logic High Output Voltage	VOH	4	-1.000	-0.840	-0.960	-	-0.810	-0.905	-0.730	Vdc	50, 55, 24	31, 56, 54	Strips Must Strips	A PORT	0	E S
Logic Low Output Voltage	VOL	4	-1.95	-1.665	-1.95	-	-1.650	-1.95	-1 625	Vdc	55, 24	50, 31, 56, 54	2	2 2 3	8	WEE
Logic High Threshold Voltage	VOHA	4	-1.02	-	-0.980	-		-0.925	-	Vdc	55, 24	31, 56, 54	50	7 12 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0.0	0.0
Logic Low Threshold Voltage	VOLA	4	-	-1.645	-	-	-1.630	-	-1.605	Vdc	24, 55	31, 54, 56	8-6-3	50	4	

NOTE: All inputs have input pulldown resistors (~ 68 kf) between the input and VEE.

SWITCHING CHARACTERISTICS OVER OPERATING VOLTAGE AND TEMPERATURE RANGE

Tables 8 and 9 define timing characteristics of the MC10900 over operating voltage and temperature ranges. Worst-Case Setup and Hold and Propagation Delays are calculated for VEE = -5.2 Volts \pm 10% and a Tymax = 115°C. The maximum recommended operating junction temperature is +130°C.

Calculated limits are based on several performance factors as described in Motorola's Preliminary Design

Manual for the MECL 10,000 Macrocell Array. Factors include worst-case delays due to Macro selections, Fan-Out, Metal Lengths, Wire-OR, and Input Follower options. AC measurements are performed on each device to assure process integrity; however, Motorola does not quarantee limits at this time.

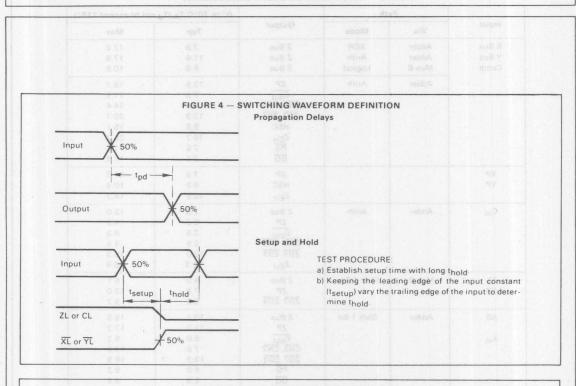
TABLE 8 — SETUP AND HOLD TIMES (nanoseconds)*
0° to +70°C TA (TJ not to exceed +115°C)

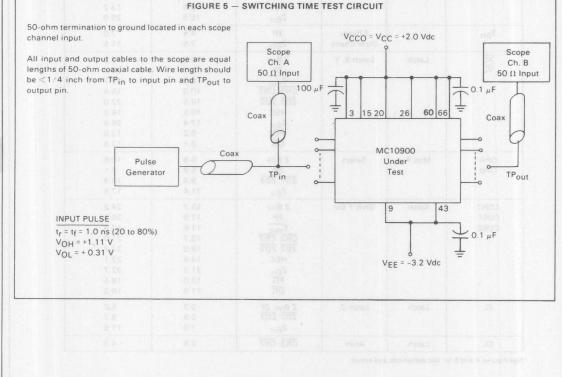
Input	Clock (Ref. Edge)	Output	Setup (Min)	Hold (Min)
X Bus, XP	XL (L - H)	All	1.6	+1.0
Y Bus, YP	YL (L → H)	All	1.6	+1.0
2 X 8 8 8 8	71 (1) 1)	Z Bus	17.8	0
X Bus, Y Bus, Comp	ZL (H L)	ZP	19.2	0
副自己 美國	CL (H - L)	CN3, CN7	14.5	0
XP, YP	ZL (H → L)	ZP	11.7	0
24 0 0 0 0 0 He He	ZL (H → L)	Z Bus	12.0	-1.0
C _{in}	ZL (H → L)	ZP	14.3	-1.0
日日 日 書稿	CL (H L)	CN3, CN7	8.6	-1.0
SL, SR	ZL (H → L)	Z Bus	6.1	+0.5
SL, Sh	ZL (H → L)	ZP	12.0	0
	ZL (H → L)	Z Bus	15.5	-1.0
X8, X _{in}	ZL (H - L)	ZP	17.2	-1.0
	CL (H - L)	CN3, CN7	12.1	-1.0
OPA, OPB	ZL (H → L)	Z Bus, ZP	10.6	+0.5
	ZL (H → L)	Z Bus	24.2	+0.5
CD60, CD61, CD62	ZL (H → L)	ZP	26.1	0
	CL (H → L)	CN3, CN7	21.1	-1.0
X 10 10 10 10 10 10 10 10 10 10 10 10 10	ZL (H → L)	Z Bus	18.9	-0.5
XL, YL (H - L Edge)	ZL (H - L)	ZP	20.4	-1.0
	CL (H - L)	CN3, CN7	15.5	-1.0
T _{Err}	ZL (H - L)	ZP	7.0	0

'See Figures 4 and 5 for test definitions and circuit.

TABLE 9 — PROPAGATION DELAY (nanoseconds)*

Input	Pa		Output		not to exceed 115°)	
mput	Via	Mode	Gatput	Тур	Max	
X Bus	Adder	XOR	Z Bus	7.9	12.2	
Y Bus	Adder	Arith	Z Bus	11.6	17.8	
Comp	Mux B	Logical	Z Bus	6.8	10.8	
	Adder	Arith	ZP	12.5	19.2	
	Addel	Anth	Cout	7.5	11.5	
				9.4	14.4	
			ZD7, ZD3	13.9	20.7	
			HSC	9.8	15.1	
			Z _{Err}	16.7	25.7	
			PG	7.5	11.5	
			GG	7.4	11.3	
XP			ZP	7.6	- bs/ -11.7	
YP			HSC	6.8	10.4	
			Z _{Err}	10.5	16.2	
				-		
Cin	Adder	Arith	Z Bus	7.8	12.0	
			ZP	9.3	14.3	
			Cout CN3, CN7	2.8	4.3 8.5	
			ZD7, ZD3	10.0	15.3	
		EPUOZOGRA TA	Z _{Err}	12.3	18.9	
19100	good draw is no	COLUMN CALIFICATION		-		
marai SL might of	Mux B	Shift 4 Bits	Z Bus	4.0	6.1	
SR			ZP	7.8	12.0	
		bloot som	ZD7, ZD3	6.3	9.7	
X8	Adder	Shift 1 Bit	Z Bus	10.1	15.5	
			ZP	1.1.2	17.2	
Xin			Cout	6.0	9.2	
			CN3, CN7	7.8	12.0	
			ZD7, ZD3	12.3	18.9	
			PG	6.0	9.2	
			GG	5.8	8.9	
				- 8 3 8 0 0 8 .6	13.2	
			Z _{Err}	15.5	23.8	
T _{Err}		Z Parity	ZP	4.5	7.0	
		Error Check	ZErr	7.5	11.5	
XL	Latch	Latch X, Y	Z Bus	12.3	18.9	
TOP YL			ZP	Secric 13,3 4 m MAI	20.4	
			Cout	01 100 11 8.31 040 11	12.7	
			CN3, CN7	10.0	15.4	
			ZD7, ZD3	14.5	22.0	
Locar Cour			HSC xaco	10.5	16.2	
			ZErr	17.4	26.8	
			PG GG	8.2	12.6	
4	- 0000 H	100	10	8.1	12.4	
OPA	Mux A	Select	Z Bus	6.9	10.6	
OPB			ZP ZP	5.9	(ana) 9.1	
			ZD7, ZD3	9.4	14.4	
			ZErr	11.4	17.5	
CD60	Adder	Shift 1 Bit	Z Bus	15.7	24.2	
CD61			ZP	17.0	26.12.09	
CD62			Cout	11.6	17.9	
			CN3, CN7	13.7	21.0	
			ZD7, ZD3	18.0	27.7	
			HSC	14.4	22.1	
			ZErr	21.3	32.7	
			PG GG	12.0	18.5	
			GG	11.9	18.3	
ZL	Latch	Latch Z	Z Bus, ZP	3.3	5.0	
			ZD7, ZD3	5.5	8.7	
			ZErr	7.0	11.6	
			-Err	7.0	11.0	

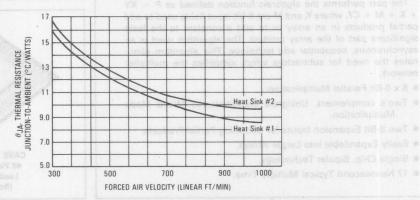




Advance Information

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FIGURE 6 — THERMAL CHARACTERISTICS (TYPICAL)



Heat Sink #1 is from THERMALLOY #15832-1, 3 Horizontal Fins, 0.563 inches square, Model No. 2284C. Heat Sink #2 is from WAKEFIELD #4493, Vertical Fins, 0.5 inches square.

NOTE: $T_J = (\theta_{JA})$ (P_D) + T_A WHERE T_J is the Junction Temperature, T_A is the Ambient Temperature, $P_D = (I_{EB})$ (V_{ED}) + (15 mW) (number of 50 Ω outputs).

Still air 7JA (no heat sink) - 35°C/W.

6

MC10901

Advance Information

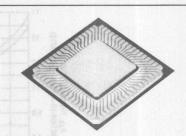
8 X 8 BIT EXPANDABLE MULTIPLIER

The MC10901 is a high speed 8 x 8-bit multiplier that can multiply two eight-bit unsigned or signed 2's complement numbers and generate the sixteen-bit unsigned or signed product. The device can be used as a stand-alone eight-bit multiplier or as a building block for larger multiplier arrays.

The part performs the algebraic function defined as P=XY+K+M+C7, where K and M are 8-bit input fields used to add partial products in an array or to add a constant to the least significant part of the array product. The algorithm used is an asynchronous, sequential add technique. This algorithm eliminates the need for subtractors which simplifies the multiplier network.

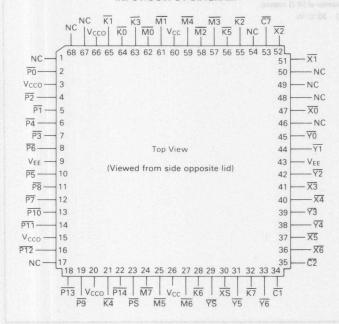
- 8 x 8-Bit Parallel Multiplication.
- Two's complement, Unsigned Magnitude, or Mixed Mode Multiplication.
- Two 8-Bit Expansion Inputs for Summing Partial Products.
- Easily Expandable Into Larger Arrays.
- Single Chip, Bipolar Technology.
- 17 Nanosecond Typical Multiply Time.

MECL-LSI 8 × 8-BIT MULTIPLIER

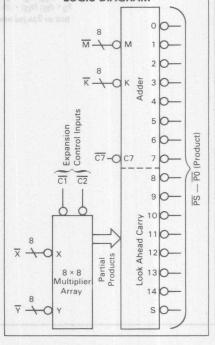


CASE 745 — Z Suffix 68 Pin, JEDEC Std. Leadless Package (Bottom view)

INPUT/OUTPUT DIAGRAM



LOGIC DIAGRAM



The MC10901 is a high-speed programmable 8 x 8-bit multiplier utilizing the MECL Macrocell Array. The MC10901 uses an asynchronous, sequential add technique for multiplying two numbers in either straight magnitude or two's complement notation. The device generates the function: $P = X \cdot Y + K + M + C7$, where;

- · = times
- + = plus
- X = 8-bit multiplicand where X0 is LSB, XS is MSB
- Y = 8-bit multiplier where Y0 is LSB, YS is MSB
- K = 8-bit constant where K0 is LSB, K7 is MSB
- M = 8-bit constant where M0 is LSB, M7 is MSB
- C7 = 1-bit constant in bit position 2^7
- P = 16-bit product where P0 is LSB and PS is MSB

Two control inputs, $\overline{C}1$ and $\overline{C}2$, are provided for simplifying expansion to larger array sizes. The control inputs can be programmed to select either two's complement or straight magnitude multiplication. A carrylookahead technique is used to further improve multiplier performance.

DEVICE OPERATION

The multiplication matrix for the MC10901 is shown in Table 1. This matrix shows how the MC10901 calculates the product. The product is the binary sum of all the terms in the matrix. Note that all the terms in the matrix show positive values. The MC10901 requires negative or inverted inputs and produces a product of negative or inverted outputs when positive logic is used. If negative logic is used, no inversion is

required on the inputs, while the outputs will be the "true" value.

Operation and expansion of the device are controlled by two inputs C1 and C2. When C2 is at a logic H, the X inputs are in straight magnitude form. A low on C2 indicates the X inputs are in two's complement form. The Y inputs and C1 function the same as above. For a straight multiply, control inputs are programmed in the high state. For a two's complement multiply C1 and C2 are programmed in the low state. Due to the nature of the algorithm, correction terms need to be added to obtain the correct two's complement signed product. The sign bits of the X and Y inputs must be added to the product in their respective bit locations. This can be accomplished by connecting Xs and Ys to the M7 and K7 inputs, see figure 1. For expansion into larger arrays, an additional input, C7, has been provided. C7 accomplishes the same function as a M7 or K7 input. If a straight magnitude number is to be multiplied by a two's complement number only the sign bit of the two's complement number is to be added in as correction.

EXPANSION RULES

The MC10901 can be used in larger arrays to produce a two's complement product of 2 two's complement numbers. The following rules apply:

For an M-bit by N-bit multiplier, an (M + N) bit product is formed. The number of MC10901's equals (M x N) /64. As an example, a 32 x 32-bit array (figure 3) requires (32 x 32) /64 = 16 packages.

TABLE 1 — MULTIPLICATION MATRIX FOR MC10901 (P = (X) times (Y) plus K plus M plus C7)

				1 20 20	29-71 34 54										
100								C7							
0.485				1 25	10000			K7	K6	K5	K4	КЗ	K2	K1	KO
			-	LI DO				M7	M6	M5	M4	МЗ	M2	M1	MO
			-	1 613				XS-(C2⊕Y0)	X6-Y0	X5-Y0	X4-Y0	X3-Y0	X2-Y0	X1-Y0	X0-Y
191			-	H 075			XS-(C2⊕Y1)	X6-Y1	X5-Y1	X4-Y1	X3-Y1	X2-Y1	X1-Y1	X0-Y1	
200			100000000000000000000000000000000000000	4 173		XS-(C2⊕Y2)	X6-Y2	X5-Y2	X4-Y2	X3-Y2	X2-Y2	X1-Y2	X0·Y2		
	C1-C2-YS		-	4 675	XS-(C2⊕Y3)	X6-Y3	X5-Y3	X4-Y3	X3-Y3	X2-Y3	X1-Y3	X0-Y3			
	C1-C2-XS		PROPERTY AND IN	XS-(C2⊕Y4)	X6-Y4	X5-Y4	X4-Y4	X3-Y4	X2-Y4	X1-Y4	X0-Y4		9145		1
100	C1-C2-XS-YS		XS-(C2⊕Y5)	X6-Y5	X5-Y5	X4-Y5	X3-Y5	X2-Y5	X1-Y5	X0-Y5		N 19			
100	C1-C2-XS-YS	XS-(C2⊕Y6)	X6-Y6	X5-Y6	X4-Y6	X3-Y6	X2-Y6	X1-Y6	X0-Y6						1999
C1-C2	XS-YS-(C1⊕C2)	YS-(C1⊕X6)	YS-(C1⊕X5)	YS-(C1⊕X4)	YS-(C1⊕X3)	YS-(C1⊕X2)	YS-(C1⊕X1)	YS-(C1⊕X0)	Di-	and I					
PS	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	PO

Note: For magnitude operations (C1 = 0, C2 = 0 or C1 = H, C2 = H), the C7 input must be tied to a "High" voltage state in order to eliminate the possibility of overflow and invalid results. For X = 255, Y = 255, K = 255, and M = 255, the product will be the maximum value possible of 65,535 (PS - P0 = 1). If C7 was also used as an input during magnitude operations, the most significant product bit, PS will be a "1" (PS = L) during an overflow condition where the result exceeds 65,535.

For 2's complement or mixed mode multiplications, the multiplication matrix (Table 1) produces the proper product at the PS through P0 outputs.

- The normal parallelogram structure consists of several stages, each multiplying 8 bits of multiplier times 8 bits of multiplicand and adds the partial products.
- 3. The sign bits of the multiplicand and multiplier must be added to the product. As an example, an 8 x 16-bit multiplier would require the sign bit of the 8-bit word to be added to the least significant 8th bit of the product. Likewise the sign bit of the 16-bit word is to be added to the least significant 16th bit of the product. The X sign bit and Y sign bit must be added to the product with a binary weight (power of 2) equivalent to their respective binary weights.
- The control inputs C1 and C2 must be programmed correctly depending on the multiplier type and on the position of the MC10901 within the array:
 - A) For magnitude arrays, all control inputs are programmed "H".
 - B) For two's complement arrays, the programming is controlled by the position of the multiplier and the terms required by the algorithm.

A simple means of determining the required control line states is shown in the following table:

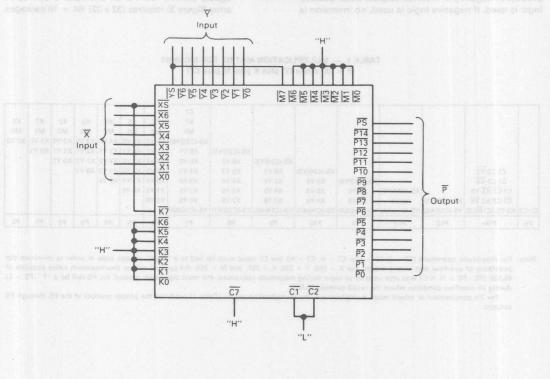
Multiplication Inputs	C1	C2
NO SIGN BITS	HI	н
X _S ONLY	HI	LOW
XS ONLY	LOW	HI
BOTH SIGN BITS	LOW	LOW

The maximum times possible for various N-bit by N-bit arrays are:

Number Of Bits	Total Multiply Time (ns) Max.	Package Count
8	24.3	C7 = 1-bit operant is
16	51.8	W 1210040 nd-81 = 9
24	81.5	lateran ge uneo owi
32	111.2	16

Because of the versatility of the MC10901, many other arrays can be built. Faster arrays using additional adders, pipeline techniques, one's complement and magnitude multipliers, and truncated product multipliers can be constructed. Applications of such arrays include digital filters, FFT's, complex multipliers, and recursive and nonrecursive filter elements.

FIGURE 1



16 X 16-BIT EXAMPLE

Figure 2 shows 4 MC10901's in a 16 x 16-bit array. A 32-bit two's complement product is produced from a 16-bit multiplier and a 16-bit multiplicand. At the first level of multiplication, no partial products have been obtained so the \overline{K} and \overline{M} expansion inputs are tied high. These inputs on the first level can be used to add a constant to the least significant end of the product. Further levels require the \overline{K} and \overline{M} inputs to add the accumulated partial products. Control inputs $\overline{C}1$ and $\overline{C}2$ are programmed according to their relative position of each device in the array. Since both \overline{X} and \overline{Y} are in two's complement form, their respective sign

bits must be added to the accumulated products for correction. This can be accomplished by inputing the sign bit of the \overline{X} input to $\overline{C7}$ of device B and sign bit of the \overline{Y} bus to $\overline{C7}$ of device C. The same expansion techniques are extended to the 32 x 32-bit multiplier in Figure 3.

However, when adding the sign bits to the array for correction, the sign bits must be added to the $\overline{C7}$ input of the devices that have $\overline{C1} = H$, $\overline{C2} = L$ or $\overline{C1} = L$, $\overline{C2} = H$ in the 32nd bit of the product, as indicated in Figure 3. The sign bits cannot be added to the $\overline{C7}$ input of devices that have $\overline{C1} = H$ and $\overline{C2} = H$, as indicated in Table 1.

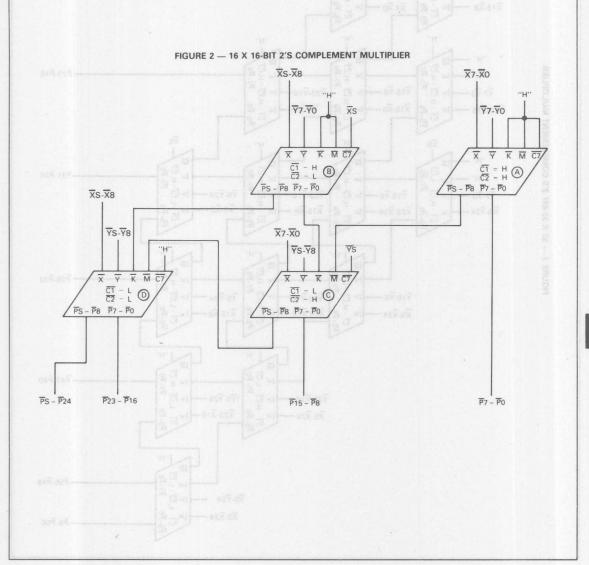


TABLE 2 — ABSOLUTE MAX RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (V _{CC} = 0)	VEE	-8 to 0	Vdc
Input Voltage (VCC = 0)	V _{in}	0 to VEE	Vdc
Output Source Current — Continuous — Surge	Io	<30 <100	mAdc
Storage Temperature	T _{stg}	-55 to +150	°C
Junction Temperature	TJ	165	°C

NOTE: 1. Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

TABLE 4 — ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board with heatsink and transverse air flow greater than 1000 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs tested in the same manner.

Parameter	Symbol	Value	Unit
Supply Voltage (V _{CC} = 0 Volts)	VEE	-4.68 to -5.72	Vdc

TABLE 3 — RECOMMENDED OPERATING CONDITIONS —

MC10901

Parameter	Symbol	Value	Unit	
Supply Voltage (V _{CC} = 0 Volts)	VEE	-4.68 to -5.72	Vdc	
Operating Temperature (Functional)	TA	0 to +70	°C	
Output Drive	의 의 기 영기	50 Ω to -2.0 Vdc	90 900	
Max Junction Temp	TJ	130	°C	

		Test	Voltage Valu	ies	
@ Test			Volts		
emperature	VIH max	VIL min	VIHA min	VILA max	VEE
0°C	-0.840	- 1.95	-1.145	-1.490	-5.2
+ 25°C	-0.810	- 1.95	-1.105	-1.475	-5.2
+70°C	-0.730	- 1.95	- 1.050	- 1.450	-5.2

										+ 10-0	-0.730	-1.95	- 1.050	-1.450	-5.2	N. 10 100
Pin			18	MC10901 Test Limits						2	2 0 0			(Vcco)		
Characteristics	Symbol	Under	0°	С	9 5 6	+ 25°C		8	+70°C		Voltage Applied to Pins Listed Below				3 1	(VCC)
		Test	Min	Max	Min	Тур	Max	Min	Max	Unit	VIH max	VIL min	VIHA min	VILA max	VEE	E Gnd
Power Supply Drain Current	IEE	9,43	-	868	700	695	868	-	868	mAdc	-	- N	10 mm		9,43	3,15,20 26,60,66
Input Current C1, C2, X, Y K4, M4, M5, M6, M7	linH linH	= 101	ŧ	650 300	Mary Sur	Carisqua	650 300	=	650 300	μAdc μAdc	47 47	WASIO 	und thus not thing out thing	seriores pele Luc nu serre	d	S SIGNAL
All Others	linH liNL		1	200	0.5	_ §	200	_	200	μAdc μAdc	47	47		2 2 S	AGE AGE	and a second
Logic "H" Output Voltage	VOH	2	-1.000	-0.840	- 0.960	- 49	-0.810	- 0.905	- 0.730	Vdc	34,35,53 47	8-	1 2 2 2	10.0 10.0 10.0 10.0 10.0 10.0 10.0 10.0	9 7 8	esmit tipod e m.
Logic "L" Output Voltage	VOL	2	- 1.950	- 1.665	- 1.950	- 170	- 1.650	- 1.950	- 1.625	Vdc	34,35,53	47	200 K	1000		2 4 6
Logic "H" Threshold Voltage	VOHA	2	-1.02	-	-0.980	- 1	-	- 0.925	1	Vdc	34,35,53	1 -	47			
Logic "L" Threshold Voltage	VOLA	2		- 1.645	A 0 7	7.6	- 1.630	-	-1.605	Vdc	34,35,53	18-1	2 2 2	47		5 5 G

NOTE: All inputs have input pulldown resistors (\sim 68K Ω) between the input and VEE.

SWITCHING CHARACTERISTICS OVER OPERATING VOLTAGE AND TEMPERATURE RANGE

Table 5 defines the timing characteristics of the MC10901 over operating voltage and temperature ranges. Worst-Case Setup and Hold and Propagation Delays are *calculated* for $V_{EE}=-5.2$ Volts \pm 10% and a Tymax = 115°C. The maximum recommended operating junction temperature is \pm 130°C.

Calculated limits are based on several performance factors as described in Motorola's Preliminary Design Manual for the MECL 10,000 Macrocell Array. Factors include worst-case delays due to Macro selections, Fan-Out, Metal Lengths, Wire-OR, and Input Follower options. AC measurements are performed on each device to assure process integrity; however, Motorola does not guarantee limits at this time.

FIGURE 4 — SWITCHING WAVEFORM DEFINITION Propagation Delays

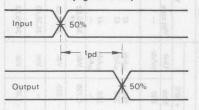
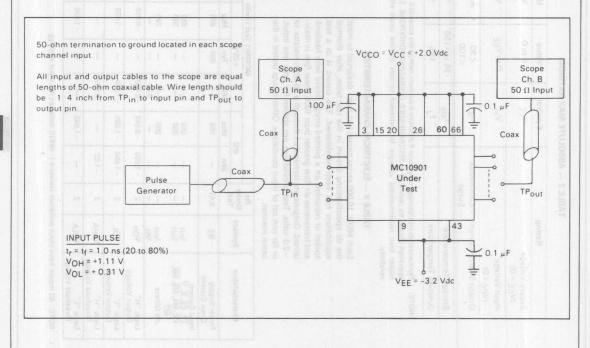


TABLE 5 — PROPAGATION DELAY (Nanoseconds)

Input	Output	0 to 70°C TA (TJ not to exceed 115°C)			
	17 5	Тур	Max		
$\overline{X7} - \overline{X0}, \overline{Y7} - \overline{Y0},$	P6 - P0	13.9	19.9		
	P7	13.0	18.6		
	P14 - P8	17.0	24.3		
	PS	16.3	23.3		
M7 – M0	P6 - P0 P7 P14 - P8 PS	7.8 6.9 9.3 8.6	9.8 13.3 12.3		
<u>K4</u> – <u>K0</u>	P6 - P0	8.2	11.7		
	P7	7.2	10.3		
	P14 - P8	9.7	13.8		
	PS	8.9	12.7		
<u>K6, K5</u>	P6 - P0	9.4	13.4		
	P7	10.5	15.0		
	P14 - P8	12.9	18.4		
	PS	12.2	17.4		
<u>K7</u>	P7	9.9	14.1		
	P14 – P8	13.9	19.9		
	PS	12.2	18.8		
C7	P7	10.8	15.4		
	P14 – P8	14.9	21.2		
	PS	14.1	20.1		

FIGURE 5 — SWITCHING TEST CIRCUIT

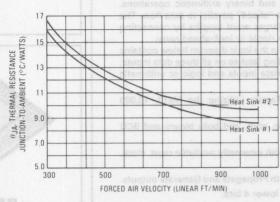




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FIGURE 6 — THERMAL'CHARACTERISTICS

(TYPICAL) QUIDING A DESIGN OF SELECTION OF SELE



Heat Sink #1 is from THERMALLOY #15832-1, 3 Horizontal Fins, 0.563 inches square, Model No. 228AC.

Heat Sink #2 is from WAKEFIELD #4493, Vertical Fins, 0.5 inches square.

NOTE: $T_J = (\theta_{JA}) (P_D) + T_A$ WHERE T_J is the Junction Temperature, T_A is the Ambient Temperature,

 $P_D = (I_{EE}) (V_{EE}) + (15 \text{ mW}) \text{ (number of 50 }\Omega \text{ outputs)}$

Still air TJA (with no heat sink) = 35°C/W.

EA. A BUS EB B GUS EC C BUS C C BUS EACH A Latch C Lat

MC10902

Advance Information

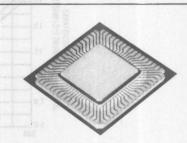
8-BIT BINARY/BCD ALU SLICE

The MC10902 is a high speed ALU building block for digital processors. The circuit operates directly on BCD data in addition to doing normal logic, shift, and binary arithmetic operations. Each part is 8 bits wide and is "sliced" parallel to data flow. The MC10902 easily expands to larger word lengths by connecting circuits in parallel, either with ripple or look-ahead carry.

The MC10902 as illustrated in the logic diagram below contains independently controlled holding latches on all three data inputs. Five function (F) lines select data inputs and logic or arithmetic circuit operation.

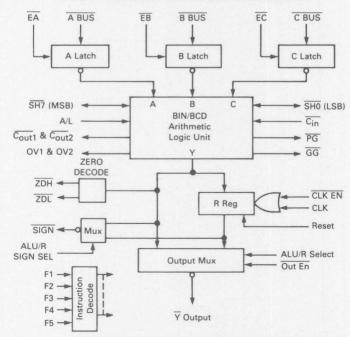
- Member of the M10900 Family utilizing the MECL 10,000 Macrocell Array.
- 34 functions including logic, shift, and both binary and BCD arithmetic.
- Internal 8-bit accumulator with externally available reset, clock, and clock enable.
- Internal look-ahead carry with Propagate and Generate outputs.
- Zero detects for upper and lower 4 bits.
- · Select pin for logic or arithmetic shift right.

MECL-LSI 8-BIT BINARY/BCD ALU SLICE



CASE 745
68 Pin, JEDEC Std.
Leadless Package

FIGURE 1 — 8-BIT BINARY/BCD ALU SLICE BLOCK DIAGRAM

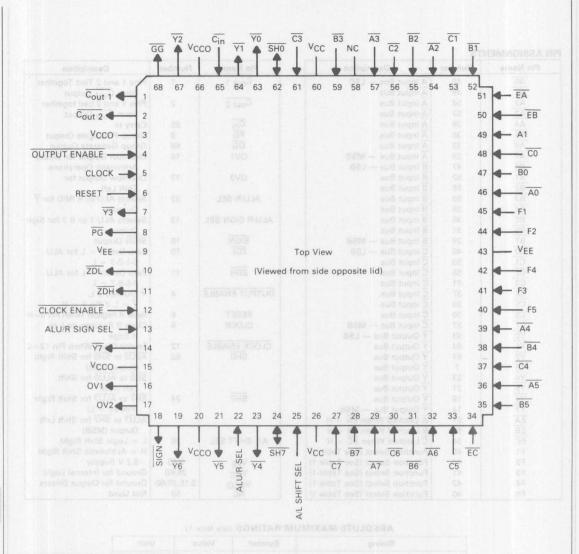


Pin Name	Number	Description	Pin Name
A0	46	A Input Bus — LSB	Cout 1
A1	49	A Input Bus	
A2	54	A Input Bus	Cout 2
A3	57	A Input Bus	
A4	39	A Input Bus	Cin
A5	36	A Input Bus	PG
A6	32	A Input Bus	GG
A7	29	A Input Bus — MSB	OV1
B0	47	B Input Bus — LSB	
B1	52	B Input Bus	OV2
B2	55	B Input Bus	
B3	59	B Input Bus	ALU/R SEL
B4	38	B Input Bus	/ ALOM OLL
B5	35	B Input Bus	ALU/R SIGN S
B6	31	B Input Bus	ALOM SIGN S
B7	28	B Input Bus — MSB	SIGN
CO	48	C Input Bus — LSB	ZDL
C1	53	C Input Bus — LSB	ZUL
C2	56	C Input Bus	ZDH
C3	61	C Input Bus	ZDH
C4	37	C Input Bus	OUTPUT ENAB
C5	33		OUTFUT ENAL
		C Input Bus	DECET
<u>C6</u>	30	C Input Bus	RESET
C7	27	C Input Bus — MSB	CLOCK
YO	63	Y Output Bus — LSB	OLOOK ENLADI
	64	Y Output Bus	CLOCK ENABI
Y2	67	Y Output Bus	SH0
Y3	7	Y Output Bus	
<u>Y4</u>	23	Y Output Bus	No. of the last of
Y5	21	Y Output Bus	
<u>Y6</u>	19	Y Output Bus	SH7
Y7	14	Y Output Bus — MSB	25 22 24 24
EA	51	A Latched When EA = H	
EB	50	B Latched When EB = H	
EC	34	C Latched When EC = H	A/L SHIFT SE
F1	45	Function Select (See Table 1)	2 中上中
F2	44	Function Select (See Table 1)	VEE
F3	41	Function Select (See Table 1)	VCC
F4	42	Function Select (See Table 1)	Vcco
F5	40	Function Select (See Table 1)	NC

Pin Name	Number	Description
Cout 1	va ¹ sa	Pins 1 and 2 Tied Together Form Cout Output
Cout 2	2	Pins 1 and 2 tied together Form Cout Output
Cin	65	Carry In
PG	8	Group Propagate Output
GG	68	Group Generate Output
OV1	16	Overflow Output for Binary Arithmetic Operations
OV2	17	Overflow Output for Shift Left
ALU/R SEL	22	Selects ALU or R REG for Y Outputs
ALU/R SIGN SEL	13	Selects ALU 7 or R 7 for Sign
SIGN	18	SIGN Output
ZDL	10	Zero Detect = L for ALU 0-1-2-3 = L
ZDH	11	Zero Detect = L for ALU 4-5-6-7 = L
OUTPUT ENABLE	4	\overline{Y} Enabled if L, \overline{Y} = L if Pin 4 = H
RESET	6	Reset R Register When Pin 6=H
CLOCK	5	Clock R Register on L to
CLOCK ENABLE	12	Enable Clock When Pin 12=
SH0	62	ALU0 to SH0 for Shift Right Output (LSB)
		SH0 to ALU0 for Shift
SH7	24	Left Input SH7 to ALU7 for Shift Right (PIN 25 = L)
	18 19 2	ALU7 to SH7 for Shift Left
A/L SHIFT SEL	25	Output (MSB) L = Logic Shift Right
8 W P 8 00	0.42	H = Arithmetic Shift Right
VEE	9,43	-5.2 V Supply
Vcc	26,60	Ground for Internal Logic
Vcco	3,15,20,66	Ground for Output Drivers Not Used

ABSOLUTE MAXIMUM RATINGS (see Note 1)

Supply Voltage (V _{CC} = 0)	VEE	-8 to 0	Vdc	CHITECTURAL I	
Input Voltage (V _{CC} = 0)	V _{in}	0 to V _{EE}	Vdc	the M10900 familical Array The A	
Output Source Current — Continuous — Surge	l _o lo edi evel 0	<30 <100		threate and BCD and Value of three input value.	
Storage Temperature	T _{stg}	-55 to +150	°C °C	gle bir date paths	
Junction Temperature	TJ	165	°C	arconnect MC1990 pagate and grav	



ARCHITECTURAL DESCRIPTION

The MECL 8-bit BCD/Binary ALU Slice is a member of the M10900 family utilizing the MECL 10,000 Macrocell Array. The ALU performs logic, shift, binary arithmetic and BCD arithmetic operations on one or two of three input variables, \bar{A} Bus, \bar{B} Bus, and \bar{C} Bus. Single bit data paths \bar{C}_{in} , $\bar{C}_{out\,1}$, $\bar{C}_{out\,2}$, \bar{S}_{in} , and \bar{S}_{in} interconnect MC10902s for longer word lengths. Group propagate and group generate outputs can be used with external look-ahead carry logic for faster system performance.

A \overline{Y} output multiplexer selects output data from either the ALU or R Register outputs. Sign select input

selects the ALU or R Register MSB for a special \overline{SIGN} condition code output. Independent selects permit monitoring the ALU sign bit while reading the R Register in a pipelined structure. Other condition code outputs such as zero detect, carry out, and overflow are taken directly off the ALU. Zero Detect is divided into \overline{ZDL} for bits 0 through 3 and \overline{ZDH} for bits 4 through 7 allowing zero detect of BCD digits. The $\overline{C_{out~1}}$ and $\overline{C_{out~2}}$ must be connected together externally to form $\overline{C_{out~2}}$

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TABLE 1 — MC10902 ALU LOGIC FUNCTIONS

					LC	OGIC FUNC	TIONS	
Function No.	F5	F4	F3	F2	F1	A/L	ALU Function	Y (ALU Output)
16	Н	L	L	L	L	X	OR	A + B
18	H	L	L	Н	L	X	OR	C + B
	L	L	L	L	L	X	NOR	A + B
2	L.	L	L	Н	L	X	NOR	C + B
21	Н	L	Н	L	Н	X	AND	A · B
5	Luch	L	Н	L	Н	X	NAND	A · B
7	Lo	L	H	H	Н	X	Logic 1	sied upea Tues
12	atebe	H	Н	Lo	L	X	Logic 0	
8	JOIL 1	н	PLD I	q Lq	CLOT	X	EX OR	A ⊕ B
10	pollo	H	84.	- H	Line	X	EX OR	C⊕B
vez 11 orluv	L	He	L	H	o Hol	X	EX NOR	A ⊕ B
6	Ja La	6560	H	Н	o Linu	X	Invert	and only Change side
4 4	8 Lo	eu Lsv	H	- L	Late	X	Invert	I III) ma A A deuc
9 9	tell bis	H	BL	o Le	Had	X	Logic	$A + \overline{B}$
14	L	H	H	H	L	X	Logic	C · B

TABLE 2 - MC10902 ALU ARITHMETIC FUNCTIONS

					ARITI	HMETIC F	UNCTIONS	
Function No.	F5	F4	F3	F2	F1	A/L	ALU Function	Y (ALU Output)
28	Н	OH.	Н	L	L	X	Binary Add	A Plus B Plus Cin
30	Н	H	Н	Н	L	X	Binary Add	C Plus B Plus Cin
29	H	Н	Н	L	Н	X	Binary Sub	A Plus B Plus Cin
31	Н	Н	Н	Н	Н	X	Binary Sub	B Plus A Plus Cin
24	Н	Н	L	L	L	X	BCD Add*	A Plus B Plus Cin
26	Н	H	L	Н	L	X	BCD Add*	C Plus B Plus Cin
25	Н	Н	L	L	Н	X	BCD Sub*	A Plus (9's Comple ment of B) Plus Cir
27	H	Н	belief	Н	HVO TOURTS	X	BCD Sub*	B Plus (9's Comple ment of A) Plus Cir
20	Н	L	Н	L	L	X	Increment	A Plus Cin
23	Н	L	Н	Н	Н	X	Increment	B Plus Cin
22	H	L	H	Н	L	X	Increment	C Plus Cin
15	L	H	H	Н	Н	X	Complement	A Plus Cin
13	16000	H	Н	DE	H	X	Complement	B Plus Cin

*NOTE: For BCD, each four-bit BCD (binary coded decimal) number must have a decimal equivalent of 0 to 9 to be a valid input where A7, A6, A5, A4 is the most significant BCD Digit and A3, A2, A1, A0 is the least significant digit (the B BUS and C BUS inputs are similar).

sedencio CIUS, rewol and perfey are TABLE 3 - MC10902 ALU SHIFT FUNCTIONS WARE TRUSA here JRZ RULLA frestown

HEU THEAT	WHS THE	N -1191	STE UT	Man h	SI	HIFT FUN	CTIONS	= M3 TUO) belo
Function No.	F5	F4	F3	F2	F1	A/L	ALU Function	Y (ALU Output)
1	L	L	L	L	Н	L	Logic Shift Right	A
+84UA-	ALJUS	L	JAL "	L	Н	Н	Arithmetic Shift Right	inis-licol At 10 y
3	L	L	L	Н	Н	L	Logic Shift Right	В
3	L	L	L	Н	Н	Н	Arithmetic Shift Right	В
17	Н	L	L	L	Н	X	Shift Left	A
19	Н	L	L	Н	Н	X	Shift Left	В

Function Select — F1, F2, F3, F4, and F5

F1 through F5 inputs control the ALU function and select from A, B, and C Bus inputs. (See Tables 1, 2, and 3.) Two instructions, shift right A Bus and shift right B Bus, use the A/L SHIFT SELECT input to control the sign bit for arithmetic or logic shifts. Tables 1, 2, and 3 define ALU operation at A, B, C, and Y nodes which are complemented at the package pins.

Data Inputs - A0-A7, B0-B7, and C0-C7

Data enters the MC10902 through three 8-bit data ports. Bit 0 is always the least significant and Bit 7 is the most significant. Each port can be latched independently.

Input Latch Enables - EA, EB, and EC

Each input bus is routed through an 8-bit latch controlled by independent latch enable pins. A low logic level (L) on the enable opens the latch allowing input data to ripple through. A high (H) level latches the circuit holding ALU inputs constant independent of data changes on the bus ports.

Data Outputs - Y0-Y7

Data exits the MC10902 through Y Bus outputs. As with input data, bit 0 (Y0) is the least significant and Y7 the most significant. Y output data can be selected from either the ALU or R Register.

Output Mux Controls — ALU/R SEL and OUT **ENABLE**

Output MUX control is shown in Table 4. OUT ENABLE forces the Y outputs to a MECL low logic level simplifying computer bus architectures.

TABLE 4 — OUTPUT MUX CONTROL

ALU/R SEL	OUT EN	Y BUS
L	La tour	R REGISTER
Н	L	ALU
X	Н	OUTPUT LOW (L)

Sign Bit and Control - SIGN and ALU/R Sign SEL

A sign bit condition code output displays the most significant bit of the R Register or ALU as selected by the ALU/R SIGN SEL input. A low (L) on the select input gives the R Register MSB and a high (H) selects the ALU MSB.

Note if ALU/R SEL and ALU/R SIGN SEL inputs are connected together, SIGN will be the same as Y7 when the Youtput is enabled (OUT EN = L).

Carry In - Cin

Cin is used to interconnect ALUs for word lengths longer than 8 bits. Cin connects Cout of the previous ALU for ripple carry or to look-ahead carry logic for look-ahead carry. Carry-in functions only for arithmetic operations and has no effect on logic, see Tables 1, 2, and 3.

Carry Out — Cout 1 and Cout 2

Carry out, Cout, for the MC10902 is equal to logic Cout 1 OR Cout 2. IMPORTANT the OR function is implemented externally by connecting pins 1 and 2 together forming a MECL wired OR. Carry out automatically adjusts to binary or BCD arithmetic operations. Carry out may be high or low during ALU logic and shift functions and should be ignored since this is a "don't care" condition.

Group Propagate and Generate - PG and GG

Group propagate and group generate connect to external look-ahead carry logic (MC10179 or equivalent logic) for best performance when several MC10902 circuits operate in parallel. PG output goes to a low (L) state when the value of a binary arithmetic calculation is 255 or a BCD calculation is 99 (not including Cin). GG goes to a low level when a binary calculation exceeds 255 or a BCD calculation exceeds 99 (not including Cin) and is a high for all other numbers. The PG output will be a high level when the value of a binary calculation is less than 255 or a BCD calculation is less than 99 (not including Cin). Propagate and generate may be high or low during ALU logic and shift functions and should be ignored since this is a "don't care" condition.

Overflow — OV1 and OV2

OV1 is the overflow for binary arithmetic operations, while OV2 is the overflow for shift left operations. These two signals can be connected together (wire ORed) so that either condition will cause an overflow condition. In a system, the most significant slice is used to form the overflow function.

- 1. OV1 is enabled only during binary arithmetic operations (OV1 = L for all non-binary arithmetic operations). OV1 = H means that the sign bit (MSB) is in error due to the result exceeding the maximum positive or negative word value. OV 1 = (Cout & C7) · (function No. 13, 15, 20, 22, 23, 28-31) where C7 is the carry-in for generating ALU bit Y7.
- 2. OV2 is enabled only during shift left operations (OV2 = L for all other operations). OV2 = H means the sign bit has changed state due to the shift left operation. OV2 = (SH7 + Y7) · (function 17, 19)

Zero Detect — ZDL and ZDH

Zero Detects show when the lower (ZDL) or upper (ZDH) four bits of the ALU results are all positive logic zero (low L logic state). ZDL and ZDH can be externally connected together generating an 8-bit ZD. Zero detect outputs are defined by the following equations:

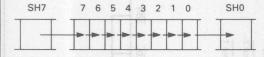
> ZDL = ALU0 + ALU1 + ALU2 + ALU3 ZDH = ALU4 + ALU5 + ALU6 + ALU7

 $\overline{SH0}$ and $\overline{SH7}$ are bidirectional single bit data lines. For shift right, $\overline{SH0}$ is an output and $\overline{SH7}$ is an input. For shift left, $\overline{SH0}$ is an input and $\overline{SH7}$ is an output. In addition, shift right may be logic or arithmetic controlled by the A/L SHIFT SELECT as shown below. The $\overline{SH0}$ and $\overline{SH7}$ are "low" for all ALU operations not requiring shift right or shift left.

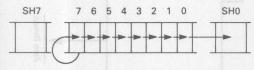
SHIFT LEFT (A/L SEL = DON'T CARE)



LOGIC SHIFT RIGHT (A/L SEL = L)



ARITHMETIC SHIFT RIGHT (A/L SEL = H)



R Register Control — CLOCK, CLOCK EN, and RESET

The MC10902 has a built in 8-bit register, R Register (composed of master/slave flip-flops), primarily in-

tended for pipeline system structures. The R Register can also function as an accumulator by connecting the \overline{Y} outputs to one of the three input buses. The respective bus input latch can hold accumulator data, thus freeing the \overline{Y} Bus for ALU output results.

CLOCK and CLOCK EN are equal inputs, logic ORed together as shown on the Page 1 logic diagram. Either input will clock the R Register on a low to high transition if the other input is low (L). Assigning pin 5 as CLOCK, pin 12 can be used for clock enable. A logic low (L) on CLOCK EN enables CLOCK to update R Register with ALU results on each positive going CLOCK transition. A high (H) on CLOCK EN disables the CLOCK. Care should be taken to disable the clock, low to high transition on CLOCK EN, while the CLOCK is high. Otherwise CLOCK EN could clock the R REGISTER.

Reset sets the R Register to all bits equal logic low (L). (\overline{Y}) bus output = H when R register is selected).

Reset R Register = Reset · (CLOCK + CLOCK EN)

Reset can be made to appear independent of clocking signals (asynchronous) by connecting RESET to CLOCK EN forcing both high at the same time. However, a narrow positive going spike (1 to 2 ns wide) on the R Register output can result on the leading edge of Reset. This narrow pulse can also occur if the Reset = H while clocking the R register (CLK switches from L to H while CLOCK EN = L).

Positive versus Negative Logic

System designers use MECL 10,000 in both positive and negative logic formats. Positive logic has MECL VOH (approx. –0.9V) for logic 1 and MECL VOL (approx –1.7 V) for logic 0. Negative logic reverses logic 1 and 0 voltage definitions with VOL being a logic 1. This data sheet is written around positive logic definitions. Tables and descriptions are written in terms of high (H) and low (L) logic levels to simplify translation between formats.

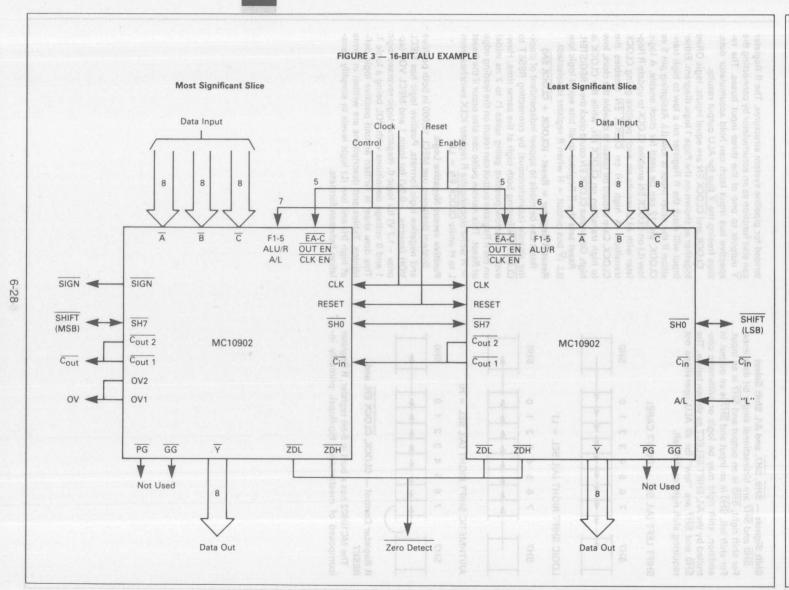


TABLE 5 — RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Supply Voltage (V _{CC} = 0 Volts)	VEE	-4.68 to -5.72	Vdc
Operating Temperature (Functional)	ТА	0 to +70	°C
Output Drive	_	50 Ω to -2.0 Vdc	-
Junction Temp	TJ	130 Max	°C

TABLE 6 — ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board with heat sink and transverse air flow greater than 1000 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs tested in the same manner.

	1 333	Test	Voltage Valu	ies	1			
@ Test	Volts							
Temperature	VIH max	VIL min	VIHA min	VILA max	VEE			
0°C	-0.840	- 1.950	-1.145	- 1.490	-5.2			
+ 25°C	-0.810	- 1.950	-1.105	- 1.475	-5.2			
-70°C	-0.730	- 1.950	-1.050	- 1.450	-5.2			

										100	0.730	1.000	1.000	1.450	0.2	
		Pin			N	AC10902	Test Limits									
Characteristics Symbol	Under	0°	С	1	+25°C			+70°C		V	oltage Appl	ied to Pins Li	sted Below		(Vcco	
	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	VIH max	VIL min	VIHA min	VILA max	VEE	Gnd	
Power Supply Drain Current	IEE	9,43		890	-	712	890	-	890	mAdc		-	# E 8		9,43	3,15,20 26,60,60
		4	7 - 1	1750	-	-	1750	- 1	1750	μ Adc	4	8-	0 20 8	8 5 B	1 7 4	8 8
	L	40 45,42	1-1	750	_		750	-8	750	μ Adc	40	8 -	08 m 00	1 - 65.		adian e
Input Current	linH	24, 44,41, 50,51, 65,34, 12,5, 22,6	X	550			550	pris accord	550	μ Adc	65	STORE BANK	due to Mac thirs JO-en are percon	Order + are transported to transported to	oy Side -	aling onerse
		*	1 - 1	200	_	-	200	-11	200	μ Adc	46	0 - 0	3 4 5	5 3 S E	3 9 7	2 3
	linL	/ *	0.5	- 1	0.5	_	_	0.5		μ Adc		46	1 1 1 2 1	5 5 5 5	111	1 9 9
Logic "1" Output Voltage	VOH	63	-1.000	-0.840	- 0.960		-0.810	- 0.905	-0.730	V _{dc}	5,6,13,22 25,65	夏-H	0 d d d	3 6 6 8	3 3 8	
Logic "0" Output Voltage	VOL	63	-1.950	- 1.665	-1.950	-	- 1.650	- 1.950	-1.625	V _{dc}	13,22,25 41,44,45,65	- 5	8 - 8	E 0 0 E	3 1 8	0 B 0
Logic "1" Threshold Voltage	Vона	63	- 1.02	- 1	- 0.980		-	-0.925	(A - L	V _{dc}		0 - 8	5,6,13,22, 25,65	1 4 3 3	1010	T ST
Logic "0" Threshold Voltage	VOLA	63		- 1.645	_		- 1.630	-	- 1.605	Vdc	34	-4 - g	13,22,25,41 44,45,65	9 5 9		*

^{*}All or All Other Inputs

NOTE: All inputs have input pulldown resistors (\sim 68 k Ω) between input and VEE

Switching Characteristics Over Operating Voltage and Temperature Range

Tables 7 and 8 define timing characteristics of the MC10900 over operating voltage and temperature ranges. Worst case Setup and Hold and Propagation Delays are calculated for VEE $=-5.2\,\text{volts}\pm10\%$ and a T_J max $=115^\circ\text{C}$. The maximum recommended operating junction temperature is $+130^\circ\text{C}$.

Calculated limits are based on several performance factors as described in Motorola's Preliminary Design Manual for the MECL 10,000 Macrocell Array. Factors include worst case delays due to Macro selections, Fan-Out, Metal Lengths, Wire-Or, and Input Follower options. AC measurements are performed on each device to assure process integrity; however, Motorola does not guarantee limits at this time.

TABLE 7 — SET UP AND HOLD TIMES (NANOSECONDS) 0 to 70°C T_A (T_J NOT TO EXCEED 115°C)*

Input	Clock (Ref. Edge L To H)	Set up (Min)	Hold (Min)
Ā, Ē, C BUS	EA, EB, EC	1.6	+0.6
A, B, C, BUS	CLK, CLK EN	16.3	-2.0
F1, F2, F3, F4, F5	CLK, CLK EN	17.9	-0.9
SH7, SH0, A/L SHIFT SEL	CLK, CLK EN	8.7	-0.8
Cin	CLK, CLK EN	8.9	-0.2
EA, EB, EC (H→L EDGE)	CLK, CLK EN	17.0	-2.5
CLOCK EN (H→L EDGE)	CLK	4.4	+0.4

*See Figures 4 and 5 for test definitions and circuit

TABLE 8 — PROPAGATION DELAY (NANOSECONDS) 0 TO 70°C T_A (T_J NOT TO EXCEED 115°C)

Input	Output	Max
A, B, C BUS	Y OUTPUT, ZDH, ZDL, SIGN	17.9
EA, EB, EC	Y OUTPUT, ZDH, ZDL, SIGN	18.7
F1, F2, F3, F4, F5	Y OUTPUT, ZDH, ZDL, SIGN	19.6
SH7, SH0, A/L SHIFT SELECT	Y OUTPUT, ZDH, ZDL, SIGN	10.3
Cin	Y OUTPUT, ZDH, ZDL, SIGN	10.5
CLK, CLK EN	Y OUTPUT, SIGN	5.8
ALU/R SEL, ALU/R SIGN SEL	Y OUTPUT, SIGN	4.4
RESET	Y OUTPUT, SIGN	7.8
OUT EN	Y OUPUT, SIGN	5.4
A, B, C BUS	Cout 1, Cout 2, PG, GG	11.5
EA, EB, EC	Cout 1, Cout 2, PG, GG	13.0
F1, F2, F3, F4, F5	Cout 1, Cout 2, PG, GG	12.8
Cin	Cout 2	4.3
F1, F2, F3, F4, F5	OV1, OV2	17.3
A, B, C BUS	OV1, OV2	16.2
EA, EB, EC	OV1, OV2	17.5
Cin	OV1	9.5
A, B, C BUS	SH0, SH7	8.6
EA, EB, EC	SH0, SH7	9.5
F1, F2, F3, F4, F5	SHO, SH7	9.7

FIGURE 4 — SWITCHING WAVEFORMS

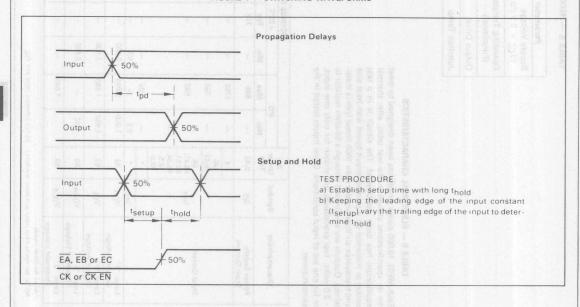


FIGURE 5 — SWITCHING TIME TEST CIRCUIT

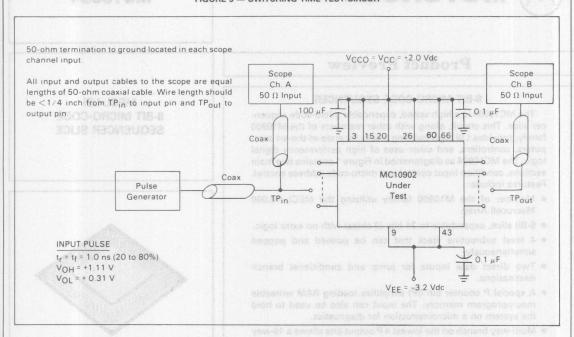
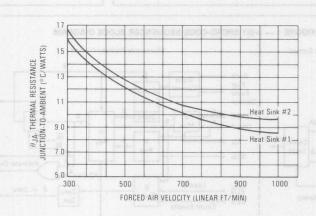


FIGURE 6 — THERMAL CHARACTERISTICS (TYPICAL)



Heat Sink #1 is from THERMALLDY #15832-1, 3 Horizontal Fins, 0.563 inches square, Model No. 2284C. Heat Sink #2 is from WAKEFIELD #4493, Vertical Fins, 0.5 inches square. NOTE: $T_J = (\theta_J A) (P_D) + T_A$ WHERE T_J is the Junction Temperature, T_A is the Ambient Temperature, $P_D = (I_{EE}) (V_{EE}) + (15 \text{ mW})$ (number of 50 Ω outputs).

Still air $\overline{\theta}$ JA (no heat sink) = 35°C/W.



MC10904

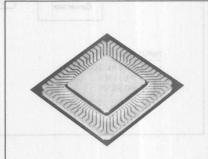
Product Preview

8-BIT MICRO-CODE SEQUENCER

The MC10904 is a high speed, expandable micro-code sequencer slice. This circuit, along with other members of the M10900 family, provides LSI logic building blocks for state-of-the-art computers, controllers, and other uses of high performance digital logic. The MC10904 as diagrammed in Figure 1 contains two main sections, condition input control and micro-code address control. Features include:

- Member of the M10900 family utilizing the MECL 10,000 Macrocell Array.
- 8-Bit slice, expandable to 24 bits (3 chips) with no extra logic.
- 4 level subroutine stack that can be pushed and popped simultaneously.
- Two direct data inputs for jump and conditional branch destinations.
- A special P counter pin (IP) simplifies loading RAM writeable macroprogram memory. The input can also be used to hold the system on a microinstruction for diagnostics.
- Multi-way branch on the lowest 4 P output bits allows a 16-way branch.
- Six branch condition inputs can be combined in 14 logic patterns to minimize external branch control logic.
- R register for holding microprogram address information.
- An 8-bit counter for repeating instructions or sequences. Can also be used to count events, conditions, or time.

MECL-LSI 8-BIT MICRO-CODE SEQUENCER SLICE

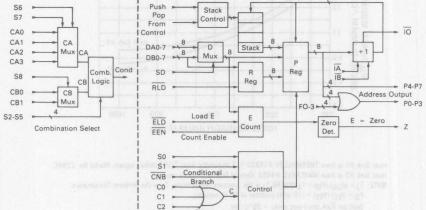


CASE 745 68 Pin, JEDEC Std. Leadless Package

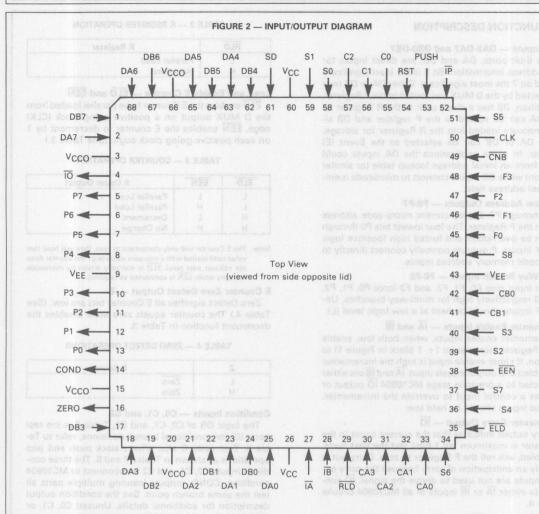
FIGURE 1 — 8-BIT MICRO-CODE SEQUENCER BLOCK DIAGRAM Condition Input Control Bush Bush 8

RST

CLK



Force P to Inc



ARCHITECTURAL DESCRIPTION

The M10900 family is a line of high performance standard digital LSI products designed around the MECL Macrocell Array. The MC10904 8-bit Micro-code Sequencer circuit controls a microprogram by generating microcode memory addresses, providing a means for sequencing through programs, and making micro-code conditional branch decisions. Each part is 8 bits wide and circuits are easily combined to meet microprogram memory size requirements.

The MC10904 P Register (Figure 1) holds the current micro-code address and supplies address information on outputs P0-P7. Next address is computed from inputs DA0-DA7, inputs DB0-DB7, and several points internal to the circuit including P Register incrementer, 4 deep subroutine stack, and the R Register. Select lines and conditional branch inputs control circuit op-

eration. The 4 bottom P address outputs are gated with force inputs F0-F3, thus providing 16-multiway branch capability.

Each MC10904 handles up to six condition inputs divided into groups of four (CA0-CA3), and two (CB0-CB1). One bit from each group can be used by itself or logically combined with a bit from the other group to determine branch condition status. For example, a single micro-code instruction could incorporate "branch if less than or equal" by having an ALU sign bit on one set of condition inputs and zero detect on the other, then with S2-S5 select "A or B" in the Conditional Combinational Logic. The six condition inputs expand with additional sequencer circuits. Two MC10904s can address 64K micro-code words and provide up to 12 conditional branch inputs.

PIN FUNCTION DESCRIPTION

Data Inputs - DA0-DA7 and DB0-DB7

Two 8-bit ports, DA and DB, are direct inputs for next address information. Bit 0 is the least significant bit and bit 7 the most significant. Either DA or DB may be selected by the D MUX and routed to the P Register. In addition, DB has a direct path to the R Register so that DA can be routed to the P register and DB simultaneously loaded into the R Register for storage. Either DA or DB can be selected to the Event (E) Counter. In some applications the DA inputs could come from an initial address lookup table (or similar function) while DB inputs connect to microcode memory next address field.

Program Address Outputs - P0-P7

P0 through P7 display current micro-code address held in the P Register. The four lowest bits P0 through P3 can be overridden and forced high (positive logic 1) by F inputs. P outputs normally connect directly to microcode memory address inputs.

Multi-Way Branch Inputs - F0-F3

Four input pins F0, F1, F2, and F3 force P0, P1, P2, and P3 respectively high for multi-way branches. Unused F inputs should be held at a low logic level (L).

Incrementer Enable Inputs — IA and IB

Incrementer enable inputs, when both low, enable the P Register incrementer (+ 1 block in Figure 1) to function. If either enable input is high the incrementer is disabled and output equals input. IA and IB are either connected to a previous stage MC10904 IO output or used as a control input to override the incrementer. Unused inputs should be held low.

Incrementer Carry Output - 10

Carry output indicates that the current count in the P register is maximum (all 1 bits) and the next cycle, if enabled, will roll the P Register to zero. Carry out is actually an anticipation of carry because the carry enable inputs are not used to derive the signal. $\overline{\text{IO}}$ connects to either $\overline{\text{IA}}$ or $\overline{\text{IB}}$ inputs of all MC10904 circuits above it.

Select D Input - SD

SD controls an 8-bit, 2-input multiplexer that selects either DA or DB inputs to an internal 8-bit bus. The bus goes to both the P Register and E counter. (See Table 1.) This bit is normally driven by the microcode memory.

TABLE 1 — SELECT DATA OPERATION

SD	Register/Counter Input
L	DA Input
H	DB Input

LOAD R REGISTER - RLD

RLD enables the R Register to be loaded from the DB inputs on a positive going clock, CLK, input. (See Table 2.)

TABLE 2 - R REGISTER OPERATION

RLD	R Register
L	Parallel Load
50 H 28	Hold Data

Load and Enable E Counter — ELD and EEN

ELD enables the E Counter to be parallel loaded from the D MUX output on a positive going clock (CLK) edge. EEN enables the E counter to decrement by 1 on each positive going clock edge. (See Table 3.)

TABLE 3 - COUNTER OPERATION

ELD	EEN	E Count Output
L	L	Parallel Load
L	Н	Parallel Load
Н	L	Decrement
Н	Н	No Change

Note: The E Counter will only decrement to zero, then will hold that value until loaded with a non-zero value (e.g., the counter does not rollover past zero). ELD is normally driven by microcode memory while EEN is connected as required.

E Counter Zero Detect Output — Z

Zero Detect signifies all E Counter bits are low. (See Table 4.) The counter equals zero state disables the decrement function in Table 3.

TABLE 4 - ZERO DETECT OPERATIONS

Z	E Counter
L	Zero
Н	Zero

Condition Inputs — C0, C1, and C2

The logic OR of C0, C1, and C2, Table 5 is the test point (C) for conditional branch decisions, refer to Table 6. Test node C also affects stack push and pop operations as shown in Tables 7 and 8. The three condition inputs C0, C1, and C2 interconnect to MC10904 condition, COND, outputs insuring multiple parts all test the same branch point. See the condition output description for additional details. Unused C0, C1, or C2 inputs should be held low.

TABLE 5 — CONDITION INPUT OPERATIONS

CO	C1	C2	C (Internal Test Point)
L	L	pargeral	m e dentro curant e m
Н	X	X	sting microcorp memory as
X	Н	X	gans for spacething through t
X	X	H	identificate conditional branch i

Conditional Branch Input — CNB

CNB selects between conditional branch and unconditional jump. A low (L) level on this input enables the MC10904 to test CO, C1, and C2 and determine the next P Register address. A high (H) level on CNB overrides the C inputs enabling a direct jump. (See Table 6.) CNB also affects stack push and pop operations as shown in Tables 7 and 8.

TABLE 6 - P REGISTER SOURCE CONTROL

S1	S1 S0		C*	Next P	Instruction		
a notional	a elgeked	X	X	P Incr	Increment		
a. Evgn th	BOR XHID B	Hos History	X	D Bus	Direct Jump		
ro n t o shu	got EH rins	est. F thro	Н	D Bus	Br. Cond. Met		
luovLinees!	F.autHuo S	InsoLingia	785.9) L	P Incr	Br. Cond. Failed		
onibHol as	is of nan	metHe to	X	R Reg	Direct Jump		
B Henry	neireLa be	districted as a	Н	R Reg	Br. Cond. Met		
Н	adi Las h	he in Liver	A costs L	P Incr	Br. Cond. Failed		
Н	H	Н	X	Stack	Direct Jump/Pop		
Н	Н	L	Н	Stack	Br. Cond. Met/Pop		
Н	Н	L	L	P Incr	Br. Cond. Failed		

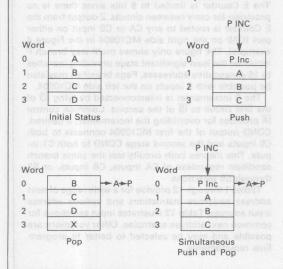
Branch Selection Inputs - S0 and S1

These two inputs are decoded to select a source for the next P Register address. The selection may be modified for conditional branch instructions as shown in Table 6. S0 and S1 also control stack operation as shown in Table 8. These bits are normally driven by microcode memory.

Stack Push Input - Push

When pushed, the incremented P count is written into the top of the stack and all previous stack contents are pushed down by one. There is no check for overflow on a stack push or underflow on stack pop. Simultaneous stack push and pop results when jumping or branching to the stack (Table 6) and asserting a PUSH command (Table 7). The stack is automatically popped on any stack to P Register transfer except simultaneous push and pop and does not require external control. Figure 3 illustrates the various stack operations. Note the simultaneous push/pop saves the previous stack top even though the system jumped to that address.

FIGURE 3 — MC10904 Stack Operation



Tables 7 and 8 define stack push and pop operation. Push is normally driven from microcode memory.

TABLE 7 - STACK PUSH OPERATION

CNB	C	Push	Stack Push	Instruction
X	X	L	No	No Stack Push
L	Н	Н	Yes	Push On Cond. Met
Н	X	Н	Yes	Push Always
L	L	Н	No	Push On Cond. Failed

TABLE 8 - STACK POP OPERATION

S1	SO	CNB	NB C Push Stack Pop		Stack Pop	Instruction				
L	L	X	X	X	No	Increment P				
L	H	X	X	X	No	Select D Bus				
H	L	X	X	X	No	Select R Register				
H	H	H	X	L	Yes	Jump to Stack				
H	H	L	H	L	Yes	Branch to Stack Cond. Me				
H	H	L	L	X	No	Branch to Stack Cond. Fail				
H	Н	H	X	H	No	Simultaneous Push Pop				
H	Н	L	Н	Н	No	Simultaneous Push Pop				

Condition A Inputs — CA0, CA1, CA2, CA3, S6 and S7

One of four external test conditions CA0–CA3 can be selected by S6 and S7 to an internal node, CA. (See Figure 1.) CA test selection is defined in Table 9.

TABLE 9 — CA CONDITION TEST POINT SELECTION

Г	S6	S7	CA Test Point
1	30	3/	CA Test Point
9	L	L	CA0
1	Н	L	CA1
3 0	E CHAR	H	CA2
	Н	Н	CA3

Condition B Inputs — CB0, CB1, and S8

One of two external test conditions CB0 or CB1 can be selected by S8 to an internal node, CB. CB test selection is defined in Table 10.

TABLE 10 — CB CONDITION TEST POINT SELECTION

S8	CB Test Point
bine & Lo Al au	CB0
Н	CB1

Conditional Branch Combination Logic Select — S2, S3, S4, and S5

S2 through S5 are decoded into 14 different logic selections. (See Table 11.) Final decoded condition selection is presented on the COND output. Table 11 uses CA and CB test points previously defined in tables 9 and 10.

TABLE 11 — CONDITION LOGIC COMBINATION SELECTION

S5	S4	S3	S2	COND
L	L	L	L	L
L	L	L	Н	CA
L	L	Н	L	CB
L	L	Н	Н	CA and CB
L	Hoo	Ta La	Form	CA or CB
L	H-VTO	mer soc	H	CA and CB
L	Н	Н	L	CA or CB
L	H	HAST	Н	-Ly anales
H	aita Litera	L	L	H Anna 1 o
H	L	L	Н	CA
Н	En Liber	Н	Low	CA CB
H	aued uou	Н	H	CA or CB
Н	H	L	L	CA and CB
H	H	Burne L	H	CA or CB
Н	Н	Н	L	CA and CB
Н	HTA	H S	H	H BURAT

Condition Output - COND

COND output is the result of selecting CA0 through CA3, CB0 or CB1, and logically combining the selections. The COND output of one MC10904 goes to a condition input C0, C1, or C2 of itself and other parallel MC10904 circuits. Three MC10904s would be interconnected by tying COND output of one to all three C0 inputs, COND output of the second to all C1 inputs, and COND output of the third to all C2 inputs.

Increment P Input - IP

The increment P register input is normally used to provide micro-code addressing at system start up when it is required to load read/write RAM micro-program storage. $\overline{\text{IP}}$ overrides all input controls except F0 through F3 inputs and Reset, causing the MC10904 to function in an Increment P Register mode only. A second $\overline{\text{IP}}$ function could be to halt system operation by forcing $\overline{\text{IP}}$ low and disabling the incrementer with $\overline{\text{IA}}$ and $\overline{\text{IB}}$ inputs. $\overline{\text{IP}}$ operation is shown in Table 12.

TABLE 12 - IP FORCED INCREMENT CONTROL

IP 80	P Register Operation
L	Increment P
Н	Normal

Note that if $\overline{\mathbb{IP}}$ is held low and the clock input (CLK) continues running and both $\overline{\mathsf{IA}}$ and $\overline{\mathsf{IB}}$ are low then the MC10904 will increment the P counter at the clock rate. To load a microcode memory from a slow data source either clock must be slowed or, $\overline{\mathsf{IA}}$ or $\overline{\mathsf{IB}}$ held high while accessing a new data word.

Reset - RST

Reset overrides all other inputs including \overline{IP} and forces the P Register to all logic low outputs (positive logic 0). Reset is a clocked function and operates on the positive going clock edge. Even though P Register is reset, F0 through F3 inputs can override the four least significant P outputs. Reset would be commonly used at system start up, after loading micro-code, to locate a predefined starting address. Reset also zeros the E counter and sets the microprogram stack to the first location. Reset is normally at a low logic level (L) and is taken high for reset.

Clock - CLK

All registers and counters are activated on a positive going (LOW to HIGH) clock edge.

APPLICATIONS INFORMATION

Two MC10904 circuits, interconnected as shown in Figure 4, generate up to 16-bit micro-code addresses. The right side MC10904 handles the 8 least significant bits and the left side up to 8 most significant bits. Not using all 8 most significant bits adapts the circuit to microprogram memory size.

Parallel address paths DA and DB go to both circuits with least significant address bits going to the right side MC10904. DA and DB inputs normally require the same number of bits as P micro-code address outputs. Control signals are divided into three groups as shown in Figure 4. Common controls go to the same input on both circuits. Common controls handle data transfers and subroutine stack operations, thus insuring both parts perform the same next address function. Each MC10904 also requires separate control inputs, primarily for selecting branch decision test points.

Separate controls on the least significant MC10904 operate the E Counter through ELD and EEN inputs. The E Counter is limited to 8 bits since there is no provision for carry between circuits. Z output from the E Counter is routed to any CA or CB input on either part (CA0 on the right side MC10904 in the Figure 4 example). The figure only shows multi-way branch F inputs on the least significant stage providing branches to 16 consecutive addresses. Page branches may also be possible with F inputs on the left side MC10904.

The P incrementer is interconnected by tying $\overline{\text{IO}}$ of the first circuit to $\overline{\text{IB}}$ of the second. Common control $\overline{\text{IA}}$ provides for overriding the incrementer, if desired. COND output of the first MC10904 connects to both C0 inputs and the second stage COND to both C1 inputs. This insures both circuits test the same branch condition regardless of CA inputs, CB inputs, or S2 through S8 selections.

Tables 1 through 12 provide for a wide range of next address sequence instructions and various address input sources. Table 13 illustrates input selections for common next address examples. Other variations are possible and may be selected to better fit program flow requirements.

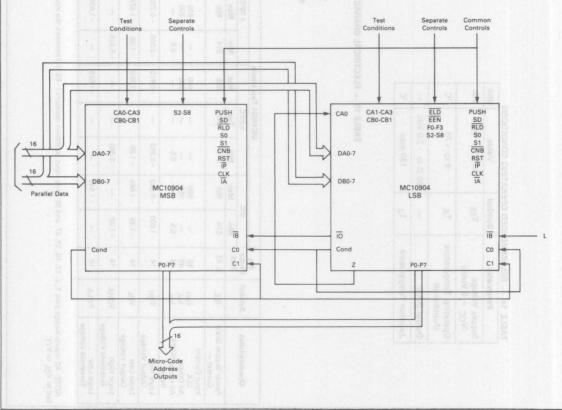
for all conditional branch decisions. Most of the instructions are self explanatory and source selections between DA, DB, and R Register are more for programming example than system architecture. Instruction 9 loads the E Counter to set up a repeat instruction sequence. The repeat is shown in instruction 10 where the microprogram would continue executing the com-

is easily accomplished with condition combinational logic (Table 11). Repeating a given subroutine could be accomplished with the following commands: 1) Set E Counter, 2) Jump to Subroutine, 3) Decrement the E Counter once during the subroutine, and 4) Return on Condition from Subroutine. Failure to return would cause a jump to subroutine start.

TABLE 13 — MC10904 SEQUENCE INSTRUCTION EXAMPLES

	SD	RLD	ELD	EEN	S1	SO	CNB	PUSH	C	INSTRUCTION
1	X	Н	Н	н	L	L	X	L	X	INCREMENT
2	Н	Н	Н	н	L	Н	Н	L	X	JUMP TO DB BUS
3	L	L	H	н	L	Н	Н	L	X	JUMP TO DA BUS, DB BUS TO R REG
4	X	Н	H	н	Н	L	L	L	C	CONDITIONAL BRANCH TO R REG
5	L	Н	Н	H	L	Н	Н	H	X	JUMP TO SUBROUTINE AT DA BUS
6	X	Н	H	н	Н	Н	Н	L	X	RETURN FROM SUBROUTINE
7	Н	Н	Н	H	L	Н	L	Н	C	COND. BRANCH TO SUBROUTINE AT DB
8	X	Н	Н	Н	Н	Н	L	Lo	C	COND. RETURN FROM SUBROUTINE
9	L	Н	L	H	1L	L	X	L	X	INCREMENT, DA TO E COUNTER
10	X	H	Н	L	Н	L	L	L	Z	JUMP TO R UNTIL E COUNT = ZERO

FIGURE 4 — 16 BIT MICRO-CODE SEQUENCER EXAMPLE



Parameter	Symbol	Value	Unit	
Supply Voltage (V _{CC} = 0 Volts)	VEE	-4.68 to -5.72	Vdc	
Operating Temperature (Functional)	ТА	0 to +70	°C	
Output Drive		50 Ω to -2.0 Vdc	-	
Junction Temperature	TJ	130 max	°C	

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table (Table 15), after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 1000 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs tested in the same manner.

TABLE 15 — ELECTRICAL CHARACTERISTICS

- 6	Test Voltage Values											
@ Test	Volts											
Temperature	VIH max	VIL min	VIHA min	VILA max	VEE							
0°C	-0.840	-1.95	-1.145	- 1.490	-5.2							
+ 25°C	-0.810	-1.95	-1.105	- 1.475	-5.2							
-70°C	-0.720	-1.95	-1.045	- 1.450	-5.2							

	The second second			C. Luciania						-700	-0.720	-1.55	-1.045	1.450	- 5.2		
		Pin			N	AC10904	Test Limits						181	- E	3 6	2,3,3	
Characteristics	Symbol	Symbol	Under	0°C			+25°C			+70°C			Voltage Applied to Pins Listed Below				(Vcco)
		Test	Min	Max	Min	Тур	Max	Min	Max	Unit	VIH max	VIL min	VIHA min	VILA max	VEE	Gnd	
Power Supply Drain Current —	IEE	9, 43	514	855	514	685	855	514	855	mAdc	L Z z :	X TL3	25	# - # J	9, 43	3, 15, 20 26, 60, 66	
Input Current CLK All Others All except NOTE below	linH linL linL	50 49 49	 0.5	600 250	 0.5		600 250	— 0.5	600 250	μAdc	50 49 —	49	TO 123	Collette 42 -	dastiriona associationa	di ei sult	
Logic High Output Voltage	VOH	14	-1.000	-0.840	-0.960		-0.810	-0.905	-0.730	Vdc	51	36, 39, 40	EZ	outo	Part I		
Logic Low Output Voltage	VOL	14	- 1.95	- 1.665	- 1.95	50	- 1.650	-1.95	- 1.625	Vdc	36, 39, 40	51	TES	-8	8 6		
Logic High Threshold Voltage	VOHA	14	-1.02	8	-0.980		dia	- 0.925	-	Vdc	X S X S	36, 39, 40	51	- 000	STORE STORE	1995	
Logic Low Threshold Voltage	VOLA	14	-	-1.645		-	-1.630	-	-1.605	Vdc	36, 39, 40	1.02 (5.07.0	190.4	51			

NOTE: All inputs except pins 1, 2, 17, 18, 19, 67, and 68 have input pulldown resistors (-68 kΩ) between the input and VEE. These 7 inputs, if unused, must be tied to VOL or VTT.

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Switching Characteristics Over Operating Voltage and Temperature Range

Tables 16 and 17 define timing characteristics of the MC10904 over operating voltage and temperature ranges. Worst-case Setup and Hold and Propagation Delays are calculated for $V_{EE}=-5.2$ volts \pm 10% and a $T_{J}max=115^{\circ}C$. The maximum recommended operating junction temperature is \pm 130°C.

TABLE 16 — SETUP AND HOLD TIMES (NANOSECONDS)

0° to 70°C T_A (T_J not to exceed +115°C)

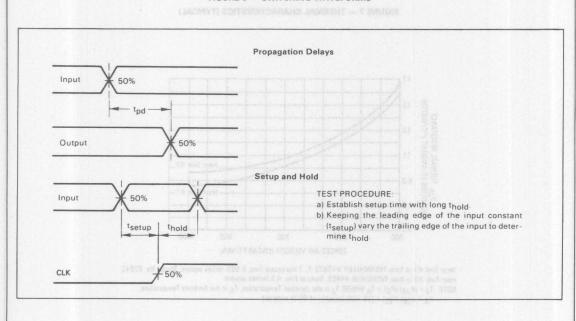
From	То	Setup (Min)	Hold (Min)
DA BUS, DB BUS	CLOCK	1.0	9.0
PUSH, SD, RLD, ELD, EEN	CLOCK	4.0	7.0
ĪĀ, ĪB	CLOCK	4.6	2.0
S0, S1, CNB	CLOCK	2.0	8.0
C0, C1, C2	CLOCK	2.0	8.0
IP, RST	CLOCK	2.5	8.0

Calculated limits are based on several performance factors as described in Motorola's Preliminary Design Manual for the MECL 10,000 Macrocell Array. Factors include worst case delays due to Macro selections, Fan-Out, Metal Lengths, Wire-OR, and Input Follower options. AC measurements are performed on each device to assure process integrity; however, Motorola does not guarantee limits at this time.

TABLE 17 — PROPAGATION DELAY (NANOSECONDS)
0° to 70° T_A (T_J not to exceed +115°C)

Input	Output	Тур	Max
CLOCK	P4-P7	9.1	14.0
CLOCK	P0-P3	9.1	14.0
CLOCK	ĪŌ	11.1	17.0
CLOCK	Z	15.7	24.0
F0-F3	P0-P3	2.9	4.5
S2-S5	COND	6.5	10.0
S6-S8	COND	7.2	11.0
CA0-3, CB0-1	COND	6.9	10.5

FIGURE 5 — SWITCHING WAVEFORMS



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FIGURE 6 — SWITCHING TIME TEST CIRCUIT

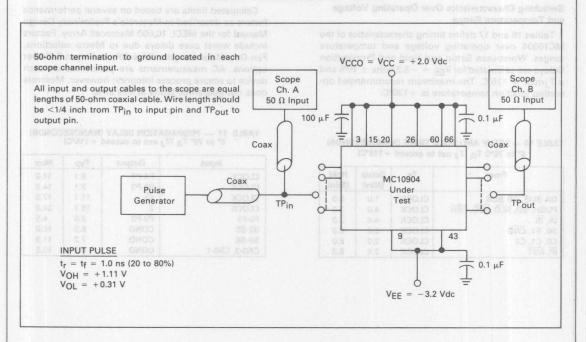
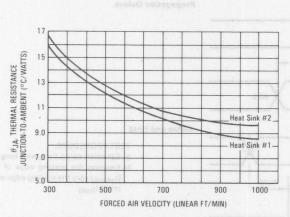


FIGURE 7 — THERMAL CHARACTERISTICS (TYPICAL)



Heat Sink #1 is from THERMALLOY #15832-1, 3 Horizontal Fins, 0.563 inches square, Model No. 2284C. Heat Sink #2 is from WAKEFIELD #4493, Vertical Fins, 0.5 inches square. NOTE: $T_J = (\theta_JA) (P_D) + T_A$ WHERE T_J is the Junction Temperature, T_A is the Ambient Temperature, $P_D = (I_{EE}) (V_{EE}) + (15 \text{ mW})$ (number of 50 Ω outputs).



MC10905

Advance Information

16-BIT EXPANDABLE ERROR DETECTION AND CORRECTION UNIT

The MC10905 is a high speed 16-bit error detection and correction unit that is easily expandable to handle up to 96 data bits. The unit is designed to improve the reliability of memory systems by detecting and correcting any single bit error while detecting all double bit errors and some multiple bit errors. A high speed pipelined architecture is an important feature providing separate input and output data ports which improves the performance and simplifies the system design.

- High Speed Pipelined Architecture.
- On-Chip Latches for Input Data, Check Bits, Output Data, and Error Flags.
- · Separate Input and Output Data Ports.
- Expandable to 96 Bits.
- Full Single Error Correction and Double Error Detection.
- During a Read or Check Mode, Data Correction Can Be Disabled While Checking for Errors.
- Very Fast Error Detect

For 16 Bits, 17.2 ns Max.

For 32 Bits, 21 ns Max.

For 48 through 96 Bits, 28.2 ns Max.

Very Fast Data Correct

For 16 Bits, 19.7 ns Max.

For 32 Bits, 28 ns Max.

For 48 through 96 Bits, 31.3 ns Max.

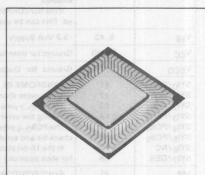
Very Fast Check Bit Generate

For 16 Bits, 10.7 ns Max.

For 32 Bits, 17 ns Max.

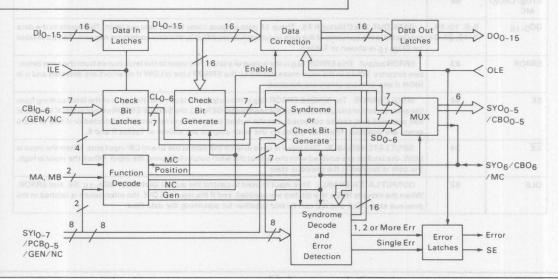
For 48 through 96 Bits, 17.8 ns Max.

MECL-LSI
16-BIT EXPANDABLE
ERROR DETECTION AND
CORRECTION UNIT



CASE 745 68 Pin, JEDEC Std. Leadless Package

BLOCK DIAGRAM - FIGURE 1

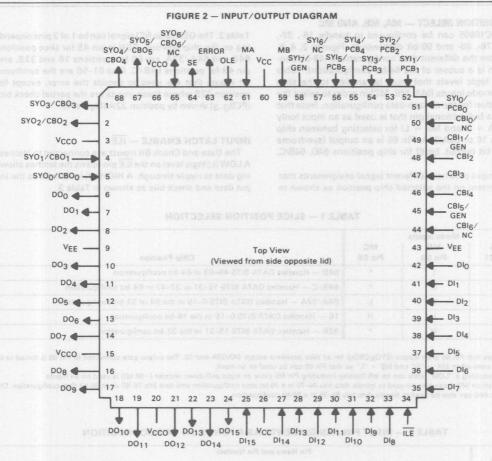


This document contains information on a new product. Specifications and information herein are subject to change without notice.

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Pin Assignments and Definitions (See Figure 2.)

Pin Name	Number	Definition and Description
DI ₀₋₁₅	42-35, 33-27, 25	DATA IN, bits 0 through 15: These 16 data inputs are connected to a data input latch which is then used in error detection and/or correction, and for generating check bits.
CBI _O /NC CBI ₁ /GEN CBI ₂ CBI ₃ CBI ₄ CBI ₅ /GEN CBI ₆ /NC	50 49 48 47 46 45 44	CHECK BITS IN/NO CORRECTION/GENERATE: These input pins can serve one of three functions depending on the selected slice position as described in Table 2. As an example, for slice position 32B, these input pins are all used to input the check bits. For slice position 64A/32A, the first five pins are "don't cares" while pin 45 is GENERATE. Pin 44 is NO CORRECTION. The Check Bits are connected to an input latch which is then used to help generate the syndrome bits used in error detection. (See Table 4). The GENERATE pin when a HIGH selects the generate check bit mode and when a LOW selects the read mode for error checking and/or correction of the input data and check bits. The NO CORRECTION pin, when HIGH during the read mode (GEN = L), disables the data correction while continuing to check for errors. When the pin is LOW during the read mode, the data correction circuitry is enabled. If the NO CORRECTION pin is HIGH when the GENERATE pin is HIGH, the diagnostic write mode is selected. This can be used to check the error detection and correction circuitry of the MC10905.
VEE	9, 43	-5.2 Volt Supply Anusarida A benissin besse dgill •
Vcc	26, 60	Ground for Internal Logic
Vcco	3, 15, 20, 66	Ground for Output Drivers
SYI ₀ /PCB ₀ SYI ₁ /PCB ₁ SYI ₂ /PCB ₂ SYI ₃ /PCB ₃ SYI ₄ /PCB ₄ SYI ₅ /PCB ₅ SYI ₆ /NC SYI ₇ /GEN	51 52 53 54 55 56 57 58	SYNDROME IN, bits 0-7/PARTIAL CHECK bits 0-5/NO CORRECTION/GENERATE: These input pins perform more than one function depending on the selected slice position (as described in Table 2). The SYI ₀₋₇ pins are used to input the syndrome bits (for slice positions 64D, 64B/C, and 64A/32A) for decoding the error status and correcting the single data bit errors. (See Tables 6c, d, and e.) The PCB ₀₋₅ pins are used in the 32-bit data configuration by slice 32B in order to generate the complete check bit and syndrome bit information (See Table 4 and Figure 4.) In the 16-bit slice position, pins 51-56 are don't care conditions. Pin 57 is NC and pin 58 is the GEN signal for slice positions 16 and 32B. The NC and GEN signal definitions are described above.
MA MB SYO ₆ /CBO ₆ / MC	61 59 65	SLICE POSITION MODE SELECT: These pins are used to select the slice position as shown in Table 1. Pin 65 is a bidirectional pin that is used as an input (when MA = H and MB = L) for selecting between slice position 16 or $64A/32A$. Pin 65 is an output (syndrome or check bit output, bit 6) for slice position $64D$, $64B/C$, and $32B$.
SYO ₀ /CBO ₀ SYO ₁ /CBO ₁ SYO ₂ /CBO ₂ SYO ₃ /CBO ₃	5 4 2 1	SYNDROME OUTPUT/CHECK BIT OUTPUT: When GEN $\stackrel{.}{=}$ L, the syndrome output appears at these pins, and when GEN $\stackrel{.}{=}$ H, the generated check bits appear. The truth table for these outputs is shown in Table 4. Note that pin 65 is used as a slice position input (MC) when MA $\stackrel{.}{=}$ H and MB $\stackrel{.}{=}$ L.
SYO ₄ /CBO ₄ SYO ₅ /CBO ₅ SYO ₆ /CBO ₆ / MC	68 67	For 32 Bits, 17 ns Mayo For 48 through 96 Bits, 17,8 ns Max. Budok 5
DO ₀₋₁₅	6-8, 10-14, 16-19, 21-24	DATA OUT, bits 0 through 15: These 16 data outputs come from a data out latch. The inputs to the data out latch are the contents of the data input latch as modified by the data correction network. The truth table for DO ₀₋₁₅ is shown in Table 5.
ERROR	63	ERROR output: This ERROR flag is the output of a latch. The input to the latch comes from the error detection circuitry. When in the read mode (GEN = L), the ERROR Line is LOW if no errors are detected and it is HIGH if one or more errors are detected.
SE a_gora a_gora	64	SINGLE ERROR: The SINGLE ERROR flag is the output of a latch with the input of the latch coming from the error detection circuitry. When in the read mode (GEN = L), the SINGLE ERROR output is HIGH if an error has occurred that can be corrected, and the output is low if no error has been detected or if two or more errors are detected. The truth tables for the error outputs are shown in Tables 5 and 6.
BOBDASOYS	34	INPUT LATCH ENABLE: This input is used to latch the data at the DI and CBI input pins. When the input is LOW, the latches are enabled with the data at the latch output following the input. When the input is high, the data is latched in the previous state.
OLE	62	OUTPUT LATCH ENABLE: This input is used to control the output latches for DO_{0-15} , SE, and ERROR. When the input is HIGH, the latches are enabled, and if the input is LOW, the information is latched in the previous state. OLE and $\overline{\text{ILE}}$ can be tied together for pipelining the data flow.



ARCHITECTURAL DESCRIPTION

The M10900 family is a line of high performance standard digital LSI products designed around the MECL Macrocell Array. The MC10905 provides an error detection and correction unit (EDCU) between the memory and the CPU that improves system reliability by virtually eliminating system downtime due to memory errors without sacrificing performance. For high speed memory systems it is important that the EDCU be as fast as possible since the delay for detecting errors can add directly to the memory access time.

The dual bus, pipelined architecture (Figure 1) of the MC10905 simplifies system design, reduces the part count, and provides the fastest EDCU on the market. A master-slave data transfer can be accomplished by connecting the latch enables (ILE and OLE) together. Error logging can be accomplished by monitoring the syndrome output. Catastrophic memory failures (all 1's or 0's) are also detected. A diagnostic write mode is a special feature which can be used to test the error checking of the MC10905.

In most high performance memory systems, separate MC10905 configurations will be used for writing and reading data to and from memory using separate input and

output data buses. Bidirectional data buses slow the performance of high speed memory systems by requiring additional components in the data path such as multiplexors and buffers, and complicating transmission line terminations.

FUNCTIONAL DESCRIPTION

* The MC10905 uses a modified Hamming code that allows single error correction with single and double error detection. When writing data to memory, check bits are generated by the MC10905 from selected bits of the data word and stored in memory along with the data word. For a 16-bit wide data word, 6 check bits are required, while 32-bit and 64-bit data words require 7 and 8 check bits respectively. When reading the data from memory, the MC10905 regenerates the check bits and exclusive OR's them with the check bits read from memory producing syndrome bits. If the syndrome bits are all LOW, no errors are detected. If one or more of the syndrome bits are HIGH, an error has been detected. The syndrome bits identify the bit-in-error for single errors, all double errors, and some multiple errors. If a single data bit is in error, the data correction logic inverts this bit (if NC = 0), thus correcting the data word.

The MC10905 can be configured to handle 16-, 32-, 48-, 64-, 76-, 88- and 96-bit data words. Figures 3, 4, 5, and 6 show the different data configurations (48-bit configuration is a subset of the 64-bit configuration). Table 1 shows logic levels that must be applied to the slice position mode inputs (MA, MB, MC) in order to select the chip position for the chosen data configuration. Note that Pin 65 is a bidirectional pin that is used as an input (only when MA = H and MB = L) for selecting between chip positions 16 or 64A/32A. Pin 65 is an output (syndrome or check bit output, bit 6) for chip positions 64D, 64B/C, and 32B.

Some input pins have different signal assignments that are dependent on the selected chip position as shown in

Table 2. The GEN (also NC) signal can be 1 of 3 pins depending on the chip position. GEN is pin 45 for slice positions 64D and 64A/32A, pin 58 for positions 16 and 32B, and pin 49 for positions 64B/C. Pins 51-56 are the syndrome bit inputs that are used to decode the error, except for position 32B where these inputs are the partial check bits (PCB_{O-5}) driven by position 32A (Figure 4).

INPUT LATCH ENABLE - ILE

The Data and Check Bit inputs are connected to latches. A LOW (L) logic level on the ILE pin opens the latches allowing data to ripple through. A HIGH (H) level latches the input data and check bits as shown in Table 3.

TABLE 1 - SLICE POSITION SELECTION

	Mode Inputs		
MA Pin 61	MB Pin 59	MC Pin 65	bit missour para ment bewerter Chip Position
L	L		64D — Handles DATA BITS 48-63 in 64-bit configuration
L	120 -H 15		64B/C — Handles DATA BITS 16-31 or 32-47 in 64-bit configuration.
Н	giū (5) (5)	L	64A/32A — Handles DATA BITS 0-15 in the 64 or 32-bit configuration.
Н	gioLos en	Н	16 — Handles DATA BITS 0-15 in the 16-bit configuration.
Н	H		32B — Handles DATA BITS 16-31 in the 32-bit configuration.

NOTES

- 1. *indicates that Pin 65 is an output (SYO₆/CBO₆) for all slice positions except 64A/32A and 16. The output gate connected to Pin 65 is forced to the "LOW" state when MA = "H" and MB = "L" so that Pin 65 can be used as an input.
- 2. Inputs requiring a "LOW" state can be left floating (including Pin 65) since an input pull-down resistor (~68 kΩ) is used on all inputs.
- 3. Chip position 64B/C can also be used to handle data bits 64–75 in a 76-bit data configuration and data bits 76–87 in an 88-bit data configuration. Chip position 64D can also be used to handle data bits 88–95 in a 96-bit configuration.

TABLE 2 - INPUT PIN ASSIGNMENTS AS A FUNCTION OF SLICE POSITION

Slice				Pii	n Name an	d Pin Number				
Position (See Table 1)	CBI _O /NC 50	CBI ₁ /GEN 49	CBI ₂	CBI ₃	CBI ₄	CBI ₅ /GEN 45	CBI ₆ /NC	SYI ₀₋₅ /PCB ₀₋₅ 51-56	SYI6/NC 57	SYI7/GEN 58
64D	CBIO	CBI ₁	CBI ₂	CBI ₃	CBI ₄	GEN	NC	SYI ₀₋₅	SYI ₆	SYI ₇
64B/C	NC	GEN	X	X	X	CBI ₅	CBI ₆	SYI ₀₋₅	SYI ₆	SYI7
64A/32A	X	X	X	X	X	GEN	NC	SYI ₀₋₅	SYI ₆	SYI ₇
16	CBIO	CBI ₁	CBI ₂	CBI ₃	CBI ₄	CBI ₅	X	X	NC	GEN
32B	CBIO	CBI ₁	CBI ₂	CBI ₃	CBI ₄	CBI ₅	CBI ₆	PCB ₀₋₅	NC	GEN

NOTES:

- 1. "X" is a don't care condition, Input is not used.
- 2. For position 32A, Pin 58 must be left open or connected to a VOL voltage.
- 3. In the generate check-bit mode (GEN = H), the SYI; inputs are not used for slice positions 64D, 64B/C and 64A/32A. The CBI; inputs are also not used; however, the input check-bit latches are functional.

ODEC TABLE 3 — TRUTH TABLE FOR INTERNAL DATA IN AND CHECK BIT LATCHES

ILE	Internal Lat	Internal Latch Outputs								
(Pin 34)	DL ₀₋₁₅	CL ₀₋₆								
L STATE OF THE STA	DI ₀₋₁₅	CBI ₀₋₆								
H. H. Starter	alonia sal — storan	no semplos de								

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- 10 by 816 and grades and 16 and 1, denotes NO CHANGE. Outputs are latched. The problem is problem and state of state of the state of
 - 2. Latches are enabled when ILE = "L"

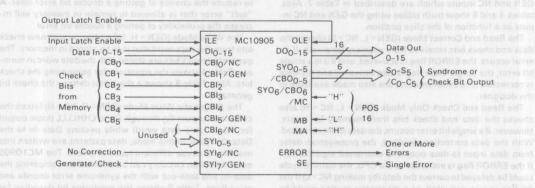
	(See Ta	Inp	(See Table 1)			Syndror	ne or Check Bit	Outputs		
Operating Mode	GEN	NC NC	Slice Positions	(Pin 5) SYO ₀ /CBO ₀	(Pin 4) SYO ₁ /CBO ₁	(Pin 2) SYO ₂ /CBO ₂	(Pin 1) SYO ₃ /CBO ₃	(Pin 68) SYO ₄ /CBO ₄	(Pin 67) SYO ₅ /CBO ₅	(Pin 65) SYO ₆ /CBO ₆
Write Mode.	Н	L	64D	PO	P1 -	P2	P3	P4	P5A	P6
Generate	China		64B/C	PO	P1	P2	P3	P4	P5B	P6
Check Bits	1		64A/32A	PO	P1	P2	P3	P4	P5A	8.6-0
			16	PO PO	P1	P2	P3	P4	P5A	
			32B	PO ⊕ PCB _O	P1 ⊕ PCB ₁	P2 ⊕ PCB ₂	P3 ⊕ PCB ₃	P4 ⊕ PCB ₄	P5B ⊕ PCB ₅	P6
Diagnostic	Н	Н	64D	E O en	L	E) one	L	L	L	L
Write Mode. Initialize Check Bits			64B/C, 64A/32A, 16, 32B	L	н	F-H RM	N PDS {	Selenic	L	Chigot
Read Mode.	L	×	64D	PO ⊕ CL _O	P1 ⊕ CL ₁	P2 ⊕ CL ₂	P3 ⊕ CL ₃	P4 ⊕ CL ₄	P5A	P6
Check Data			64B/C	PO	P1	P2	P3	P4	P5B ⊕ CL ₅	P6 ⊕ CL6
and Check Bits			64A/32A	PO	P1	P2	P3	P4	P5A	L
and Generate			16	PO ⊕ CLO	P1 ⊕ CL ₁	P2 ⊕ CL ₂	P3 ⊕ CL ₃	P4 ⊕ CL ₄	P5A ⊕ CL ₅	
Syndrome Bits	3	81	328	PO ⊕ PCB _O ⊕ CL _O	P1 ⊕ PCB ₁ ⊕ CL ₁	P2 ⊕ PCB ₂ ⊕ CL ₂	P3 ⊕ PCB ₃ ⊕ CL ₃	P4 ⊕ PCB ₄ ⊕ CL ₄	P5B ⊕ PCB ₅ ⊕ CL ₅	P6 ⊕ CL ₆

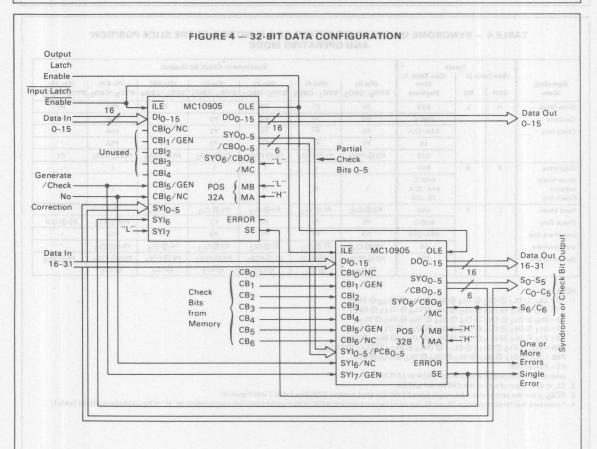
NOTES:

- 1. PO = DL₀ \oplus DL₁ \oplus DL₂ \oplus DL₄ \oplus DL₆ \oplus DL₈ \oplus DL₁₀ \oplus DL₁₂ P1 = DL₀ \oplus DL₁ \oplus DL₃ \oplus DL₅ \oplus DL₇ \oplus DL₉ \oplus DL₁₁ \oplus DL₁₃
 - P2 = DLO + DL2 + DL3 + DL4 + DL5 + DL8 + DL9 + DL14
 - P3 = DL1 + DL2 + DL3 + DL6 + DL7 + DL10 + DL11 + DL15
 - P4 = DL4 + DL5 + DL6 + DL7 + DL12 + DL13 + DL14 + DL15
 - P5A = DL8 + DL9 + DL10 + DL11 + DL12 + DL13 + DL14 + DL15
 - $\mathsf{P5B} = \mathsf{DL}_0 \oplus \mathsf{DL}_1 \oplus \mathsf{DL}_2 \oplus \mathsf{DL}_3 \oplus \mathsf{DL}_4 \oplus \mathsf{DL}_5 \oplus \mathsf{DL}_6 \oplus \mathsf{DL}_7$ P6 = P5A ⊕ P5B

 - where DL; is the output of bit i of the DATA IN LATCH.
- 2. CLi is the output of bit i of the CHECK BIT LATCH.
- 3. PCB₀₋₅ are the partial check bit inputs (pins 51-56) for slice position 32B (See Table 2 and Figure 4).
- 4. * indicates that for slice position 16, pin 65 is a slice position mode input (MC) that must be externally connected to an "H" or VOH voltage level (see Table 1).

FIGURE 3 — 16-BIT DATA CONFIGURATION





OPERATING MODES - GEN, NC

Four different operating modes can be selected with the GEN and NC inputs which are described in Table 7. Also, tables 4 and 5 show truth tables using the GEN and NC inputs as a function of the slice position.

The Read and Correct Mode (GEN = L, NC = L) checks the data and check bits received from memory for errors. If an error occurs, the ERROR flag is activated, and if it is a single bit error, the Single Error flag is also activated and the data is corrected. The syndrome bits are also made available to the designer.

The Read and Check Only Mode (GEN = L, NC = H) also checks the data and check bits from memory for errors. However, if a single bit error occurs, the data is not corrected. With the data correction disabled, the propagation delay from data input to data output is shortened significantly. If the ERROR flag is activated to the CPU, the current cycle could be delayed to correct the data (by making NC = L) if the SE flag is also activated, or a diagnostic routine could be initiated. If a single bit error is detected, the corrected data

should be rewritten into the same memory location in order to reduce the chance of getting a double bit error later. A "soft" error that is allowed to remain in memory will increase the probability of getting a double bit error.

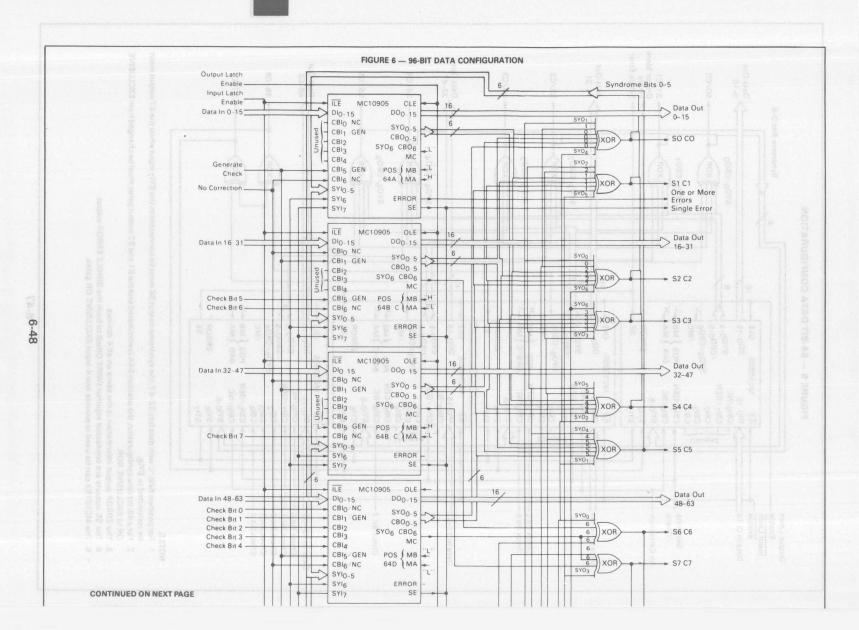
The Write Mode (GEN = H, NC = L) generates new check bits from the data word that is to be stored in memory. The generated check bits are stored with the data word in memory. Table 4 shows the equations for generating the check bits. Also, Table 8 shows a chart that defines the check bit generation.

The Diagnostic Write Mode (GEN = H, NC = H) forces the check bit outputs C_0 through C_7 to LHHLLLL (logic output for the all zero-data word) while passing Data-In to the Data-Out pins. In this mode, data patterns are written into memory to cause different types of errors. The MC10905 error detection circuitry can be checked by comparing the data-in and data-out with the syndrome error decode and error flags. Table 9 shows the syndrome bit decoding for the data configurations shown in Figure 3, 4 and 5.

FIGURE 5 -- 64-BIT DATA CONFIGURATION Output Latch Syndrome Bits 0-5 Enable Input Latch TLE MC10905 OLE Enable Data Out DO₀₋₁₅ Data In 0-15 DI0-15 0-15 CBIO/NC SYOO/CBOO SYO0-5 CBI1/GEN /CBO₀₋₅ CBI₂ XOR ► S0/C0 SYO6/CBO6 CBI3 /MC CBI4 Generate SYO1/CBO1 POS MB CBI5/GEN /Check CBI6/NC 64A MA H XOR ► S1/C1 SYI0-5 No Correction -One or More SYI6 ERROR Errors SE Single Error SYI7 ILE MC10905 OLE Data Out DI0-15 DO₀₋₁₅ Data In 16-31 16-31 CBIO/NC 6 SYO0-5 CBI1/GEN SYO2/CBO2 /CBO₀₋₅ CBI2 SYO6/CBO6 CBI3 XOR - S2/C2 /MC CBI4 CBI5/GEN Check Bit 5 POS MB SYO3/CBO3 Check Bit 6 CBI6/NC 64B/C MA SYIO-5 XOR - S3/C3 ERROR SYIE SYI7 SE ILE MC10905 OLE 16 DI₀₋₁₅ Data Out DO₀₋₁₅ Data In 32-47 32-47 CBIO/NC SY00-5 CBI1/GEN SYO4/CBO4 /CBO₀₋₅ CBI₂ SYO6/CBO6 CBI3 XOR - S4/C4 CBI4 /MC CBI5/GEN POS MB SYO5/CBO5 CBI6/NC Check Bit 7 64B/C MA SYI0-5 XOR - S5/C5 SYIA ERROR SE SY17 ILE MC10905 OLE > Data Out 48-63 Data In 48-63 DO₀₋₁₅ DI0-15 Check Bit 0 CBIO/NC SYO0-5 Check Bit 1 CBI1/GEN /CBO₀₋₅ CBI₂ Check Bit 2 SYO6/CBO6 XOR S6/C6 Check Bit 3 CBI3 /MC Check Bit 4 CBI₄ CBI5/GEN POS MB -L' 64D MA -L' XOR - S7/C7 CBI6/NC 64D (MA SYIO-5 SYI6 ERROR SYI7 SE

NOTES:

- For position 64B/C with data bits 32-47, the syndrome output S6 must be connected to the SYI7 input while the S7 output must be connected to SYI6.
- For a 48-bit data configuration, the position 64A is eliminated and the S1 and S2 output gates must be changed from EXCLUSIVE OR to EXCLUSIVE NOR.
- 3. The ERROR output information is the same on all 4 devices.
- 4. The SE outputs are connected together (WIRE ORed) to form the SINGLE ERROR output.
- 5. The MC10163 can be used to provide two 4-input EXCLUSIVE OR gates.



SYNDROME/CHECK BIT OUTPUTS -SYO0_6/CBO0_6

The logic equations for the syndrome or check bit outputs are shown in Table 4 as a function of the slice position and operating mode. These outputs contain the check bits during write to memory (GEN = H, NC = L). For a real cycle (GEN = L), these outputs contain the syndrome bits used for error identification. Table 8 shows a chart for check bit generation for various data configurations. Note that for data configurations of greater than 32 bits, exclusive OR gates must be used to generate the total syndrome or check bit field as shown in Figures 5 and 6. For the 32-bit data configuration (see Figure 4), the partial check bits generated by one MC10905 (32A) are passed to another MC10905 (32B) for generating the complete syndrome/check bit field without additional hardware.

The code used to generate the check bit patterns is based on the parity of selected data bits. An all LOW syndrome field indicates that no errors have been detected. If an even number of HIGH's occur in the syndrome field, a double error has been detected, while an odd number of HIGH's indicate a single error or multiple error has been detected. Table 9 shows the syndrome bit decoding.

Note that the generated parity (P1 and P2) is inverted on the SYO1/CBO1, and SYO2/CBO2 outputs for slice positions 16 and 64A/32A. This allows for the detection of catastrophic errors such as all 1's or 0's in the data and check bit field.

OUTPUT LATCH ENABLE — OLE

The internal data and error outputs are connected to latches. A HIGH (H) logic level on the OLE pin opens the latches allowing the information to flow through. A LOW (L) level latches the data and the SE and ERROR outputs as shown in Table 5.

DATA OUTPUT - DO0-15

The unmodified contents of the Data-In latches (DLO-15) are connected to the inputs of the Data-Out latches for all modes except when GEN = L and NC = L (check and correct data mode) as shown in Table 5. If the data is to be corrected (GEN = L and NC = L), the data correction network will invert any single bit error of the Data-In latch before placing it at the input of the Data-Out latch (see Tables 5 and 6).

SINGLE ERROR AND ERROR FLAGS - SE, ERROR

In the write mode (GEN = H), a LOW is forced on the inputs of the error flag latches as shown in Table 5. In the read mode (GEN = L), Table 6 defines the error flags for the various slice positions. The input to the ERROR latch is a LOW only if no errors are detected (data is valid) and it is a HIGH if one or more errors are detected. The input to the Single Error latch is HIGH only if a single bit error has been detected in the Data-In or Check Bit latches.

TABLE 5 — DATA OUT, SE, AND ERROR OUTPUTS AS A FUNCTION OF THE SLICE POSITION AND OPERATING MODE

Operating	SHARP OF AN	- M		PUTS	(See Note 2)	(See Table 1) Slice	0.0	OUTPUTS						
Mode	OLE	GEN	NC	SYI0-7	SD ₀₋₆	Position	DO ₀₋₁₅	SE	ERROR					
Output Latched	L	X	X	X	X	X	-	1-1	10 10 10					
WRITE Mode	Н	HA	X	X	X	X	DL ₀₋₁₅	3 L 5	3 3 L					
READ Mode	H	L	Н	X	See Table 6a	16	DL ₀₋₁₅	See 1	able 6a					
No Data Correction				Partial Check Bit Input	See Table 6b	32B	DL ₀₋₁₅	See 7	able 6b					
				See Table 6c	X	64A/32A	DL ₀₋₁₅	See 1	Table 6c					
				See Table 6d	X	64B/C	DL ₀₋₁₅	See 1	able 6d					
				See Table 6e	X	64D	DL ₀₋₁₅	See 7	Table 6e					
READ Mode	Н	L	L	X	See Table 6a	16	See Note 6	See 1	Table 6a					
Check and				Partial Check Bit Input	See Table 6b	32B	See Note 6	See T	able 6b					
Correct			5	See Table 6c	X	64A/32A	See Note 6	See 7	Table 6c					
Data				See Table 6d	X	64B/C	See Note 6	See 1	able 6d					
				See Table 6e	X	64D	See Note 6	See 1	Table 6e					

- 1. X = Input don't care Condition.
- 2. SD_{0-6} are the internal syndromes which are equal to the syndrome output SYO₀₋₆ (see Table 4). 3. Tables 6a-6e describe the outputs in the READ mode as a function of the syndrome bits.
- denotes NO CHANGE. Outputs are latched. Outputs are enabled when OLE = "H".
- 5. DL₀₋₁₅ is the output of the DATA IN latches.
- 6. If a single data bit error occurs (see tables 6a-6e), the data bit in error will be corrected (by inverting it) while the other 15 bits from DL₀₋₁₅ will appear unchanged at DO0-15

A single MC10905 will handle 16 data bits plus 6 check bits while two MC10905's will handle 32 data bits plus 7 check bits without additional hardware (see Figures 3 and 4). For the 64-bit configuration, four MC10905s are required, plus some additional exclusive OR (XOR) gates as shown in Figure 5. A 48-bit configuration can be generated from Figure 5 by eliminating the MC10905 in position 64A and changing the S1 and S2 output gates from XOR to XNOR (exclusive NOR). The MC10163, MC10107, MC10H107, or MC10H160 can be used to provide the XOR/XNOR functions.

Tables 7, 8 and 9 show the operating modes, the parity tree chart for the check bits, and the syndrome bit decoding, respectively. Table 10 was generated for use in calculating the delays of the important propagation delay paths for multi-chip data configurations. The maximum propagation delays specified in Tables 14 and 15 are used in these calculations.

TABLE 6 — TRUTH TABLES FOR BIT-IN-ERROR, AND THE SE AND ERROR OUTPUTS WHEN IN THE READ OR CHECK MODE (GEN = L)

(a) FOR SLICE POSITION 16

		SD ₅		L			Н			L			Н		-	L			н			L			н	
		SD ₄		L			L			н			н			L		7	L	-3.7		н			н	
		SD3	_	L		44.	L			- L			L			н	1000		н	100		Н			Н	
SD ₀	SD ₁	SD ₂	Bit In Error	SE	Error	Bit In Error	SE	Error	Bit In Error	SE	Error	Bit In Error	SE	Error	Bit In Error	SE	Error	Bit In Error	SE	Error	Bit In Error	SE	Error	Bit In Error	SE	Erro
L	L	L		L	L	CL ₅	н	н	CL ₄	н	н	-	2	н	CL3	н	н	-	L	н	-	L	н	DL ₁₅	н	н
L	L	н	CL ₂	н	н	-	L	н	- 4	L	н	DL14	н	н	-	L	н	-	L	н	15-	L	Н	-	L	н
L	н	L	CL ₁	н	н	-	L	н	-	L	Н	DL ₁₃	н	н	-	L	н	DL ₁₁	н	Н	DL7	н	н	-	L	н
L	н	н	-	L	н	DL9	н	н	DL ₅	н	н		L	н	DL3	н	н	-	L	н	-	L	н	-	L	н
н	L	L	CLO	н	н	-	L	н		L	н	DL ₁₂	н	н	-	L	н	DL10	н	н	DL ₆	н	н	-	L	н
н	L	н	-	L	н	DL ₈	н	н	DL ₄	н	н	-11	L	н	DL ₂	н	н	-	L	н	-	L	н	-	L	н
н	н	L	+	L	н	-	L	н	- 6	L	н	-11	L	н	DL ₁	н	н	-	L	н	-	L	Н	-	L	н
н	н	н	DLO	н	н	-	L	н	- 8	L	н	-11	L	н	-11	L	н	4	L	н	12	L	н	-	L	н

1. SD_i is the internal syndrome, bit i, which is equal to the syndrome output bit, SYO_i (see Table 4). NOTES

2 — = NO BITS ARE CORRECTED; DO₀₋₁₅ = DL₀₋₁₅
• = NO ERRORS

3. DL; = SINGLE BIT ERROR in the DATA-IN LATCH output, bit i. If NC = 0, data bit will be corrected by inverting it.

4. CL; = SINGLE BIT ERROR in the CHECK BIT LATCH output, bit i.

5. BIT IN ERROR specifies the single bit in error detected by the indicated slice position.

6. Unlisted input SYI combinations in tables 6c, 6d, and 6e perform no data correction, SE = "L", and ERROR = "H"

7. The SE and ERROR output latches (for Table 6) are enabled, OLE = "H"

(b) FOR SLICE POSITION 32b

			SD6		Н		-	н		1	Н			н			L			L		-	L			L	
			SD ₅		L	TE	-	L	170		Н		-	н		-	L	-	-	L		-	н			н	
			SD4		L	ni		н	nst.		L	145		н	99		L		-	н	- ns		L	m.		н	
SD ₀	SD ₁	SD ₂	SD ₃	Bit In Error	SE	Error	Bit In Error	SE	Error	Bit In Error	SE	Error	Bit In Error	SE	Error	Bit In Error	SE	Error	Bit In Error	SE	Error	Bit In Error	SE	Error	Bit In Error	SE	Erro
L	L	L	L	CL6	н	н	-	L	н	-	L	н	-	L	н		L	L	CL ₄	н	н	CL ₅	н	н	-	L	н
L	L	L	н	-	L	н	DL ₁₅	н	н	-	L	н	-	L	н	CL ₃	н	н	-	L	н		L	н	-	L	н
L	L	н	L	-	L	н	DL ₁₄	н	н	-	L	н	-	L	н	CL ₂	н	н	-	L	н	-	L	н	-	L	н
L	L	н	н		L	н		L	н	-	L	н	-	L	н		L	н	-	L	н	-	L	н		L	н
L	н	L	L	-	L	н	DL ₁₃	н	н		ι	н	-	L	н	CL ₁	н	н		L	н		L	н		L	н
L	н	L	н	DL ₁₁	н	н	-	L	н	-	L	н	DL7	н	н	-	L	н	-	L	н	-	L	н	-	L	н
L	н	н	L	DL ₉	н	н	-	L	н	-	L	н	DL ₅	н	н	-	L	н	-	L	н	-	L	н	-	L	н
L	н	н	н	-	L	н	-	L	Н	DL ₃	н	н	-	L	н	-	L	н	-	L	н	-	L	н	-	L	н
н	L	L	L	-	L	н	DL ₁₂	н	н	-	L	н	-	L	н	СГО	н	н	-	L	н	-	L	н	-	L	н
н	L	L	н	DL10	н	н	-	L	н	-	L	н	DL ₆	н	н	-	L	н	-	L	н	-	L	н	-	L	н
н	L	н	L	DL8	н	н	-	L	н	-	L	н	DL ₄	н	н	-	L	н	-	L	н	-	L	н	-	L	н
н	L	н	н	-	L	н	-	L	н	DL ₂	н	н	-	L	н	-	L	н	-	L	н	-	L	н	-	L	н
н	н	L	L	-	L	н	-	L	н	-	L	н		L	н	-	L	н	-	L	н	-	L	н		L	н
н	н	L	н	-	L	н	-	L	н	DL ₁	н	н	-	L	н	-	L	н	-	L	н	-	L	н	-	L	н
н	н	н	L	-	L	н	-	L	н	DLO	н	н		L	н	-	L	н	-	L	н	-	L	н	-	L	н
Н	н	н	н	-	L	н	-	L	н	-	L	н	-	L	н	-	L	н	-	L	н	-	L	н	-	L	н

viling and , sebom poistance and work of box 8. TABLE 6 - (continued) and a tox of court tow of 30 PO FAM by a stiff of the party of th

(c) FOR SLICE POSITION 64A/32

			SYI7	511974	L	J DETAIL	D ex	L		BREIN	L		31 471	L	abu ah	90 -	L	nous	antil	Н	a ma
			SYI6	0 41	L	96 L I	De:	L	NE SE	STEED	L		N PA	d fu	012/2/1	gras	Н	Grun	A. SEL	L	aren
			SYI5		L			L	E11(31)	ditta.	н	ni	ALM A	н	SUPACIE	SU	L	ill rus	ano i	L	2116
			SYI4		L			н			L			н			L			L	
SYIO	SYI ₁	SYI ₂	SYI3	Bit In Error	SE	Error	Bit In Error	SE	Error	Bit In Error	SE	Error	Bit In Error	SE	Error	Bit In Error	SE	Error	Bit In Error	SE	Error
L	L	L	L		L	L	CL ₄	н	н	CL ₅	н	н	-	L	н	CL ₆	н	н	CL7	н	н
L	L	L	н	CL ₃	н	н	0	L	н	-	L	н	DL ₁₅	н	н	14-	L	н	-	L	н
L	L	н	L	CL ₂	н	н	-	L	н	-	L	н	DL ₁₄	н	н	-	L	н	-	L	н
L	L	н	н	-	L	Н	-	L	Н	-	L	н	-	T	н	-	L	н	-	L	н
L	н	L	L	CL ₁	н	н	-	L	н	1-	L	Hall	DL ₁₃	н	н	-	L	н	1	L	н
L	н	L	Н	10313	L	Н	DL7	н	н	DL11	н	н	200	L	н	E _104	٠.٢	Н	el L e	L	н
L	н	н	L	.15	L	н	DL ₅	н	н	DLg	н	н	- "	L	н	- 1	L	н	1	L	н
L	н	н	н	DL3	н	н	.2	L	н	_81	L	н	-	L	н	1-1	L	н	-	L	н
н	L	L	L	CLO	н	н	25	L	н	-1	L	н	DL ₁₂	н	н -	-	L	н -	-	L	н
н	L	L	н	-4	U	н	DL ₆	н	н	DL10	н	н	- 11	L	н	- 1	L	н	-	L	н
н	L	Н	L	-	L	H	DL ₄	н	н	DL8	н	н	- M	L	н	- 7	L	н	-	L	н
Н	L	н	-н	DL ₂	н	н.		L	н	-97	L	н	- H	L	н	- 1	L	н	-	L	н
н	н	L	L	-	L	н		L	Had	-11	L	н	- 19	Ĺ	н	1-1	L	н	-	L	н
н	н	L	_H	DL ₁	н	H.	-1	L	н.	-91	L	н	- 10	L	н_	-	L	н	-	L	н
н	н	н	L	DLO	н	н	-	L	н	o litte	L	н	uā,	L	н		L	н	nie la	L	н
н	н	н	н	-	L	н	-	L	н	-	L	н	-	L	Н	t 7500	L	н	1093	L	н

(d) FOR SLICE POSITION 64B/C

			SYI7		L			L			L			L			L			L			L			Н	
			SYI6		н			н			н			Н	Tail.		L			L	14.3	C. 911	L	1000	200	L	
			SYIS		L			L			н			н			L			L			н	47 40		L	
			SYI4		L			н			L	200		н			L		2	н			L		aue	L	1
	evi	SYI2	ev.	Bit In Error	SE	Error	Bit In Error	SE	Error	Bit In Error	SE	Error	Bit In Error	SE	Error	Bit In Error	SE	Error	Bit In Error	SE	Error	Bit In Error	SE	Error	Bit In Error	CE	Erro
0.11	3111	3112									-		Error	-		e e e			-	-		-				-	
L	L	L	L	CL6	н	н	19317	L	н	700.00	L	н	10.00	L	Н	TOTAL	L	L	CL ₄	Н	Н	CL ₅	н	H	CL7	н	Н
L	L	L	н	-	L	н	DL ₁₅	н	н	-	L	н		L	н	Cr3	н	Н	-	L	н	-	L	н	-	L	н
L	L	Н	L	-1	L	Н	DL ₁₄	н	н	-	L	н	-	L	н	CL ₂	н	н	-	L	Н		L	Н	-	L	Н
L	L	н	н	-	L	н	-	L	н	-	L	н	-	L	н	-	L	н	-	L	н	-	L	н	-	L	н
L	н	L	L	_	L	н	DL ₁₃	н	н	-	L	н		L	н	CL ₁	н	н	-	L	н		L	н	-	L	н
L	н	L	н	DL ₁₁	н	н	-	L	н	-	L	н	DL7	н	н	-	L	н	-	L	н		L	н	-	L	н
L	н	н	L	DLg	н	н	-	L	н		L	н	DL ₅	н	н		L	н	-	L	н		L	н		L	н
L	н	н	н	-	L	н	-	L	н	DL ₃	н	н	-	L	н	-	L	н	-	L	н		L	н		L	н
н	L	L	L	-	L	н	DL ₁₂	н	н	-	L	н	- **	L	н	CLO	н	н	-	L	н	-	L	н		L	н
н	L	L	н	DL10	н	н	-	L	н		L	н	DL6	н	н	-	L	н	-	L	н		L	н	2	L	н
н	L	н	L	DL8	н	н		L	н	-	L	н	DL ₄	н	н		L	н		L	н		L	н	115	L	н
н	L	н	н		L	н	19	L	н	DL ₂	н	н		L	н		L	н		L	н	-	L	н		L	н
н	н	L	L		L	н		ı	н		L	н		L	н		L	н		L	н	-5-	L	н		L	н
н	н	L	н	-2	L	н			н	DL,	н	н	77	i.	н		L	н		L	н			н		L	н
н	н	н	L		L	н			н	DLO	н	н		L	н		L	н		L	н		L	н	121	L	н
н	н	н	н		ľ	н		L	н	10	L	н		L	н	77	L	н		L	н		1	н		L	н

TABLE 7 — OPERATING MODE SELECTION FOR 16, 32, 48, AND 64-BIT DATA CONFIGURATIONS

	Generate / Check	No Correction	Operating Mode and Description
ge	× L I ×	L 18	READ MODE. Check for errors, generate syndrome bits S0-S7, and correct single data bit errors.
×	38 L	⊕ H , ×	READ MODE. Check for errors, generate syndrome bits S0-S7, but do not correct single data bit errors.
30	Н	L	WRITE MODE. Generate check bits CO-C7, pass data through, and force inputs to the error latches to the "LOW" state.
t	8 5 5 8	H NO	DIAGNOSTIC WRITE MODE. Force the check bits C0 through C7 to a L H H L L L L respectively, pass data through, and force inputs to the error latches to the "LOW" state.

Bits	tion	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
C ₀	XOR	х	Х	X	-	X	-	X	_	X	-	X	-	X	_	_	_	X	Х	X	_	х	_	X	-	X	-	Х	_	X	_	-	_
C ₁	XNOR	X	X	_	X	_	X	_	X	_	X	_	X	-	X	_	_	X	X	_	X	-	X	-	X	-	X	_	X	-	X	_	-
C ₂	XNOR	X	-	Х	Х	X	х	_	_	х	Х	_	-	-	-	X	-	X	-	Х	Х	X	X	4	-	X	X	-	-	_	+	Х	-
C3	XOR	-	X	X	X	_	_	X	X	-	_	Х	X	-	-	_	X	-	X	X	X	-	-	X	X	+	+	X	X	-	1	+	X
C4	XOR	_	_	-	-	х	X	х	Х	_	-	_	-	X	X	X	X	_	_	_	-	X	X	X	X	-	+	_	_	X	X	×	X
C ₅	XOR	_	-	-	-	-	-	_	_	X	X	X	X	X	X	X	X	X	X	X	Х	X	X	X	X	+	#	+	-	4	+	1	-
C ₆	XOR	_		_	-	-	-	-	-	-	_	_	+	1	_	_		X	Х	Х	X	X	X	X	X	X	×	X	X	х	X	X	X
C7	XOR	_		-	_	-	_	_	_	_	_		T	12	13	18		_	1	-	3	-	1			1	1	1	_	_	1		1

Check		9		ë l	Po	sitio	n 64	B/C -	– Da	ta Ir	32-	-47	-		1	1	-				P	ositi	on 6	4D -	- Dat	a In	48-	63	-		1	1
Bits	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	6
C ₀	X	X	X	_	×	-	X	_	X	-	X	-	×	1	-		X	X	Х	-	×	-	X	-	×	+	X	-	×	+	-	-
C ₁	X	X	_	X	- 62	X	-	X	-	X	_	X	-	X	-	-	X	X	_	X	-	X	-	X	-	X	+	X	+	X	-	-
C ₂	X		X	X	X	X	-	_	X	X	-	+	-	-	X	E	X	-	X	х	X	X	4	-	X	X	F	-	-	_	X	
C3	-	X	Х	X	19	+	X	X	-	-	X	×	-	H	E	X	-	X	X	X	-	Н	X	X	+	Ŧ	X	Х	+	+	H)
C4	-	-	-	-	X	X	X	Х	-	-	_	+	X	X	Х	X	-	-	-	-	X	X	X	X	-	+	16	-	X	X	X)
C ₅	X	X	Х	X	X	X	X	Х	-	-	_	-	-	-	L	10	-	-	_	-	-	_	_	_	X	X	X	X	×	X	Х)
C ₆	2	+	-	_	-	H	-	_	-	-	_	+	-	H	-	-	X	Х	X	X	×	X	X	X	X	X	X	X	X	X	X)
C7	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	>

Check	1	2	10		Po	sitio	n 64	B/C -	– Da	ata le	1 64-	-75									Po	sitio	n 64	B/C -	— Da	ta Ir	76-	-87				18
Bits	64	65	66	67	-	68	69	-	-	70	71	-	72	73	74	75	76	77	78	79	-	80	81	-	-	82	83	-	84	85	86	87
C ₀	X	X	-	Х	-	X	_	Х	4	X	-	X	_	X	-	-	х	X	_	X	_	X	_	X	F	X	4	X	+	X	_	-
C ₁	X	-	X	X	x	X	-	-	X	X	_	+	-		X	-	X	_	X	X	X	X	1	-	×	X	F	-	+	-	X	E
C ₂	X	X	X	-	X	_	X	-	X	-	Х	+	X	1	-	-	х	X	X	-	X	+	X	4	X	-	X	1	X	-	_	-
C3	-	X	X	X	-	-	X	х	-	-	X	X	-	_	_	X	-	X	Х	х	-	-	X	×	-	-	X	X	-	-	-)
C ₄	X	X	X	X	X	X	Х	X	1	-	_	-	-	_	_	-	Х	X	X	X	×	X	X	×	1	-	100	_	-	-	-	-
C ₅	-	-	-	+	X	X	X	X	T	-	-	F	X	X	X	Х	_	-	_	_	X	X	X	×	-	-	18	-	X	X	X	>
C ₆	X	X	X	X	X	X	Х	X	X	X	X	X	X	X	X	X	-	_	_	_	-	_	-	-	-	-	100	1	-	-	-	-
C ₇	-	3	_	1	_		_	_	3	_	_	1	_		_		x	X	X	X	X	X	X	X	×	X	X	X	X	X	X	>

	Check					P	ositi	on 6	4D -	- Dat	a In	88-	95				
L	Bits	-	88	89	_	-	90	_		-	91	_	-	92	93	94	95
	C ₀	-	_	-	+	Х	X	X	X	_	_	_	-	X	X	X	X
	C ₁	-	-	-	+	-	-	+	-	×	X	X	X	X	X	X	X
	C ₂	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
	C3	x	X	X	X	X	X	X	X	X	X	X	X	X	X	X	×
	C4	x	+	X	X	X	X	_	-	Х	X	-	H	-	-	X	-
	C ₅	X	X	-	X	-	X	-	X	-	X	_	X	-	X	-	-
	C ₆	X	X	X	_	X	-	X	-	X	_	X		Х	-	=	-
	C7	-	X	X	X	-	_	X	X	_	_	X	X	_	_	_	X

NOTES

- The check bits are derived by performing the indicated parity operation on the data bits marked with an "X" in each row. XOR = EXCLUSIVE OR, XNOR = EXCLUSIVE NOR. The XNOR is performed internally for check bits outputs CBO₁, and CBO₂ in position and 64A/32A.
- If C5 is translated by the equation C5A = C₅ ⊕ C₆ ⊕ C₇, then the binary code of C₄, C_{5A}, C₆, and C₇ define each 4bit data group in a binary sequence, for data configurations of 64 bits or less.

Positive Versus Negative Logic

System designers use MECL 10,000 in both positive and negative logic formats. Positive logic has MECL V_{OH} (approx. -0.9 V) for Logic 1 and MECL V_{OL} (approx. -1.7 V) for Logic 0. Negative logic reverses Logic 1 and

0 voltage definitions with V_{OL} being a Logic 1. This data sheet is written around positive logic definitions. Tables and descriptions are written in terms of high (H) and low (L) logic levels to simplify translation between formats.

TABLE 9 — SYNDROME BIT DECODING FOR 96-BIT DATA

				S7	L	L	L	L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н	Н
	Sync	from	е	S6	L	L	L	L	Н	Н	Н	Н	L	L	L	L	Н	Н	Н	Н
	В	its		S5	L	L	Н	Н	L	L	Н	Н	L	L	Н	Н	L	L	Н	Н
				S4	L	Н	L	Н	L	н	L	Н	L	Н	L	Н	L	Н	L	Н
S0	S1	S2	S3						2.1										0	12
L	L	L	L			C4	C ₅	Т	C ₆	T	Т	М	C7	Т	Т	M	T	M	М	Т
L	L	L	Н		С3	T	Т	D15	Т	D31	D ₇₅	Т	Т	D47	D ₈₇	Т	М	Т	T	D63
L	L	Н	L		C ₂	T	Т	D ₁₄	Т	D30	D ₇₂	T	Т	D46	D ₈₄	Т	М	T	TS	D ₆₂
L	L	Н	Н		Т	М	М	Т	D ₇₁	T	T	D ₆₉	D ₈₃	T	Т	D ₈₁	T	D89	D ₈₈	T
L	Н	L	L		C ₁	Т	Т	D ₁₃	T	D ₂₉	D74	T	Т	D45	D ₈₆	T	М	TR	T	D ₆₁
L.	Н	L	Н		T	D ₇	D ₁₁	Т	D ₂₇	T	Т	D ₂₃	D43	Т	Т	D39	T	D ₅₅	D59	Т
L	Н.	Н	L		Т	D ₅	D ₉	Т	D ₂₅	Т	T	D ₂₁	D41	T	Т	D ₃₇	T	D ₅₃	D ₅₇	T
L	Н	Н	Н		D ₃	Т	T	D ₉₁	Т	D ₆₆	D ₁₉	T	Т	D ₇₈	D ₃₅	Т	D ₅₁	Т	T	М
Н	L	L	L		CO	Т	Т	D ₁₂	Т	D ₂₈	D ₇₃	T	T	D44	D ₈₅	Т	М	Т	T	D60
Н	L	L	Н		T	D ₆	D ₁₀	Т	D ₂₆	T	T	D ₂₂	D42	T	Т	D38	T	D ₅₄	D ₅₈	Т
Н	L	Н	L		T	D ₄	D ₈	Т	D ₂₄	T	T	D ₂₀	D40	T	Т	D36	T	D ₅₂	D ₅₆	Т
Н	L	Н	Н		D ₂	T	T	D ₉₀	T	D ₆₅	D ₁₈	T	Т	D ₇₇	D34	Т	D ₅₀	T	T	М
Н	Н	L	L		Т	М	М	Т	D ₇₀	Т	Т	D ₆₈	D ₈₂	Т	Т	D ₈₀	T	М	М	T
Н	Н	L	Н		D ₁	Т	Т	M	T	D ₆₇	D ₁₇	T	T	D ₇₉	D33	Т	D49	T	Т	М
Н	Н	Н	L	- 1	Do	Т	T	М	Т	D ₆₄	D16	Т	T	D ₇₆	D32	Т	D48	T	T	М
Н	Н	Н	Н		T	D94	D93	T	D92	T	T	M	D ₉₅	T	T	М	T	M	M	Т

= No Errors

Ci = Single Bit Error in Check Bit i
Di = Single Bit Error in Data Bit i
T = Two Errors

I = IWO Errors

M = Multiple Bit Errors (More Than Two)

Si = Syndrome Bit i Output for 16, 32, 64, and 96

Data Configurations (see Figures 3, 4, 5, and 6)

NOTE:

For data configurations of less than 96 bits, unused data bits in the above table should be replaced with an "M" (for multiple bit error).

TABLE 10 — PROPAGATION DELAY EQUATIONS FOR MULTI-CHIP DATA CONFIGURATIONS

Path	Data Bit Configuration	Propagation Delay Equation
Data In	32	(DI to CBO, pos. 32A) + (PCB to CBO, pos. 32B) = 10.7 ns + 6.3 ns = 17 ns
Check Bit Out (Use Table 14)	48, 64, 76, 88, 96	(DI to CBO, pos. 64A) + XOR = 10.7 ns + XOR
Data In	32	(DI to SYO, pos. 32A) + (SYI to Error, pos. 32B) = 10.7 ns = 10.3 ns = 21 ns
Error Detect (Use Table 15)	48, 64, 76, 88, 96	(DI to SYO, pos. $64B/C$) + XOR + (SYI to Error, pos. $64A$) = 13.2 ns + XOR + 7.9 ns = 21.1 ns + XOR
Data In to Correct	32	(DI to SYO, pos. 32A) + (SYI to SYO, pos. 32B) + (SYI to DO, pos. 32A) = 10.7 ns + 6.3 ns + 11 ns = 28 ns
Data Out (Use Table 15)	48, 64, 76, 88, 96	(DI to SYO, pos. 64B/C) + XOR + (SYI to DO, pos. 64A) = 13.2 ns + XOR + 11 ns = 24.2 ns + XOR
Data In to Single Error	32	(DI to SYO, pos. 32A) + (SYI to SYO, pos. 32B) + (SYI to SE, pos. 32A) = 10.7 ns + 6.3 ns + 11.8 ns = 28.8 ns
(SE) Out (Use Table 15)	48, 64, 76, 88, 96	(DI to SYO, pos. 64B/C) + XOR + (SYI to SE, pos. 64A) = 13.2 ns + XOR + 11.8 ns = 25 ns + XOR

Note* Calculations do not include circuit board wiring delays.

Rating	Symbol	Value	Unit
Supply Voltage (V _{CC} = 0)	VEE	-7.0 to 0	Vdc
Input Voltage ² (V _{CC} = 0)	Vin	0 to VEE	Vdc
Output Source Current — Continuous — Surge	Io	<30 <100	mAdd
Storage Temperature	T _{stg}	-55 to +150	°C
Junction Temperature	□ T _J	165	°C

NOTES:

- Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
- Input voltage limit is V_{CC} to -2.0 volts for bidirectional Pin 65 when used as an input (slice position 16 or 64A/32A).

TABLE 13 - ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board with heatsink and transverse air flow greater than 1000 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to –2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs tested in the same manner.

TABLE 12 — RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Supply Voltage (V _{CC} = 0 Volts)	VEE	-4.68 to -5.72	Vdc
Operating Temperature (Functional)	TA	0 to +70	°C
Output Drive	4 10 10	50 Ω to -2.0 Vdc	s F
Max Junction Temp	TJ	130	°C

	Test Voltage Values							
@ Test Temperature	Volts							
	VIH max	V _{IL} min	VIHA min	VILA max	VEE			
0°C	-0.840	-1.95	-1.145	-1.490	-5.2			
+25°C	-0.810	-1.95	-1.105	-1.475	-5.2			
+70°C	-0.730	-1.95	-1.050	-1.450	-5.2			

				Control of the Contro			-			and the state of the state of		The state of the s				
	5 5 5	Pin	38	¥ 1	MC	10905	Test Lim	its	12.							(Vcco)
Characteristics Symbol		Under	Inder 0°C		All all	+25°C +70°C		+70°C	°C Voltage Applied to Pins Listed Below				(VCC)			
图 第二次	1 3 3	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	VIH max	V _{IL} min	VIHA min	VILA max	VEE	Gnd
Power Supply Drain Current	IEE	9, 43	N de la	897	4 6	717	897	8	897	mAdc	70 -1 50	18	1676	13-11-	9.43	3. 15, 20 26, 60, 66
Input Current							S 1.8			4 3 3	1-18	4 -1 10		7 7 7	101	2 2
DI ₀₋₁₅	linH	27	_	200		_	200	82	200	μAdc	27				-	
SYI6, SYI7	linH	57, 58	2	400		-	400	10 E	400	μAdc	57	13 1-4	- 18-12	(E L- -	81	- 4 7
OLE, SYI5	linH	62, 56	1 H	350	- 8	- 1	350	自县 .	350	μAdc	62	+ +	-		+	
All Others	linH	47	-	300	- 8	20 1	300	ă =	300	μAdc	47	18141	18401	SLH	101	2 4
All Except Pin 65	INL	47	0.5	-	0.5	m 3	7 - 1	0.5	- I	μAdc	-	47	+ : :	10 10		
Logic "H" Output Voltage	VOH	2	-1.000	-0.840	-0.960	-	-0.810	-0.905	-0.730	Vdc	44, 45, 61	ITI				8 8
Logic "L" Output Voltage	VOL	2	-1.950	-1.665	-1.950		-1.650	-1.950	-1.625	Vdc	44, 45	344		11-12		10
Logic "H" Threshold Voltage	Vона	2_	-1.02		-0.980		- 3	-0.925	1003	Vdc	I	I I	44, 45, 61			8 H
Logic ''L'' Threshold Voltage	VOLA	2	14.7	-1.645	2 3	-	-1.630	70 ± +7	-1.605	Vdc	x - c 2	[2/2]	44, 45	11-		

NOTE: All inputs have pulldown resistors (~68 k(1)) between the input and VEE including Pin 65.

Tables 14–17 define timing characteristics of the MC10905 over operating voltage and temperature ranges. Worst-case Setup and Hold and Propagation Delays are calculated for VEE = -5.2 volts $\pm 10\%$ and a T_{Jmax} = $115^{\circ} C$. The maximum recommended operating junction temperature is $\pm 130^{\circ} C$.

Calculated limits are based on several performance factors as described in Motorola's Preliminary Design Manual for the MECL 10,000 Macrocell Array. Factors include worst case delays due to Macro selections, Fan-Out, Metal Lengths, Wire-OR, and Input Follower options. AC measurements are performed on each device to assure process integrity.

TABLE 14 — MAXIMUM PROPAGATION DELAY (IN NANOSECONDS) FOR THE WRITE MODE (GEN = H), 0 to 70°C T_A (T_J NOT TO EXCEED 115°C)

To Output			
10000000		CBO ₀₋₆	
From Input	DO ₀₋₁₅	32B	Others
DI ₀₋₁₅	7.6	13.2	10.7
ILE H	10.0	15.6	13.1
PCB ₀₋₅	><	6.3	>
NC		21.1	18.7

TABLE 15 — MAXIMUM PROPAGATION DELAY (IN NANOSECONDS) FOR THE READ MODE (GEN = L), 0 to 70° C T_A (T_J Not to Exceed 115°C)

To Output	DO ₀₋₁₅			SYO ₀₋₆			ERROR		SE	
From Input		Position or 32 B No Correction NC = H	Others	32A/64A	Position 32B	Others	Po 16 or 32B	sition Others	Po 16 or 32B	sition Others
SYI ₀₋₇	12.9		11.0	><	6.3		10.3	7.9	13.7	11.8
DI ₀₋₁₅	19.7	7.6	7.6	10.7	1	3.2	17.2	X	20.6	X
TLE	22.1	10.0	10.0	13.1	1	5.6	19.7	X	23.0	X
CBI ₀₋₆	14.8				8	3.2	12.2	X	15.6	X
NC		10.2					X		X	X

TABLE 16 — MAXIMUM PROPAGATION DELAY (IN NANOSECONDS) FOR GEN, OLE, AND THE SLICE POSITION SELECT INPUTS, 0 TO 70°C TA (TJ NOT TO EXCEED 115°C)

From Inp	o Output	DO ₀₋₁₅	SYO ₀₋₆	Error	SE
OLE	78400	6.3		4.5	4.5
GEN (L -	· H)	12.5	14.5	7.9	7.9
GEN	NC = L	18.4	11.8	15.8	19.2
(H - L)	NC = H	27.4*	19.3	23.7	26.7
MA, MB,	MC	40.2	33.6	37.5	41.0

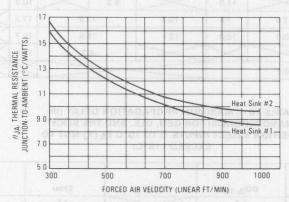
^{*} NC and GEN are both switched simultaneously H - L.

Input	Clock (Ref. Edge)	Conditions Conditions	Set Up (Min)	Hold (Min)
DI ₀₋₁₅	ĪLĒ (L → H)	A STATE TO THE PROPERTY OF THE	1.5	2.4
CBI ₀₋₆	ĪLĒ (L → H)		1.5	2.4
DI ₀₋₁₅	OLE (H → L)	GEN = L, Position - 16 or 32B	20.7	0.9
		All Others	6.3	0.9
ILE	OLE (H → L)	GEN = L, Position - 16 or 32B	23.1	0
(H → L)		All Others	8.7	0
CVI	015/11	Position - 32B	13.8	-0.5
SYI ₀₋₇	OLE (H - L)	Position - Others	11.9	0.2
CBIO:6	OLE (H → L) 9.6089	Position - 16 or 32B	15.7	-1.0
NC	OLE (H → L)	1	8.9	0.5
GEN (L → H)	OLE (H → L)	ar g002 / Juant more	11.3	0
GEN	0.5.01	NC = L	19.3	0
(H → L)	OLE (H - L)	NC = H	26.8	0
MA, MB, MC	OLE (H - L)	3,0834	41.1	0

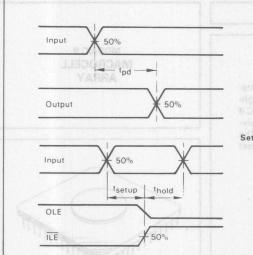
TABLE 18 — MINIMUM PULSE WIDTHS (IN NANOSECONDS)

Inputs	PW (Min)		
ILE, OLE	5		

FIGURE 7 — THERMAL CHARACTERISTICS (TYPICAL)



Heat Sink #1 is from THERMALLOY #15832-1, 3 Horizontal Fins, 0.563 inches square, Model No. 2284C. Heat Sink #2 is from WAKEFIELD #4493, Vertical Fins, 0.5 inches square. NOTE: $T_J = (\theta_J A) (P_D) + T_A$ WHERE T_J is the Junction Temperature, T_A is the Ambient Temperature, $P_D = (I_{EE}) (V_{EE}) + (15 \text{ mW})$ (number of 50 Ω outputs).

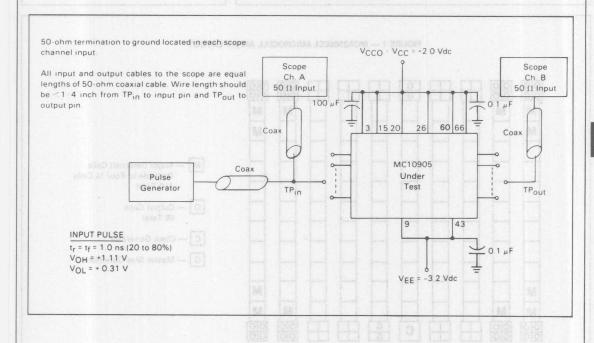


Setup and Hold Sales policy and no astee hancesonehous has

TEST PROCEDURE

- a) Establish setup time with long thold
- b) Keeping the leading edge of the input constant
 (Isetup) vary the trailing edge of the input to determine Ihold

FIGURE 9 — SWITCHING TIME TEST CIRCUIT





MCA2500ECL

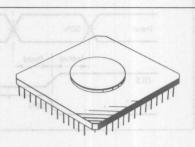
Advance Information

MCA2500ECL MACROCELL ARRAY

This specification establishes design and performance requirements for the MCA2500ECL, first in a new series of ultra high-performance bipolar arrays. Built with a high density MOSAIC II process, the circuit contains the logic power of over 2500 equivalent subnanosecond gates on one integrated circuit chip. The routing flexibility and macrocell structures are designed to meet the market needs for next generation computer systems.

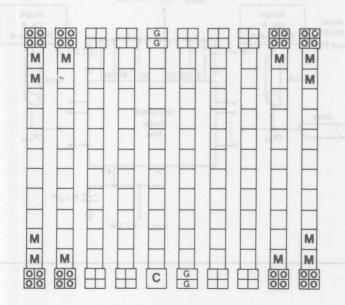
- Logic Function Specified By User
- Metal Mask Programmable (Three Unique Masks)
- Up to 2800 Equivalent Gates
- Internal Gate Delays 0.30 ns Typical
- Output Gate Delays 0.75 ns Typical
- Power Dissipation 6.5 Watts Typical
- Supported By Complete CAD Development System
- Interfaces with MECL10K/10KH or ECL 100K
- On-Chip System Design Aids

MOSAIC II
MACROCELL
ARRAY



149-Pin Pin Grid Array Package CASE 768

FIGURE 1 — MCA2500ECL MACROCELL ARRAY LAYOUT



- M Major (Internal) Cells
 Divisible to Four ¼ Cells
 110 Total
- O Output Cells 68 Total
- C Clock Generator
- G Master Bias Generator

6

PRODUCT DESCRIPTION

The MCA2500ECL Macrocell Array is a 300 picosecond, 2500 equivalent gate density LSI monolithic integrated circuit designed around the MOSAIC II oxide isolated, walled-base, walled-emitter process. The array is composed of two types of macrocells; M for major cells and O for output cells. Macrocells are similar to ECL integrated circuit packages. A macrocell library provides a selection of fully characterized logic functions, similar to an IC data book. Using the library, a designer can draw schematics for LSI macrocell array circuits similar to drawing printed circuit board schematics. The only restrictions are that designs are limited to logic functions within the library, the number of macrocell positions on the array, and the number of package I/O pins. The MCA2500ECL consists of 178 cells organized as shown in Figure 1. There are 110 major (M) cells, and 68 output (O) cells.

Most of the circuit logic is accomplished using major macrocells. Many of the M macrocell logic functions may be subdivided into half macrocells, such that different type cells can be placed into one M location for more efficient logic utilization. Simple logic functions are further divided into quarter macrocells so that it is possible to mix four different logic circuits within one M location to achieve maximum array utilization. Input signals can go directly to M or O macrocell inputs that are not marked with an asterisk (*). A signal leaving the array must go through an output (O) macrocell.

The MCA2500ECL array uses three layers of metal to accomplish the required routing and power distribution. Each cell location is comprised of uncommitted transistors and resistors, as shown in Figures 2 and 3, which are automatically interconnected with the first layer of metal forming the chosen library macro logic function. Power distribution (fixed-metal) is contained almost entirely on third layer metal and is common to all array designs. Both cell intraconnection and routing of power signals are invisible to the user. The interconnection among macrocell functions and I/O pins are accomplished with a grid of horizontal and vertical routing channels. Vertical channels are positioned between and outside the columns of cell locations, using the first layer of metal. Horizontal channels are second layer

metal and capable of routing across macrocells and vertical channels such that placement of a macro on the array never obstructs these routing channels. The three layers of metal are separated by an isolation and can be connected through "VIA's." The use of ECL seriesgated techniques yield improved circuit performance and reduces routing channel requirements, thus greatly simplifying the Computer Aided Design interconnection task

Motorola's MCA-CAD (Macrocell Array — Computer Aided Design) system is the engineering design interface between Motorola and customers developing macrocell circuits (MCA options). Customers can either use terminals at their own geographic location or access CAD software at a Motorola customer CAD design center, in both cases, over phone lines or Data Comm network. The CAD software contains programs to assist in each stage of option design with the addition of several special programs to catch syntactical errors or design violations during the design procedure rather than at test.

The CAD system is common to a variety of MCA products such that designing with one array is only "cosmetically" different than designing with another. Motorola offers a family of array products so that array size, performance, power dissipation, and package can be optimized to match system requirements. Library macrocell functions (macros) are also common to several array types.

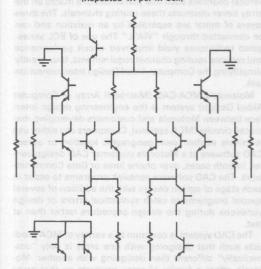
Compared with gate arrays, the use of higher component density and more efficiently designed subcircuits (macros) yield a substantial improvement in performance (circuit speed), while a greater utilization of on-chip components reduces potential system costs.

The high packing density of MCA2500ECL arrays offer up to 100-to-1 reduction in system component count when compared with equivalent systems developed using conventional logic (separately packaged SSI/MSI logic functions). System power dissipation is also reduced by as much as 12-to-1. Because a large degree of optimization is possible, the user obtains performance similar to that of a full custom design, and the accelerated turnaround time of a conventional semicustom array.

TABLE 1 — BASIC MCA2500ECL ARRAY FEATURES

- 1. 178 total cells with 120 Input/Output ports.
 - 2. Up to 2800 equivalent gates if full adders and latches are used in all cells.
 - 3. Up to 2100 equivalent gates if flip-flops and latches are used in all cells.
 - 4. Power Dissipation 6.5 watts typical.
 - 5. Major cell delays 0.30 to 0.9 ns typical.
 - 6. Output cell delays 0.60 to 1.25 ns typical.
 - 7. Up to 38 cells can drive 25 ohm loads (all outputs can drive 50 Ω loads).
 - 8. Edge speed 1.0 ns typical 20 to 80%.
 - 9. Ambient temperature range (with heat sink and 750 lfpm air) 0°C to 70°C.
 - 10. θ μ = 3.3 °C/W typical with heatsink and 750 lfpm air flow in 149 pin grid array package.
 - 11. Voltage compensated, $V_{EE} = -4.2 \text{ Vdc to } -4.8 \text{ Vdc.}$
 - 12. Interfaces with MECL 10K/10KH or ECL 100K.

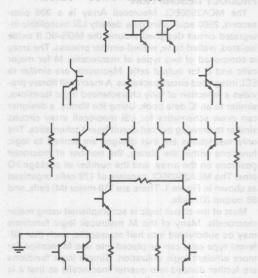
FIGURE 2 — 1/4 MAJOR CELL (M) SCHEMATIC (Repeated 4X per M Cell)



The value of series-gating can be seen by the logic equation for the 4-input exclusive OR gate shown in Figure 4. To implement this function with gates would require eight 4-input AND gates plus one 8-input OR gate. Gates also might be required to form the true and complement of each input.

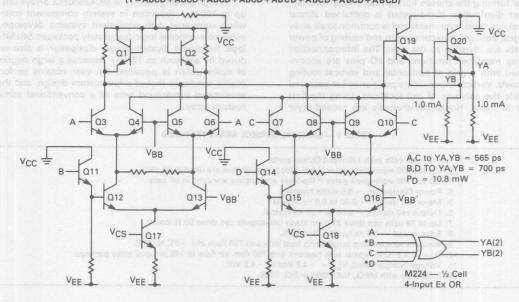
About 40 connections would be required if gates were

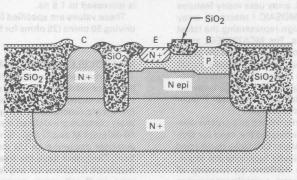
FIGURE 3 - OUTPUT CELL (O) SCHEMATIC



used, compared to five connections for the series-gated macro. Each output of the cell has a two-emitter transistor that allows a 1.0 mA or 2.0 mA emitter follower selection for power/speed optimization. This also provides the emitter-dotting capability and at the same time maintains the non-dotted output function through the second emitter.

FIGURE 4 — SCHEMATIC OF 4-INPUT EXCLUSIVE OR GATE (Y = ABCD + ABCD + ABCD + ABCD + ABCD + ABCD + ABCD)





M. G. Farrell and S. Mastroianni, U.S. Patent 4,199,380, April 22, 1980.

PROCESS DESCRIPTION

The MCA2500ECL has been fabricated by the MOSAIC II (Motorola Oxide-isolated Self-Aligned Implanted Circuits) process utilizing a walled-emitter structure and a three layer metallization system. Usage of a walled-emitter greatly reduces device area and parasitic capacitances associated with the device. A cross-section of the transistor is shown in Figure 5. Collector-to-emitter leakage current has been minimized by using a reverse master mask technique (RMMT). The reverse master mask structures in Figure 5 are the inactive base areas covered by oxide on either side of the emitter. The active base and emitter are both implanted using

this oxide for mask edge definition so that both are implanted without an intermediate masking step. Eliminating the intermediate step minimizes the collectoremitter leakage found in conventional walled-emitter structures. Separating the active and inactive base implants also reduces series base resistance without compromising the current gain of the active device. Reduced series base resistance is critical to building small transistors with high performance characteristics. Collector resistance is minimized by use of a thin epi and a deep n⁺ collector. Three levels of metallization have been used, two for interconnection wiring and the third for power buses only.

TABLE 2 — MCA1200ECL/MCA2500ECL MACROCELL ARRAY COMPARISON

FEATURE	MCA1200ECL	MCA2500ECL
Interface Levels	MECL10K	10KH/100K/10K
/O Ports	60	120
Major Cells (M)	18	110
Output Cells (O)	26	68 soltented stall aphil land
nterface Cells (I)	32	
Clock Generator	an egg No fills for sight saws	YES YES
Minimum Cell Partition	1/2 Cell 1/3	1/4 Cell
Diagnostics	is bold YES of belit and another st	Modified LSSD Macro
no.	alsored fyla sure proper operati	nal cyrrout edge rate glowdown. Once of
Basic Gate Delay (Typical)	0.65 ns	0.30 ns
4-Input OR/NOR	1.2 ns Max	0.5 ns Max
D Flip-Flop (Clock)	1.5 ns Max	0.7 ns Max
4-to-1 Multiplexer	1.4 ns Max	0.6 ns Max
Full Adder	2.8 ns Max	1.1 ns Max
Output OR Gate	3.1 ns Max	1.0 ns Max
Power (Typical)	4 Watts	6.5 Watts
Package	68 Leadless	149-Pin Grid Array
Routing Channels:		
Vertical	84	220
Horizontal	104	426
Process	MOSAIC I (2-Layer Metal)	MOSAIC II (3-Layer Metal)
Personalization Layers	3 (2 Metal and 1 VIA)	3 (2 Metal and 1 VIA)

Although the MCA2500ECL array uses many features pioneered with Motorola's MOSAIC I macrocell array family, it is a totally new design representing the latest in high-speed array concepts. The MCA2500ECL array follows Motorola's plan to continually match the latest bipolar processing technology with innovative circuit concepts. Table 2 provides a comparison between Motorola's MOSAIC I technology, MCA1200ECL array introduced in 1979, and the state-of-art MOSAIC II technology MCA2500ECL macrocell array.

In addition to improved performance and greater density, the MCA2500ECL has eliminated the need for simple I Cells by allowing each Major Cell to be partitioned into quarter cells. SSI complexity functions are implemented in quarter cells. In addition, by locating all power buses on third layer metal, a significant increase in the number of routing channels was accomplished while maintaining minimum chip dimensions.

The number of I/O ports has been increased to a full 120 channels with up to 68 outputs.

SPECIAL DESIGN FEATURES

Innovative design features have been incorporated into the MCA2500ECL array to simplify system design and enhance performance.

Clock Pulse Generator Cell (Figure 6)

The on-chip clock generator is capable of producing a narrow, edge-triggered pulse, controlled by Input A. The output signal from the generator is produced by a 10 mA emitter-follower and is capable of driving heavy loads with minimized speed degradation. Use of the generator eliminates the necessity of supplying a narrow clock pulse to the chip. Only a single clock edge needs to be supplied to the chip when the generator is used. The output of the generator can be forced high or low by using control inputs B and C.

Optional Edge Rate Selection

The typical output rise-time (20 to 80%) or fall-time (80 to 20%) is 1.0 ns. For situations where slower edge rates are desirable, such as reducing cross talk or passing signals across board connectors, Motorola offers an optional output edge rate slowdown. Once selected (via

(via CAD interface) the typical output rise- or fall-time is increased to 1.5 ns.

These values are specified for the output package pin driving 50 ohms (25 ohms for bus drivers) to -2.0 Volts.

MACROCELL LIBRARY - M CELL and O CELL

Each macrocell M and O cell location contains a number of conventional transistors and resistors that can be interconnected with CAD selected metal patterns to form logic functions. A computer-stored macrocell library contains pre-defined metal patterns for more than 60 different M and O logic functions, all available to the engineer designing an LSI circuit (macrocell array option). Designers have the freedom to select any of the macrocell functions for any M or O cell location. However, an O cell macro cannot be placed in an M cell location and visa versa. Thus, an M cell — a multiplexer, or dual flip-flop, or LSSD type diagnostic cell could be formed in any or all M locations, but not in an O location. The functions available to the designer are similar to those defined in Motorola's MOSAIC I array family, however performance is greatly improved. A list of macrocell functions currently stored in the library is shown in Table 3.

Major Cells (M)

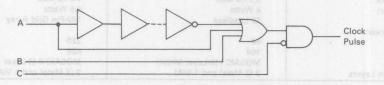
The Major Cells in the array comprise the internal area on the chip and are used for the majority of logic capability. Each Major Cell contains 56 transistors and 56 resistors as shown in Figure 2. These components are connected together on first layer metal to form logic functions with up to four series-gated structures. The macros in the Major Cell Library can use $\frac{1}{4}$, $\frac{1}{4}$, $\frac{1}{4}$ or 1 entire major cell. Each macro specifies how much of the cell is needed to implement that particular function.

Worst case propagation delay is specified for $V_{EE}=-4.2~Vdc$ to -4.8~Vdc and a maximum junction temperature of T_{J} max = 115°C. In general, a lower junction temperature can result in faster propagation delays. Macrocell power dissipation is specified at $V_{EE}=-4.5~V$.

The worst case setup and hold times are also listed for all flip-flops and latches.

The worst case minimum pulse width (tpW) is specified for the clock inputs of flip-flops and latches to insure proper operation.

FIGURE 6 — LOGIC SCHEMATIC of CLOCK PULSE GENERATOR



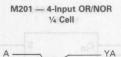
C

D

- YB

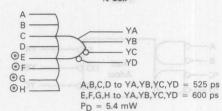
YC

YD

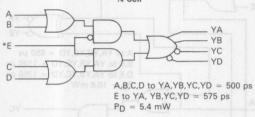


A,B,C,D to YA,YB,YC,YD = 500 ps $P_D = 3.0 \text{ mW}$

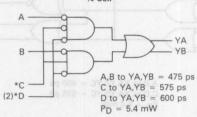
M203 - 8-Input OR/NOR 1/2 Cell



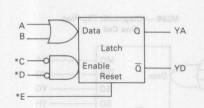
M254 — 2-to-1 Multiplexer w/Gated Inputs 1/4 Cell



M253 - 2-to-1 Multiplexer w/Enable 1/4 Cell



M293 - D Latch 1/4 Cell



YD

575

700

1000

YA

575

700

1000

M291	_	D	Flip-Flop
	1/2	C	ell

YE

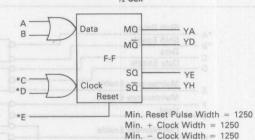
700

1750

YH

700

1750



YD

575

700

875

	-
 5475	

lold	
0	
_	
-	

C,D 1

Ho

Set

750

Reset $P_D = 26.0 \text{ mW}$

A.B

Clock \

Clock 1

Min. Clock Period = 2500 Max. Toggle Frequency ≈ 400 MHz

YA

575

700

875

(continued)

Clock 1

Set

750

Hold

0

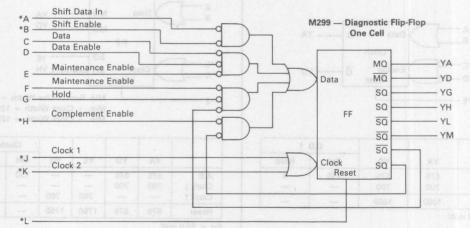
A,B

Enable

Reset

 $P_D = 14.4 \text{ mW}$

- 1. Values given for propagation delay, tpd, are max for 1.0 mA output follower current driving a fan-out of 1. Values given for power dissipation, PD, are typical with unloaded outputs. Output follower current can be selected for either 0.0 or 1.0 mA. Numbers enclosed in parenthesis at the inputs
- 2. Unmarked upper level inputs and ③ inputs can be connected to package pins.
- 3. *Inputs are connected to an input follower. Numbers enclosed in parenthesis at the output indicate the total number of internal wire OR's.



	Profit Port	nul/I		CLO	CK ↑
вациотису = 400	YA,YD	YG,YH	YL,YM	Set	Hold
A,B,H	1225	_		1400	0
C,D,E,F,G	1125	_	_	1300	0
Clock	700	ernet mwrite	d Nicoto Am	8.0 101 No.	
Clock ↑	0.1 <u>—</u> 0.0 m	700	700	OWIGHT DWG	lot mak
Reset	875	1750	1750	_	_

PD = 41.8 mW

Output Cells (O)

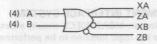
The Output Cells are located at the top and bottom of the array. These macros can use 1 or 2 output cells. The macro library specifies how many output cells are needed for each macro.

The Output Cells are primarily used to provide the interface between internal logic and logic outside the

package by supplying 50 ohm and 25 ohm drive capability. These macros also provide extra logic capability with logic functions such as OR-AND, Exclusive OR with enable, 2-to-1 multiplexer with enable, latches and flip-flops. The Output Cell Library provides macros with a similar logic capability to ½ of a Major Cell.

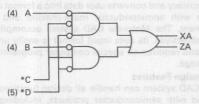
Examples of Output Cell Macros

X201 — 2-Input OR/NOR One Cell



A,B to Outputs = 875 ps PD = 16.7 mW

X253 — 2-to-1 Multiplexer w/Enable One Cell



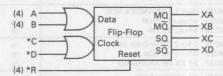
A,B to XA,ZA = 900 ps C,D to XA,ZA = 1275 ps Pp = 21.2 mW

$\rm X261 - 25~\Omega~OR/NOR~Driver$ One Cell



A,B to XA+,XB+=1900 ps A,B to XA-,XB-=1500 ps PD = 38.5 mW V_{OL} Max = -1.95 Vdc at XA=0 And XB=0 Outputs

X291 — Gated Flip-Flop Two Cells

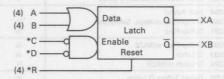


Min. + Clock Width = 2000 ps Min. - Clock Width = 2000 ps Min. Reset Pulse Width = 2000 ps

	XA,	XC,	Cloc	k↑
	ХВ	XD	Set	Hold
A,B	925 ps		1000 ps	0 ps
Clock ↑	_	1200 ps	milion ALIM 1-	14 449
Clock ↓	1150 ps	_	d Z to 1 will be	10 530
Reset	1550	3100	THE PARTY OF	SA PAR

 $P_D = 56.0 \text{ mW}$

X292 — Gated Latch One Cell



		Clock	the Tes
	XA	Set	Hold
A,B Enable	950 ps 1300 ps	1000 ps	0 ps
Reset	1800	- 85/8/	A 6 - 6 - 5 15

 $P_D = 30.2 \text{ mW}$

NOTE: All X outputs come off the collector and must be routed to the large output devices near the bonding pads. All Z outputs have a 1.0 mA emitter follower and may be used for driving internally on the chip.

Major	Cells	M-Cell
M200	5-Input OR/NOR	1/4
M201	4-Input OR/NOR 2-Input OR/NOR	1/4
M202	DATE TO MINISTER SERVICE STREET THE STREET	21 1221177
M203	8-Input OR/NOR	1/2
M204	12-Input OR/NOR	1 1/4
- 11	2-2 OTVAIND	/4
M212 M213	3-2-2-2 OR/AND 4-3-3-3 OR/AND	1/2
M214	2-2-2-1-1-1-1 OR/AND	1
M215	2-2-3-3-3 OR/AND	rapal 1
M216	4-2-3-2-3 OR/AND	1
M217	5-3-4-2 OR/AND	1
M218	5-4-3-2-1 OR/AND	1
M219	3-3 OR/AND	1/4
M221	2-2 OR/EX NOR	1/4
M222	LOTTON TO THE REAL PROPERTY OF THE PARTY OF	A 101
M223 M224	4-Input EX NOR 4-Input EX OR	1/2
100		-
M225 M226	2-1-1-2 OR/AND/EX OR 2-1-1-2 EX NOR	1/2
M227	2-1 EX OR/AND/NAND	1/2
M228	2-1 AND/EX NOR	1/4
M231	D Flip-Flop	1/2
M232	D Flip-Flop w/MUX	3/4
M241	D Latch	1/4
M242	Dual D Latch	1/2
M243	D Latch w/MUX	1/2
M244	Gated 2-Way D Latch	1/2
M245	EV NOR D Latel	3/4
M251	4-to-1 MUX w/Enable (Low)	
M252	Quad 2-to-1 MUX W/Enable (Low)	100
M253	2-to-1 MUX w/Enable (Low)	1/4
M254	2-to-1 MUX w/Gated Inputs	1/4
M255	Dual 2-to-1 MUX w/Com. SEL.	1/2
M256	2-to-1 MUX	1/2
M258	4-to-1 MUX w/Enable (High)	1
M261 M263	1-of-4 Decode (Low)	1/2
72.51	1-of-4 Decode (High)	1
M281 M282	Full Adder	1 1/2
M283	2-Bit Look-Ahead-Carry Block	1
M284	Half Adder	1/4
M290	A STATE OF THE PARTY OF THE PAR	1/2
M291	D Flip-Flop	1/2
	D Flip-Flop w/MUX	3/4
M293	D Latch	1/4
M294	D Latch w/MUX	1/2
M295 M296	Gated 2-Way D Latch EX NOR D Latch	1/2
M297	Gated 4-Way D Latch	3/4
	Dual D Latch	1/2
M299	Diagnostic D Flip-Flop	1
	4-4-4-4 AND/OR	1
M311	3-3-3-3 AND/OR	1
M312	3-3-3 AND/OR 0084	1/2
M313	2-2 OR/AND	V4
M315 M331	2-2-1-1 OR/AND	1/2
	3-2-2 AND/OR	1/2
	Gated OR	1/6
M332 M333	Gated OR Gated OR	1/2

Outpu	rt Cells	No. of O-Cells
X201 X202 X203	2-Input OR/NOR 4-Input OR/NOR 2-2 OR Gates	1
X211 X221 X231	2-2 OR/AND 2-2 OR/EX NOR D Flip-Flop	le mi bel
X232	D Latch	1
X233	Dual D Latch	2
X291	Gated Flip-Flop	2
X292	D Latch	1
X293	Dual D Latch	2
X251	2-to-1 MUX	1
X252	Dual 2-to-1 MUX	2
X253	2-to-1 MUX w/Enable	1
X261	25 Ohm OR/NOR Driver	1

DEVELOPMENT INTERFACE SYSTEM

To develop an MCA2500ECL circuit, a designer first determines the logic function to be performed by each LSI circuit. Then, using remote terminals, he defines the logic to Motorola's Western Area Computer Center in Arizona. Computer programs simplify circuit design by simulating the design logic function, placing Macrocells within the array, and automatically routing signals between the Macrocells and to the I/O package pins.

Successful implementation of a major array program such as the MCA2500ECL depends on a CAD system that accepts user design information, helps verify design accuracy and converts user data into a format compatible with semiconductor mask-making and test equipment. The Motorola CAD system accomplishes these objectives. Its data input format is easily understood and requires no special computer programming knowledge.

CAD Design Features

The CAD system can handle all design functions associated with semiconductor products, including the selection of first or second layer metal, metal widths and spacing, metal internal to Macrocells and power distribution. Macrocell Array designers use skills common to printed circuit board design, yet, with help from the CAD system, convert the equivalent of a small pc board full of SSI/MSI circuits to a high-performance custom LSI Macrocell Array device.

To help with this process, the Macrocell Array CAD system provides the following design features:

- LOGCAP functional simulation
- · Error checking of data input
- Fault grading to identify any untested nodes
- Auto place and route
- AC performance simulation to verify input to output propagation delay or performance of internal paths
- Auto definition of longest delay path between selected input and output points
- CAD data base conversion to electron beam exposure mask generation
- CAD generation of Development/Production test programs
- Customer documentation for every design

Hardware

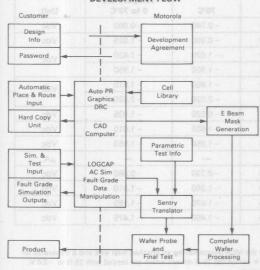
Macrocell array CAD software resides on IBM-compatible computer systems located in Scottsdale, Arizona at the Motorola Western Area Computer Center (WACC). CAD software is available to macrocell array customers on a time-share basis over normal telephone lines or datacomm network at 300 or 1200 baud data rates.

Several pieces of hardware are required at users' locations:

- Tektronix 4112, 4113 or equivalent computer display terminal
- Tektronix 4662 or 4663 interactive digital plotter (Optional)
- 300- or 1200-baud modem
- TTY-compatible keyboard/printer terminal

The appropriate CAD interface hardware is also available through Motorola Regional CAD Design Centers.

FIGURE 8 — MACROCELL ARRAY OPTION DEVELOPMENT FLOW

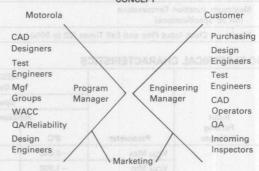


Customer	Motorola
Defines the circuit	1. Defines the
function.	Macrocell Array.
Selects the macrocells from the	Designs and controls diffusion masks.
Motorola library.	3. Develops Macrocell
3. Generates metal	Array.
interconnect pattern	4. Provides CAD
on CAD.	System to help
4. Generates the test	design options.
sequence on CAD.	5. Processes the
	C Toote the final

Program Management

Upon completion of a three-day training course, each customer is assigned a program manager to focus all technical communications during design development. The program manager serves as both engineer and administrator to assure on-time shipment of fully tested prototypes.

FIGURE 9 — MACROCELL ARRAY PROGRAM MANAGER CONCEPT



PACKAGING

The MCA2500ECL macrocell array is offered in the 149-pin grid package as shown in Figure 10.

The package has 120 I/O pins, 6 VEE pins, 6 VCC pins, 16 VCCO pins, and one orientation pin. All contacts are positioned in a uniform rectangular grid on 100 mil centers. Alumina standoffs in each corner of the package provide a 0.050 inch clearance between PC board and package surface. The macrocell array chip is dieattached to the ceramic substrate using a preform to provide excellent thermal coupling between the die and the ceramic. Thermal resistance from junction to case is less than 2°C/W.

In the schematic view of the MCA2500ECL package (Figure 12), separate power and signal metallization layers are provided to minimize lead resistance and inductance. This in turn allows up to 38 outputs to switch simultaneously into 25 ohm loads without creating excessive inductive noise. The die is mounted inverted (away from the PC board) onto a ceramic disk which is in turn brazed to an all alumina substrate. This configuration provides an elevated primary heat conducting surface which is ideally suited to conventional forced air-cooled heat sinks. The central die cavity is square to allow matched lead lengths and voltage drops. Hermiticity is provided with a solder-sealed kovar lid.

HEAT SINKS AND THERMAL CHARACTERISTICS

Worst case propagation delay in the MCA2500ECL is specified for a maximum junction temperature of 115°C. In order to meet this specification, a heat sink and air flow are required. The thermal resistance from junction-

TABLE 4 — ELECTRICAL CHARACTERISTICS

Consistent with industry LSI design requirements, the MCA2500ECL array is voltage-compensated and available in either MECL 10K/10KH temperature tracking or ECL 100K temperature compensation. The array is voltage compensated over a range of VEE values from -4.2 Vdc to -4.8 Vdc.

RECOMMENDED OPERATING CONDITIONS

Characteristic	'areau to becope	Symbol	Value	Unit
Supply Voltage (V _{CC} = 0)		VEE	-4.2 to -4.8	Vdc
Operating Temperature with Heat Sink and 750 Ifpm		TA	0 to +70	°C
Maximum Junction Temperature (for ac Specifications)	ratiolog letipida	Tj nisaanini (115 38A 10 988A	°C
Maximum Clock Input Rise and Fall Times (20 to 80%)		t _r ,t _f	10	ns

DC ELECTRICAL CHARACTERISTICS

			MECL 10K/10KH Compatible	dware is elso a O Design Cente	ECL 100K Compatible	he sppropriat i threugh Mo
	agenald 1996	Spec Limits(1)			Spec Limits(1)	
Input Forcing Voltages	Parameter	O°C An	bient Temperate	Ambient Temperature 0 to 70°C	Unit	
abotosquel /	V _{OH} Max	-0.840	-0.810	-0.740	-0.880	Vdc
	V _{OH} Min	-1.000	-0.960	-0.900	-1.025	Vdc
VIH Max	V _{OL} Max	- 1.650	- 1.650	-1.620	-1.620	Vdc
and V _{IL} Min	V _{OL} Max ²	- 1.950	- 1.950	- 1.950	- 1.950	740
	V _{OL} Min	- 1.950	- 1.950	- 1.950	-1.810	Vdc
	VOL Min ²	-2.020	-2.020	-2.020	-2.020	stook a second
VIHA Min	VOHA Min	-1.020	-0.980	-0.920	- 1.035	Vdc
and Import no b	V _{OLA} Max	- 1.630	-1.630	-1.600	-1.610	Vdc
VILA Max	VOLA Max ²	-1.950	- 1.950	- 1.950	- 1.950	Vdc
VIH Max	INH Max3	Den's a servi	THE COLUMN	1 - 45	221 - Long	μА
of molecus spec	V _{IH} Max	-0.840	-0.810	-0.730	-0.880	Vdc
Input	VIL Min	-1.950	- 1.950	- 1.950	-1.810	Vdc
Voltage Values	VIHA Min	-1.170	-1.130	-1.070	-1.165	Vdc
	VILA	-1.480	-1.480	-1.450	- 1.475	Vdc

NOTES:

- 1. DC test limits are specified after thermal equilibrium has been established with the MCA device having an attached heat sink and a transverse air flow of Ifpm. $V_{EE} = -4.5 \text{ V} \pm 0.3 \text{ V}$. All outputs are loaded with 50 Ω to -2.0 V except the 25 Ω drivers which are loaded with 25 Ω to -2.0 V.
- 2. These voltage limits are for the driver output of macros with VoL in the cutoff mode.
- 3. I_{INH} is 50 μA per input fan-in.

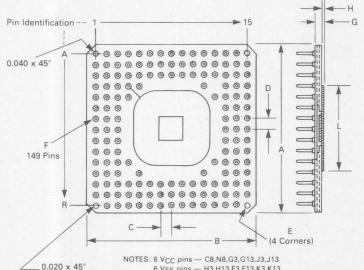
to-case is typically 1.2°C/W while the junction-to-ambient thermal is a function of heat sink configuration, mounting technique, and air flow.

Figure 11 shows typical thermal characteristics for the MCA2500ECL using a heat sink designed by Motorola. Selection of an optimum heat sink configuration takes into consideration overall height restrictions, weight, the desirability of omnidirectionality, and the need to obtain reasonably high convection coefficients. In Figure 13, a prototype heat sink was constructed from un-

coated 6061 aluminum. For attachment of heat sink to package Aremco 568 Hi-thermal conductivity adhesive was screen printed to approximately 0.0025 inch thickness on both package substrate and heat sink. Pressure was applied to remove air bubbles and ensure proper mating. The adhesive was cured at 200°F (93°C) for 30 minutes.

Care must be taken when selecting a heat sink and attachment procedures to assure mechanical integrity and reliable junction temperatures in any given system.

3 places



	Inches			
Dim	Min	Max		
Α	1.49	1.52		
В	1.49	1.52		
С	0.100	BSC		
D	0.100 BSC			
E	0.060 Ø X 0.050 Hi Alumina Standoffs — 4 Pl			
F		(0.175 Hi Pins		
G	0.054	0.066		
Н	0.045	0.050		
L	0.620 ∅	0.630 ∅		

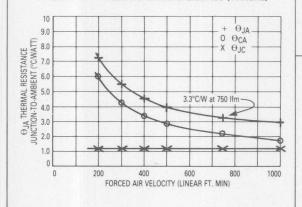
CASE 768-01

6 VEE pins - H3,H13,F3,F13,K3,K13

16 VCCO pins — C6,C7,C9,C10,D5,D11,E4,E12,L4,L12,M5,M11,N6,N7,N9,N10

Power pins are located around the die cavity on innermost leads

FIGURE 11 — THERMAL CHARACTERISTICS (TYPICAL)



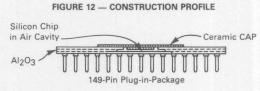
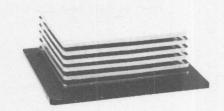
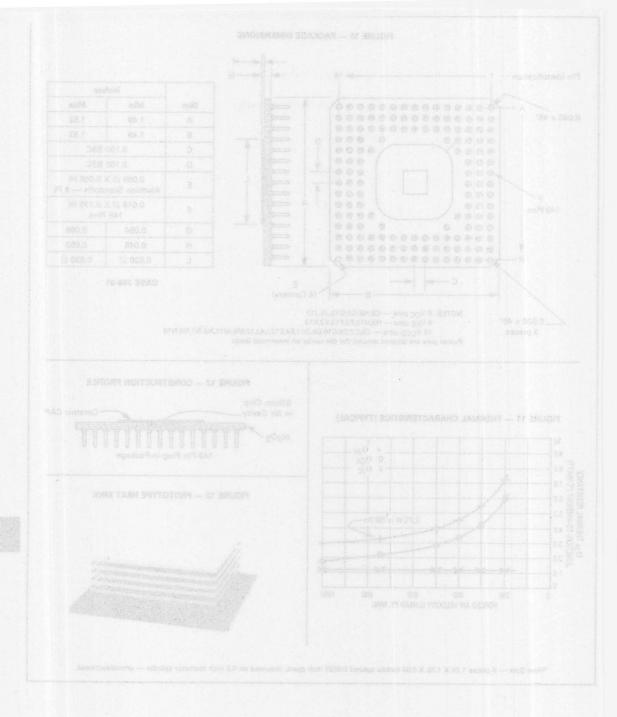


FIGURE 13 — PROTOTYPE HEAT SINK



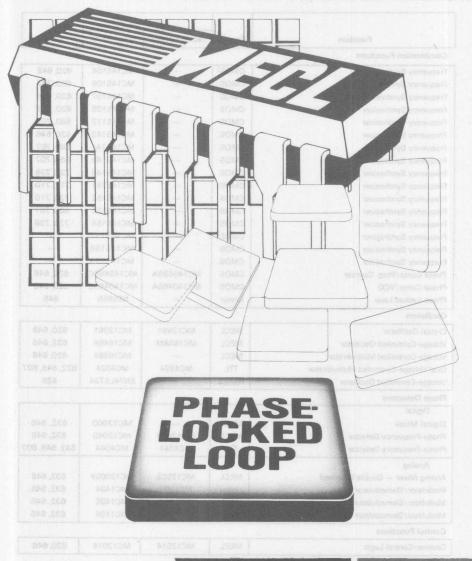
*Heat Sink — 6 plates 1.25 X 1.25 X 0.04 inches spaced 0.0625 inch apart, mounted on 0.5 inch diameter spindle — omnidirectional.



PHASE-LOCKED LOOP INTEGRATED CIRCUITS

Mocords offers the designer on erray of devices to perform phase-locked loop functions, such as phase detectors, div days, and oscillators. These devices include MECL linear, TTL and CMDS technologies covered both in this data loops and in other Motordia literature.

Datalled specification of these devices may be obtained from Mororola sales offices or authorized distributors.



Selector Guide

Data Sheets

PHASE-LOCKED LOOP INTEGRATED CIRCUITS

Motorola offers the designer an array of devices to perform phase-locked loop functions, such as phase detectors, dividers, and oscillators. These devices include MECL, linear, TTL and CMOS technologies covered both in this data book and in other Motorola literature.

Detailed specification of these devices may be obtained from Motorola sales offices or authorized distributors.

		Devi	ces		
Function	Family	-55 to +125°C 0 to +75°C		Case	
Combination Functions	The state of the s			CL SCHOOL STREET	
Frequency Synthesizer	CMOS ²	- The second	MC145104	620, 648	
Frequency Synthesizer	CMOS	Denis Denis	MC145106	680, 707	
Frequency Synthesizer	CMOS	_	MC145107	620, 648	
Frequency Synthesizer	CMOS		MC145109	620, 648	
Frequency Synthesizer	CMOS	A - 100	MC145112	680, 707	
Frequency Synthesizer	CMOS		MC145143	620, 648	
Frequency Synthesizer	CMOS		MC145144	680, 707	
Frequency Synthesizer	CMOS	73L -AT N	MC145145	680, 707	
Frequency Synthesizer	CMOS	_ h -/ ll = l	MC145146	729, 738	
Frequency Synthesizer	CMOS		MC145151	719, 710	
Frequency Synthesizer	CMOS		MC145152	733, 710	
Frequency Synthesizer	CMOS	-11	MC145155	680, 707	
Frequency Synthesizer	CMOS	11-11	MC145156	729, 738	
Frequency Synthesizer	CMOS	r Nathan	MC145157		
Frequency Synthesizer	CMOS	-1	MC145158		
Frequency Synthesizer	CMOS	-11	MC145159	seemed become	
Phase Comp/Prog. Counter	CMOS	MC14568BA	MC14568BC	620, 648	
Phase Comp/VCO	CMOS	MC14046BA	MC14046BC	620, 648	
Phase-Locked Loop	Linear		NE565N	646	
Oscillators					
Crystal Oscillator	MECL	MC12561	MC12061	620, 648	
Voltage-Controlled Oscillator	MECL	MC1648M	MC1648#	632, 646	
Voltage-Controlled Multivibrator	MECL	-	MC1658#	620, 648	
Dual Voltage-Controlled Multivibrator	TTL	MC4324	MC4024	632, 646, 60	
Voltage-Controlled Oscillator	TTL/LS		SN74LS724	626	
Phase Detectors	79a A53 SS	00-20700			
Digital					
Digital Mixer	MECL		MC12000	632, 646	
Phase-Frequency Detector	MECL	MC12540	MC12040	632, 646	
Phase-Frequency Detector	TTL	MC4344	MC4044	632, 646, 60	
Analog		90000			
Analog Mixer — Double Balanced	MECL	MC12502	MC12002#	632, 646	
Modulator/Demodulator	Linear	MC1594	MC1494	632, 646	
Modulator/Demodulator	Linear	MC1595	MC1495	632, 646	
Modulator/Demodulator	Linear	MC1596	MC1496	632, 646	
Control Functions					
Counter-Control Logic	MECL	MC12514	MC12014	620, 648	
	-				

^{*} To be introduced. #TA = -30°C to +85°C.

A = Announced.

¹ Plastic package available for commerical temperature range only.

² All CMOS devices are -40°C to +85°C.

DBS 单			Devices	
Function	Family	-55 to +125°C 0 to +75°C		Case
Prescalers/Counters				

Function	Family	-55 to +125°C	0 to +75°C	Case
Prescalers/Counters				
UHF Prescaler (÷2)	MECL		MC1690#	626, 693
÷4 Counter, 1.0 GHz	MECL		MC1697	620
÷4 Counter, 1.0 GHz	MECL	us unn Talin III	MC1699#	620, 648
Two-Modulus ÷5/÷6, 600 MHz Typ	MECL	MC12509	MC12009#	620, 648
Two-Modulus ÷8/÷9, 600 MHz Typ	MECL	MC12511	MC12011#	620, 648
Two-Modulus ÷10/÷11, 600 MHz Typ	MECL	MC12513	MC12013#	620, 648
Two-Modulus ÷32/÷33, 225 MHz	MECL	ad ast Ueo as a	MC12015##	626
Two-Modulus ÷40/÷41, 225 MHz	MECL	Coloboros esta	MC12016##	626
Two-Modulus ÷64/÷65, 225 MHz	MECL	and committee	MC12017##	626
Low-Power Two-Modulus ÷128/÷129, 520 N	MHz MECL	edonom Vi na vel s	MC12018##	626
Low-Power Two-Modulus ÷20/÷21, 225 MH	z MECL	mateuro è siul	MC12019##	626
Low-Power Two-Modulus ÷128/÷129, 1.0 G	Hz MECL	ser from 0 to 3	MC12022##	626
Low-Power ÷64 Prescaler, 225 MHz,	arugali atab is	Dates the parell	ne rugni (35	skiene lelle
3.2 to 5.5 V _{CC}	MECL	remuce edit of	MC12023	626
VHF/UHF ÷64/÷256	MECL	R) and PE input	MC12071	626
Low-Power ÷64 Prescaler, 1.1 GHz	MECL	th HA in - m	MC12073	626
Low-Power ÷256 Prescaler, 1.1 GHz	MECL	_Stock_	MC12074	626
UHF Prescaler (÷2), 750 MHz	MECL	ta sucissifiati pplications w	MC12090	626
Programmable ÷N Decade ³	TTL	MC4316	MC4016	620, 648, 650
Programmable ÷N (÷0 - 1, ÷0 - 4)	TTL	MC4317	MC4017	620, 648, 650
Programmable ÷N Hexadecimal ⁴	πTL	MC4018	MC4318	620, 648, 650
Programmable ÷N (÷0 - 3, ÷0 - 3)	TTLO	MC4319	MC4019	620, 648, 650
Programmable ÷N Decade	TTL/LS	SN54LS716	SN74LS716	620, 648
Programmable ÷N Binary	TTL/LS	SN54LS718	SN74LS718	620, 648

Notes:

#TA = -30°C to +85°C. ##T_A = -40°C to +85°C. 3 SN74LS716 is TTL/LS version of MC4016.

4 SN74LS718 is TTL/LS version of MC4018.

† PLL = Phase-Locked Loop indicates that no external synthesizer would be required to implement Electronic Tuning Systems.

** Temperature to be determined.

TBD = To be determined.

PROGRAMMABLE MODULO-N COUNTERS

The monolithic devices are programmable, cascadable, modulo-N-counters. The MC4316/4016 can be programmed to divide by any number (N) from 0 thru 9, the MC4318/4018 from 0 thru 15. The MC4317/4017 consists of a modulo 2 counter which can be programmed to divide by 0 or 1 and a modulo 5 counter which can be programmed to divide by any number from 0 to 4. The MC4319/4019 contains two modulo 4 counters which can be programmed to divide by any number from 0 to 3.

The parallel enable (PE) input enables the parallel data inputs D0 thru D3. All zeros are entered into the counter by applying a logic "0" level to the master reset (MR) and PE inputs. This causes the counter to stop counting (count = 0). All data inputs are independent of the logic level of the Clock.

Modulo-N counters are useful in frequency synthesizers, in phase-locked loops, and in other applications where a simple method for frequency division is needed.

All Types:

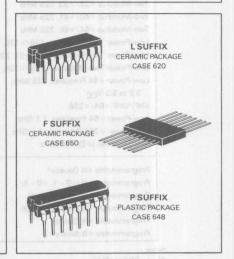
Clock, PE = 2

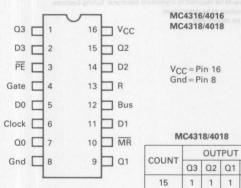
Output Loading Factor = 8

Input Loading Factor: Total Power Dissipation = 250 mW typ/pkg D0, D1, D2, D3, Gate = 1 Propagation Delay Time:

 $\overline{MR} = 4$ Clock to Q3 = 50 ns typ Clock to Bus = 35 ns typ

PROGRAMMABLE MODULO-N COUNTERS

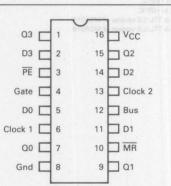




MC4316/4016

0011117		OUT	PUT	
COUNT	Q3	Q2	Q1	QO
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

COLUNIT	T											
COUNT	Q3	Q2	Q1	QO								
15	1	1	1	1								
14	1	1	1	0								
13	1	1	0	1								
12	1	1	0	0								
11	1	0	1	1								
10	1	0	1	0								
9	1	0	0	1								
8	1	0	0	0								
7	0	1	1	1								
6	0	1	1	0								
5	0	1	0	1								
4	0	1	0	0								
3	0	0	1	1								
2	0	0	1	0								
1	0	0	0	1								
0	0	0	0	0								



MC4317/4017

1410-43	17/4017
COLUNIT	OUTPUT
COUNT	Q0
1	1
0	0

COUNT	C	OUTPUT							
COUNT	Q3	Q2	Q1						
4	1	0	0						
3	0	1	1						
2	0	1	0						
1	0	0	1						
0	0	0	0						

	MC4317/4017 MC4319/4019							
2	V _{CC} = Pin 16 Gnd = Pin 8							

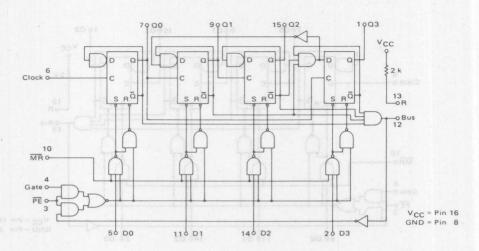
MC4319/4019

COUNT	OUT	PUT
COUNT	Q1	QO
3	1	1
2	1	0
. 1	0	1
0	0	0

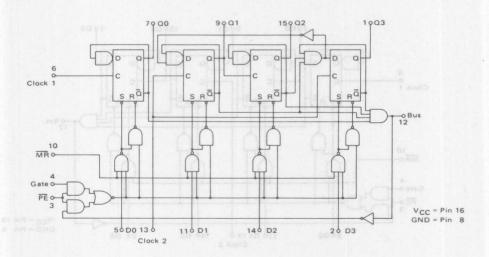
COUNT	OUT	PUT
COUNT	Q3	Q2
3	1	1
2	1	0
1	0	1
0	0	0

LOGIC DIAGRAMS

MC4316/4016

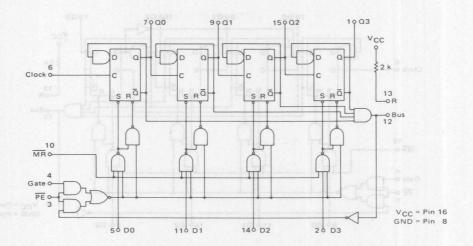


MC4317/4017

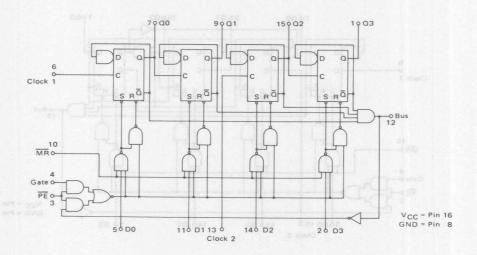


LOGIC DIAGRAMS (continued)

MC4318/4018



MC4319/4019



MC4317/4017 MC4319/4019

MC4316/4016 MC4318/4018 02 15 B 13

6 Clock 1 QO 0 5 D0 D1 02 15 0 14 D2 D3 D3 O 3 PE 10 MR Bus 12

TEST CURRENT/VOLTAGE VALUES VIH VIHH VILT VIHT VCC VCCL VCCH OL1 OL2 OL3 OH IC Temperature 50 45 55 50 45 55 -55°C 12.8 13.8 9.6 -1.6 -+25°C 12.8 13.8 9.6 -1.6 -10 0.8 MC4316-4019 2.4 2.0 0.4 0.8 5.5 2.0 5.0 4.5 5.5 2.0 5.0 4.75 5.25 2.0 5.0 4.75 5.25 +125°C 12.8 13.8 9.6 -1.6 0.4 2.4 0.8 5.5 0°C 12.8 13.8 9.6 -1.6 -+25°C 12.8 13.8 9.6 -1.6 -10 0.8 MC4016-4019 2.5 0.4 5.5 0.8 +75°C 12.8 13.8 9.6 -1.6 -0.4 2.5 0.8 2.0 5.0 4.75 5.25 5.5

			MC4316 -4319 Test Limits					ts	MC4016-4019 Test Limits					1	12.8	13.8	9.6	-1.6	-	TEST SUPPLEMENTAGE TAGE			AGE APPLIED TO PINS LIST		TED BELOW			-					
Characteristic						Pin	-5	-55°C		5°C	+12	+125°C	0	°C +2		5°C	+7	5°C			3 1 1		1	TE	STCORRE	NITVOLTAG	E APPLIE	U TO PINS LI	STED BELL	Ovv.	-	T	
	Symbol	Test	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	IOL1	IOL2	IOL3	ІОН	lic	VIL	VIH	VIHH	VILT	VIHT	VCC	VCCL	VCCH	Gnd				
nput	8 1 3	W MIR	2 9		9	5			A.					100			3	1500						10			8	1					
Forward Current	IIL1	2	1 70	-1.6	1	-1.6	-	-1.6	1	-1.6		-1.6			mAdc	-		-			2	10	-	13.2				16	3,8				
		3	100	-3.2	1	-3.2	- 1	-3.2		-3.2	-	-3.2		-3.2	1	1 = (3)	-	-			3	4	-						8,12				
		4	1	-1.6	30	-1.6	-	-1.6	-	-1.6		-1.6		-1.6		T					4	3	101-0						8				
		5	-	-1.6	-	-1.6	-	-1.6	1	-1.6		-1.6		-1.6		-	1				5	. 10	-	n n		100			3.8				
		10	NI:	-3.2	75	-3.2	10	-3.2	1	-3.2		-3.2		-3.2		-	774				10	2,5,11,14	-	130					3.8				
	1	11		-1.6	13	-6.4		-6.4	MT.	-6.4	. 3	-6.4		-6.4				1			11	10	91.						3.0				
	1 8 9	14	13	-1.6		-1.6		-1.6	1	-1.6		-1.6		-1.6			1				14	10											
		6.07	-	-	-	-		10000	-				-	1000	,	-	-		-	-			6.1	100	1		10	-	3.8				
	11L2	2	13	-1.4	17	-1.4	-	-1.4	1	-1.4	. 7	-1.4	-	-1.4	mAdc	10	100				2	10	-0				16		8.12				
		3	8.7	-2.8	1	-2.8	50	-2.8	177	-2.8	100	-2.8		-2.8			1	-			4	3	-						8				
		-	100	-1.4	1	-1.4	2	-1.4	1 2	-1.4	1	-1.4		-1.4	19 1 9						5	10	E				1 N		3.8				
		6*		-2.8	100	-2.8		-2.8		-2.8	13	-2.8		-2.8	8	1					6	10	7.5	- 6			17 H 18	R. I.	8				
		10		-5.6	100	-5.6		-5.6		-5.6		-5.6		-5.6	100						10	2,5,11,14	製工機	- 0 1				1 100	3.8				
		11	1000	-1.4	3	-1.4	1.5	-1.4	15.5	-1.4		-1.4		-1.4	8	100					11	10	6.14	19 C 21					1				
	1	14	1 3	-14		-1.4	- 1	-1.4	LU	-1.4		-1.4		-1.4		1	1.3				14	10											
Leakage Current	1.	2	- 6	40	-	40		40	1	40		40	100	40	uAdc.	-6		-			-	2	-		10112	1	100	16	8.10				
Leakage Current	TH	2		80	13	80	-	80		80		80		80	имас	-					1 3	3	AZA	A DOL				10	4.8				
		4	-	40	1	40	-	40	M. T.	40		40		40	1		1				1380	4	Y TY	The Real Property of					3.8				
	5	-	40	39	40	10	40		40		40	1	40	6						1 37	5							8.10					
	-	6	3 3	80	- 6	80		80	- 37	80	7	80		80		-					1 22	6		1					8				
		10	1	160	47	160		160		160	20	160		160							1	10	_	1 - 2		F- 12			2.5.8.11				
		11	100	40	25	40	1-1	40	-	40	1 3	40		40	100				100		1.5	11	-11-						8.10				
	1	14	-	40	-20	40	-0	40	-	40		40		40		12 0						14	-						8.10				
	Чнн	2	1.0	1	1.0	500	1.0		1.0	12	1.0		1.0		mAdc					-	100	3 0	2		IN LUMBER OF			16	8,10				
	I HHI	3	1		1.0		1		1	NE SH	1		1		I						100	19 99	3			1 8-8		1	4,8				
	1 0	4	18							0.3					Berlin 1				1045		0.5		4						3,8				
	1 2	5	2	-		-		- 1								-					00.47		5	The Walter		-		+6	8.10				
	1	6	2	-		-				200		1 4				-	TE.				走名		6						-8				
		10	50	-		-		-										1_	-		16.00		10	4.4		100			2,5,8,11				
	-	11		-		-		-	1			-		1 -2 1		-	-		-		24	-9 00	11		150			1 1	8,10				
	1	14	1	-	Y	-		. =		-		100	1	-0	V	-	-		1	0.0	2.3		14			1			8,10				
Clamp Voltage	Vic	2**	-	-	-	-1.5	-	-	-	-	-	-1.5	-	-	Vdc	-	-	-	-	2	9-5	14 -			1140	-	16	-	8				
Output		8 6					1										7		1	17.50	En 20	4 2			1				1				
Output Voltage	VOL	1	-	0.4	-	0.4	-	0.4	-	0.4	- 1	0.4		0.4	Vdc	1	-		-		2 6	13 - 0	- 1	2,3,5,11,14			16		8				
		1	-	0.4	-	0.4	-	0.4	-	0.4	104	0.4		0.4	1	-	1		3 -	1	100	0 3	-0	2,3,5,11,14		1		16	1				
		12	-	0.5	-	0.5	-	0.5	-	0.5	-	0.5	-	0.5		-	-	12	-	-	12.0		-0	3	2,5,11,14		16						
	VOH	1	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	Vdc	-	1 -1	-	1	100	14.19	18/1	-	3	2,5,11,14		16	FA) - XX	8				
Short-Circuit Current	los	1	-20	-65 -3.8	-20 -1.8	-65 -3.8	-20 -1.8	-65 -3.8	-20 -1.8	-65 -3.8	-20	-65 -3.8	-20	-65 -3.8	mAdc mAdc	-	-	7.	-	1	3	2,5,11,14	-8	1 1 2 4	Flogs	16 16		1	1,8				
D	0	13#	-1.8	-3.6	-1.8	-3.0	-1.0	-3.0	-1.0	-3.0	-1.0	-3.0	-1.0	-3.0	mAdc		-	-		-	75.67		-			10	-	-	0,13				
ower Requirements (Total Device)	13 13	i ii i																			7.5	9 9		9 5 4 6	D.C.								
Power Supply Drain	13.15	10				cc		-				65		-	mAdc				1200		0.5	8 8 7	1.3	w 63 4 4	25.4	16		1000	8				
rower Supply Drain	1cc	16	-			65						00			HMUC			Charles .			1	1 61.6				10		1	0				

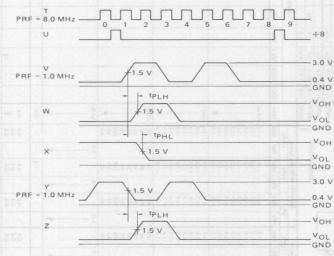
^{*}For MC4317/4017 and MC4319/4019 also test pin 13 using the same procedure except V_{II} applied to pin 13.

^{* *} Test all inputs in the same manner.

[#]Test applies only to MC4316/4016 and MC4318/4018.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 9950-ohm resistor and the scope termination impedance constitute a 200:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

 C_{T} = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitance.



SWITCHING TIME TEST PROCEDURES ($T_A = 25^{\circ}C$) (Letters shown in test columns refer to waveforms.)

				INPUT	OUTP	UT					
		Clock	Gate	D0, D1, D2	D3,PE, MR	Bus	Q3	LIMITS			
TEST	SYMBOL	Pin 6	Pin 4	Pins 5,11,14	Pins 2,3,10	Pin 12	Pin 1	Min	Max	Unit	
Toggle Frequency (Check before measuring propagation delay.)	f _{tog}	T	T 3	Gnd	2.5 V		U a	8.0		MHz	
Propagation Delay Clock to Bus	tPLH	V	V	Gnd	2.5 V	w	2 2	-	65	ns	
Propagation Delay Gate to Q3	^t PLH	Y	Y	Gnd	2.5 V		z	-	35	ns	
Propagation Delay Clock 1 to Q3 MC4316, 17/4016, 17 MC4318, 19/4018, 19	t _{PHL}	V	V	Gnd	2.5 V		×	-	45 78	ns ns	

OPERATING CHARACTERISTICS

MC4316/4016, MC4318/4018

Operation of both counters is essentially the same. The MC4316/4016 has a maximum modulus of ten while the MC4318/4018 is capable of dividing by up to sixteen. Minor differences in the programming procedure will be covered in the discussion of cascaded stages.

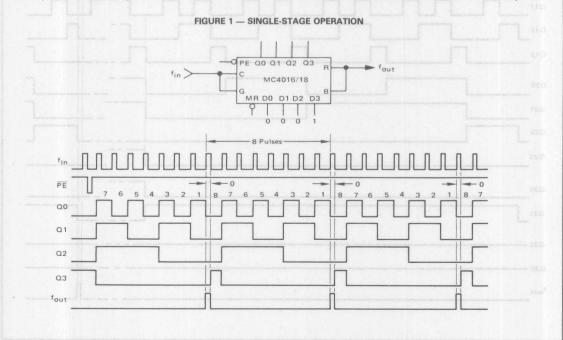
Suitable connections for operating a single stage are shown in Figure 1, as well as appropriate waveforms. The desired modulus is applied to the data inputs D0, D1, D2, and D3 in binary (MC4018) or binary coded decimal (MC4016) positive logic format. If a number greater than nine (BCD 1001) is applied to the MC4016, it treats the most significant bit position as a zero; if for example, binary fourteen (1110) were applied to an MC4016, the counter would divide by six. BCD eight is programmed in Figure 1. As PE is taken low the states on the parallel inputs are transferred to their respective outputs. Subsequent positive transitions of the input clock will decrement the counter until the all zero state is detected by the bus gate. The resulting positive transition of the bus line is internally inverted and fed back to the preset gating circuitry but does not yet preset the counter since the gateclock input is still high. As the clock returns to the low state the counter is set to the programmed state, taking the bus line low. The net result is one positive pulse on the bus line for every N clock pulses. The output pulse width is approximately equal to one clock pulse high time.

Operation will continue in this fashion until the data on the programmable inputs is changed. Since the preset circuitry is inhibited except when the counter is in the zero state, preset data may be changed while clocking is occurring. If it is necessary to enter a new number before the counter has reached zero this can be done by momentarily taking $\overline{\text{PE}}$ low. Countdown will continue from the new number on the next positive clock transition.

The counters can be made to divide by 10 (MC4016) or 16 (MC4018) by inhibiting the preset logic. This may be done by either holding the gate input high or by holding the bus line low.

The normal connections for cascading stages are indicated in Figure 2, with the appropriate waveforms. Note that the gate input of each stage is connected to the clock; all bus outputs are tied to one of the internal pullup resistors, R. The total modulus for cascaded MC4016s is determined from $N_T=N_0+10N_1+100N_2+\ldots$; N_T for MC4018s is given by $N_T=N_0+16N_1+256N_2+\ldots$ Stated another way, the BCD equivalent of each decimal digit is applied to respective MC4016 stages while the data inputs of the MC4018 stages are treated as part of one long binary number. The difference in programming is illustrated in Figure 2 where $N_T=245$ is coded for both counter types.

Cascaded operation can be further clarified by referring to the timing diagram of Figure 2. For the MC4016, counting begins with the first positive clock transition after the data has been set in. After the five clock pulses, the least-significant stage has been counted down to zero. The bus line does not go high at this time since the three bus terminals are wire-ORed and the other two stages are not in the zero state. Since no reset occurs, the next positive

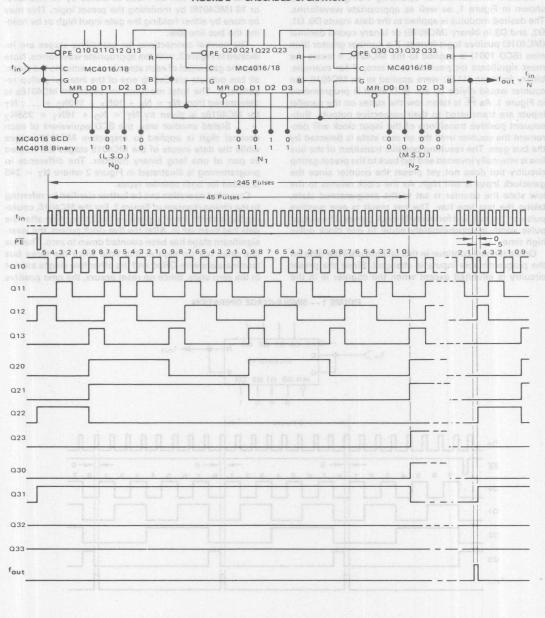


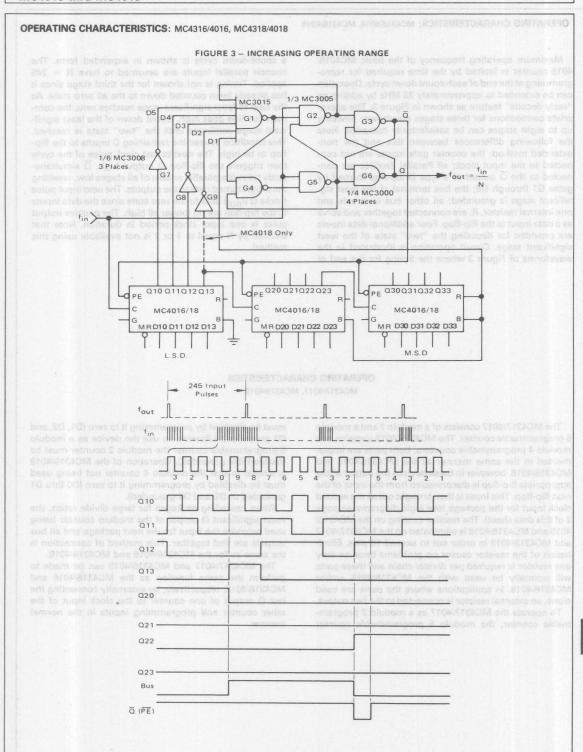
OPERATING CHARACTERISTICS: MC4316/4016, MC4318/4018

clock edge advances the least significant stage to the nine (1001) state, causing the second stage to be decremented. The process continues in this manner with the least significant stage now dividing by ten. The second stage eventually counts down to zero and also reverts to di-

viding by ten. Each pulse out of the second stage decrements the third until it reaches zero. At this time the bus line goes high; it remains high until the clock goes low, causing all three stages to be reset to the programmed count again.

FIGURE 2 — CASCADED OPERATION





Maximum operating frequency of the basic MC4016/ 4018 counter is limited by the time required for reprogramming at the end of each count down cycle. Operation can be extended to approximately 25 MHz by adding an "early decode" feature as shown in Figure 3. The appropriate connections for three stages are shown; however up to eight stages can be satisfactorily cascaded. Note the following differences between this and the nonextended method: the counter gate inputs are not connected to the input clock; all Parallel Enables are connected to the Q output of a type D flip-flop formed by gates G1 through G6; the bus terminal of the least significant stage is grounded; all other bus terminals and one internal resistor, R, are connected together and serve as a data input to the flip-flop. Four additional data inputs are provided for decoding the "two" state of the least significant stage. Circuit operation is illustrated in the waveforms of Figure 3 where the timing for the end of a count-down cycle is shown in expanded form. The counter parallel inputs are assumed to have N = 245 applied. Timing is not shown for the third stage since it has already been counted down to the all zero state. As the next-to-least significant stage reaches zero, the common bus line goes high. Count down of the least significant stage continues until the "two" state is reached. This condition causes the remaining D inputs to the flipflop to be high. The next-to-last clock pulse of the cycle then triggers the flip-flop Q output high. Q simultaneously takes the parallel enable of all stages low, resetting the programmed data to the outputs. The next input pulse clocks Q (fout) back to the zero state since the data inputs to the flip-flop are no longer all high. The positive output pulse is one input clock period in duration. Note that division by N equal to 1 or 2 is not available using this method.

OPERATING CHARACTERISTICS

MC4317/4017, MC4319/4019

The MC4317/4017 consists of a modulo 2 and a modulo 5 programmable counter. The MC4319/4019 contains two modulo 4 programmable counters. Both parts are implemented in the same manner as the MC4316/4016 and MC4318/4018, however in these devices the output of the appropriate flip-flop is disconnected from the input of the next flip-flop. This input is then brought out as the second clock input for the package (see logic diagrams on page 2 of this data sheet). The resistor existing on the MC4316/ 4016 and MC4318/4018 is eliminated on the MC4317/4017 and MC4319/4019 in order not to exceed 16 pins. Elimination of the resistor causes no problems because only one resistor is required per divider chain and these parts will normally be used with the MC4316/4016 and/or MC4318/4018. In applications where the parts are used alone, an external resistor is connected to the bus output.

To operate the MC4317/4017 as a modulo 2 programmable counter, the modulo 5 programmable counter must be disabled by programming it to zero (D1, D2, and D3 grounded). Likewise, to use the device as a modulo 5 programmable counter the modulo 2 counter must be disabled (D0 grounded). Operation of the MC4319/4019 is similar in that the modulo 4 counter not being used must be disabled by programming it to zero (D0 thru D1 grounded or D2 and D3 grounded).

When cascading packages for large divide ratios, the most significant Ω output of the modulo counter being used provides the input for the next package and all bus outputs are tied together. This method of connection is the same as for the MC4316/4016 and MC4318/4018.

The MC4317/4017 and MC4319/4019 can be made to perform the same function as the MC4316/4016 and MC4318/4018, respectively, by externally connecting the last Q output of one counter to the clock input of the other counter and programming inputs in the normal manner.

APPLICATIONS INFORMATION

A typical system application for programmable counters is illustrated in the frequency synthesizer shown in Figure 4. There the counter provides a means of digitally selecting some integral multiple of a stable reference frequency. The circuit phase locks the output, f_{VCO} , of a voltage controlled oscillator to a reference frequency, f_{ref} . Circuit operation is such that $f_{VCO} = Nf_{ref}$, where N is the divider ratio of the feedback counter.

In many synthesizer applications the VCO is operated at VHF frequencies too high for direct division by TTL counters. In these cases the VCO output is usually prescaled by using a suitable fixed divide-by-M ECL circuit as shown in Figure 5. For this configuration, fyCO = NMf_{ref}, where N is variable (programmable) and M is fixed. Design of the optimum loop filter requires that the input reference frequency be as high as possible where

FIGURE 4 — MTTL PHASE-LOCKED LOOP

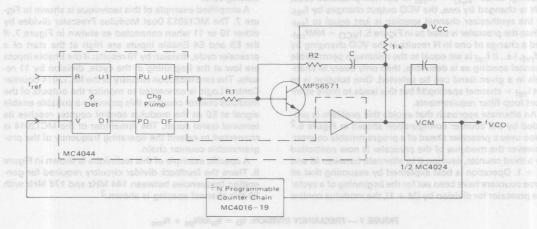
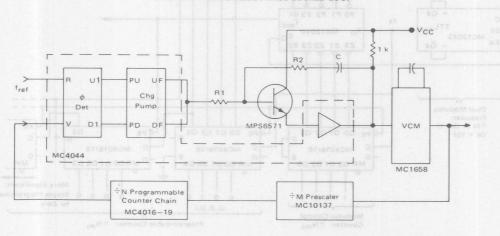
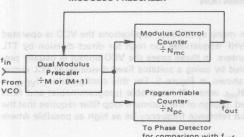


FIGURE 5 - MTTL-MECL PHASE-LOCKED LOOP



1 See Motorola Application Note AN-535 and the MC4344/4044 Data Sheet for detailed explanation of overall circuit operation

FIGURE 6 — FEEDBACK COUNTERS WITH DUAL MODULUS PRESCALER



the upper limit is established by the required channel spacing. Since $f_{VCO}=Nf_{ref}$ in the non-prescaled case, if N is changed by one, the VCO output changes by f_{ref} , or the synthesizer channel spacing is just equal to f_{ref} . When the prescaler is used as in Figure 5, $f_{VCO}=NMf_{ref}$, and a change of one in N results in the VCO changing by Mf_{ref} , i.e., if f_{ref} is set equal to the minimum permissible channel spacing as is desirable, then only every M channels in a given band can be selected. One solution is to set $f_{ref}=$ channel spacing/M but this leads to more stringent loop filter requirements.

An alternate approach that avoids this problem is provided by the counter configuration shown in Figure 6.2 It too uses a prescaler ahead of a programmable counter, however the modulus of the prescaler is now controlled by a third counter, causing it to alternate between M and M + 1. Operation is best explained by assuming that all three counters have been set for the beginning of a cycle: the prescaler for division by (M + 1), the modulus control

counter for division by N_{mc} , and the programmable counter for division by N_{pc} . The prescaler will divide by (M+1) until the modulus control counter has counted down to zero; at this time, the all zero state is detected and causes the prescaler to divide by M until the programmable counter has also counted down to zero. When this occurs, a cycle is complete and each counter is reset to its original modulus in readiness for the next cycle. For this configuration,

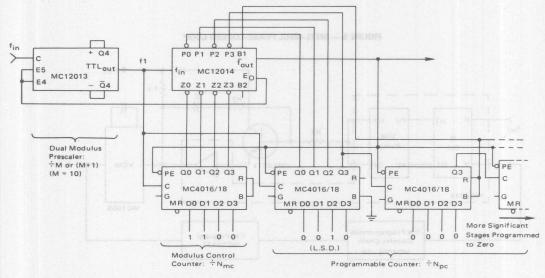
$$f_{out} = \frac{f_{in}}{MN_{pc} + N_{mc}}$$

In terms of the synthesizer application, $f_{VCO} = (MN_{pc} + N_{mc})$ fref and channels can be selected every fref by letting N_{pc} and N_{mc} take on suitable integer values, including zero.

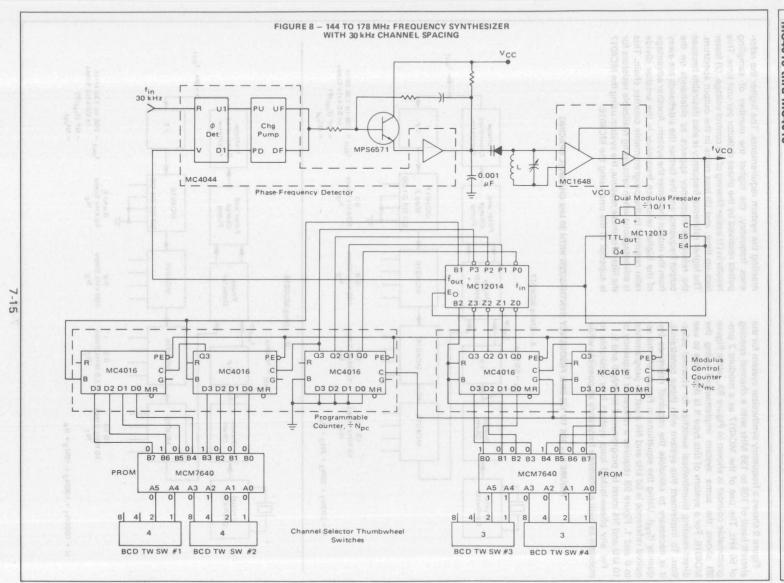
A simplified example of this technique is shown in Figure 7. The MC12013 Dual Modulus Prescaler divides by either 10 or 11 when connected as shown in Figure 7. If the E3 and E4 Enable inputs are high at the start of a prescaler cycle, division by 10 results; if the Enable inputs are low at the beginning of the cycle, division by 11 results. The zero detection circuitry of the MC12014 Counter Control Logic is connected to monitor the outputs of the modulus control counter; this provides a suitable enable signal at E0 as the modulus control counter reaches its terminal (zero) count. The remainder of the MC12014 is connected to extend the operating frequency of the programmable counter chain.

A specific example of this technique is shown in Figure 8. There the feedback divider circuitry required for generating frequencies between 144 MHz and 178 MHz with 30 kHz channel spacing is shown.²

FIGURE 7 - FREQUENCY DIVISION: fo = fin/MNpc + Nmc



2. This application is discussed in greater detail in the MC12014 Counter Control Logic data sheet.



MC4316. thru MC4319 mC4017 as a modulo 2 programmable counter is shown in Figure 9A, while Figure 9B shows the same system implemented using the MC4016. For a system of this type it is desirable to use direct-reading thumbwheel switches for channel selection. To implement this system with these constraints, it is necessary to calculate the required reference frequency (fref). Using the equations in Figure 9A, the required reference is 50 kHz and N4 must be programmed to 0 and 1. Figure 9B requires a reference frequency of 10 kHz and N4 must be programmed to only 0 and 5.

For any phase-locked loop system it is desirable to maintain as high a reference frequency as possible while

pulses received by the phase detector per unit time. This results in (1) easier filtering of the control voltage, (2) faster lock-up time, and (3) less noise in the output spectrum. The higher reference frequency is also desirable because the reference frequency appears as sidebands on the output frequency and the farther the sidebands are away from the output the better the system. Another advantage of the higher reference frequency is the smaller divide ratio required in the programmable counter chain. This is advantageous when calculating realizable resistors for the filter. For these reasons, the system using the MC4017 is superior to the one using the MC4016.

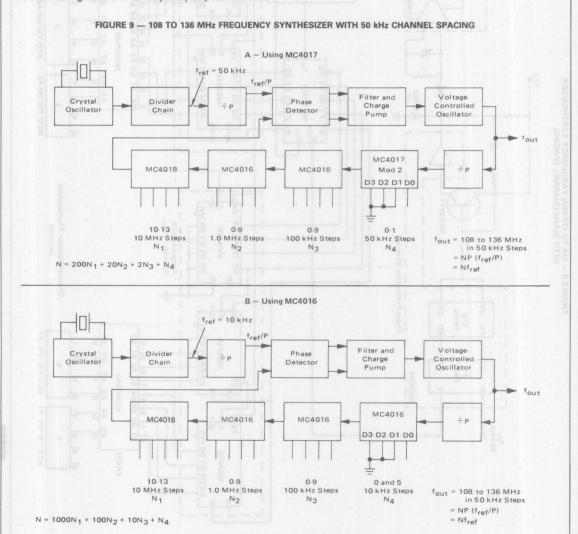
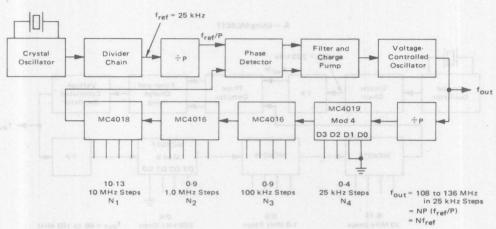


Figure 10 shows the implementation of the aircraft band synthesizer with 25 kHz channel spacing (the 25 kHz spacing has been proposed to the FCC). The system is implemented in Figure 10A using the MC4019, and has

a reference frequency of 25 kHz. Figure 10B shows the system using an MC4018 as the first counter, and has a reference frequency of 6.25 kHz to obtain the direct programming.

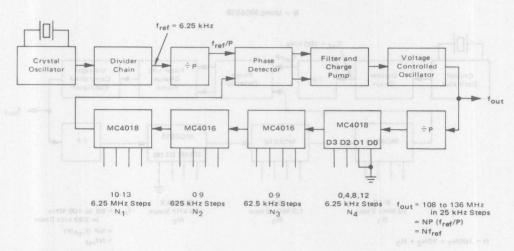
FIGURE 10 — 108 TO 136 MHz FREQUENCY SYNTHESIZER WITH 25 kHz CHANNEL SPACING

A - Using MC4019



 $N = 400N_1 + 40N_2 + 4N_3 + N_4$

B - Using MC4018



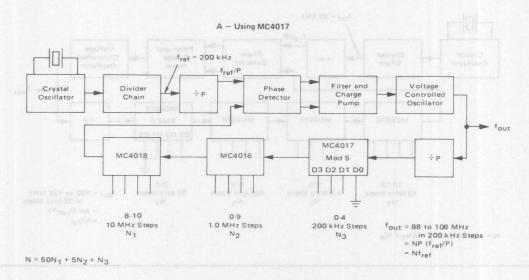
 $N = 1600N_1 + 160N_2 + 16N_3 + N_4$

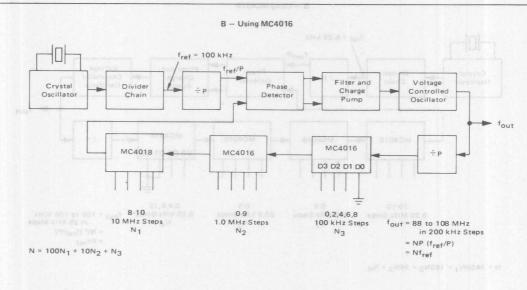
Figures 11A and 11B show the FM band implemented with MC4017 (used as a modulo 5 counter) and MC4016, respectively. The first system has a 200 kHz reference frequency, and the second system has a 100 kHz reference frequency. These systems using the MC4017/19 offer the same advantages over the MC4016/18 as with the aircraft band systems.

These examples illustrate the desirability of the MC4317/4017 for phase-locked loop applications where the chan-

nel spacing is 2 \times 10ⁿ Hz when used as a modulo 5 programmable counter, and 5 \times 10ⁿ Hz when used as a modulo 2 programmable counter. The MC4319/4019 is for applications with a channel spacing of 2.5 \times 10ⁿ Hz. The MC4316/4016 covers phase-locked loop applications where the channel spacing is 1 \times 10ⁿ Hz. The MC4318/4018 is used when the most significant digit is between 9 and 15.

FIGURE 11 — 88 TO 108 MHz FREQUENCY SYNTHESIZER WITH 200 kHz CHANNEL SPACING







MC4324/ MC4024

DUAL VOLTAGE-CONTROLLED MULTIVIBRATOR

The MC4324/4024 consists of two independent voltagecontrolled miltivibrators with output buffers. Variation of the output frequency over a 3.5-to-1 range is guaranteed with an input dc control voltage of 1.0 to 5.0 voltage.

Operating frequency is specified at 25 MHz at 25°C. Operation to 15 MHz is possible over the specified temperature range. For higher frequency requirements, see the MC1648 (200 MHz) or the MC1658 (125 MHz) data sheet.

This device was designed specifically for use in phase-locked loops for digital frequency control. It can also be used in other applications requiring a voltage-controlled frequency, or as a stable fixed frequency oscillator (3.0 MHz to 15 MHz) by replacing the external control capacitor with a series mode crystal.

Maximum Operating Frequency = 25 MHz Guaranteed @ 25°C

Power Dissipation = 150 mW typ/pkg

TYPICAL APPLICATIONS

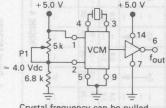
FIGURE 1 — ASTABLE MULTIVIBRATOR

+5.0 V 25 pF +5.0 V 4 0 3 14 6 VCM 7 fout

f_{out} = 10 MHz

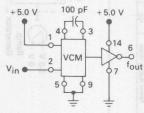
Output Loading Factor = 7

FIGURE 2 — CRYSTAL CONTROLLED MULTIVIBRATOR



Crystal frequency can be pulled slightly by adjusting P1.

FIGURE 3 — VOLTAGE-CONTROLLED MULTIVIBRATOR



V_{in} = 2.5 V to 5.5 V f_{out} = 1.0 MHz min, 5.0 MHz max

DUAL VOLTAGE-CONTROLLED MULTIVIBRATOR



L SUFFIX CERAMIC PACKAGE CASE 632 (TO-116)

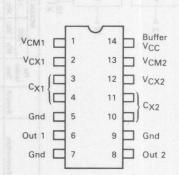
F SUFFIX CERAMIC PACKAGE CASE 607





P SUFFIX
PLASTIC PACKAGE
CASE 646
(MC4024 only)

PIN ASSIGNMENT



7-20

Power Supply Drain

1.3.14

37

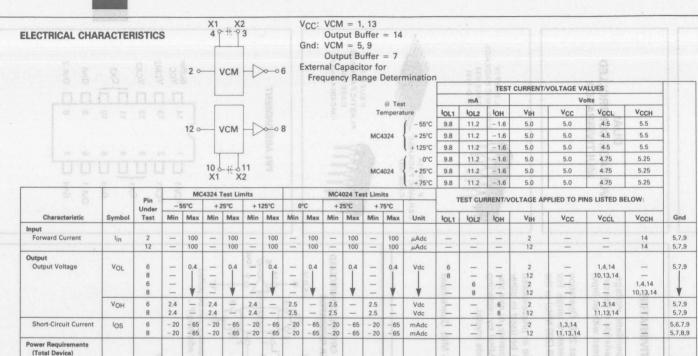


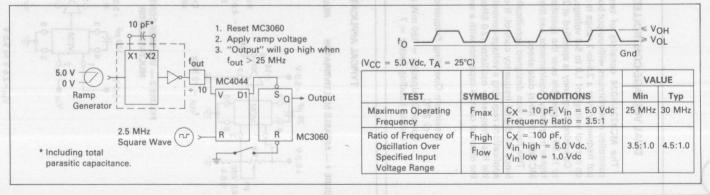
FIGURE 4 — AC TEST CIRCUIT AND WAVEFORMS

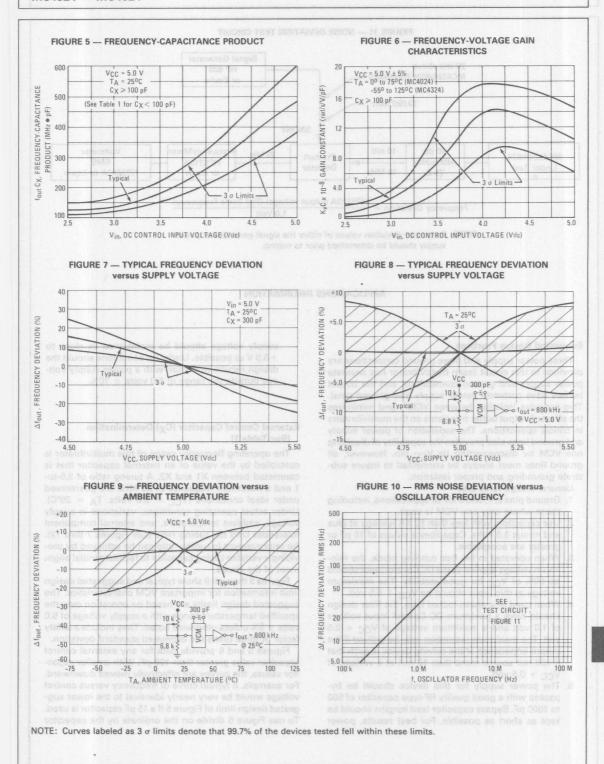
mAdc

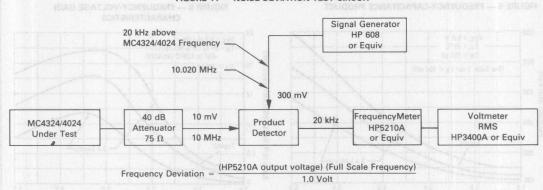
2,4,10,12

1,13,14

5,7,9







NOTE: Frequency deviation values of either the signal generator or power supply should be determined prior to testing.

APPLICATIONS INFORMATION

Suggested Design Practices

Three power supply and three ground connections are provided in this circuit (each multivibrator has separate power supply and ground connections, and the output buffers have common power supply and ground pins). This provides isolation between VCM's and minimizes the effect of output buffer transients on the multivibrators in critical applications. The separation of power supply and ground lines also provides the capability of disabling one VCM by disconnecting its VCC pin. However, all ground lines must always be connected to insure substrate grounding and proper isolation.

General design rules are:

- Ground pins 5, 7, and 9 for all applications, including those where only one VCM is used.
- Use capacitors with less than 50 nA leakage at plus and minus 3.0 volts. Capacitance values of 15 pF or greater are acceptable.
- When operated in the free running mode, the minimum voltage applied to the DC Control input should be 60% of V_{CC} for good stability. The maximum voltage at this input should be V_{CC} + 0.5 volt.
- 4. When used in a phase-locked loop, the filter design should have a minimum DC Control input voltage of 1.0 volt and a maximum voltage of V_{CC} + 0.5 volt. The maximum restriction may be waived if the output impedance of the driving device is such that it will not source more than 10 mA at a voltage of V_{CC} + 0.5 volt.
- The power supply for this device should be bypassed with a good quality RF-type capacitor of 500 to 1000 pF. Bypass capacitor lead lengths should be kept as short as possible. For best results, power

supply voltage should be maintained as close to +5.0 V as possible. Under no conditions should the design require operation with a power supply voltage outside the range of 5.0 volts \pm 10%.

External Control Capacitor (C_X) Determination (See Table 1)

The operating frequency range of this multivibrator is controlled by the value of an external capacitor that is connected between X1 and X2. A tuning ratio of 3.5-to-1 and a maximum frequency of 25 MHz are guaranteed under ideal conditions (VCC = 5.0 volts. $T_A = 25^{\circ}\text{C}$). Under actual operating conditions, variations in supply voltage, ambient temperature, and internal component tolerances limit the tuning ratio (see Figures 7 thru 12). An improvement in tuning ratio can be achieved by providing a variable tuning capacitor to facilitate initial alignment of the circuit.

Figures 5 through 9 show typical and suggested design limit information for important VCM characteristics. The suggested design limits are based on operation over the specified temperature range with a supply voltage of 5.0 volts \pm 5% unless otherwise noted. They include a safety factor of three times the estimated standard deviation.

Figures 5 and 6 provide data for any external control capacitor value greater than 100 pF. With smaller capacitor values, the curves are effectively moved downward. For example, a typical curve of frequency versus control voltage would be very nearly identical to the lower suggested design limit of Figure 5 if a 15 pF capacitor is used. To use Figure 5 divide on the ordinate by the capacitor

TABLE 1 — EXTERNAL CONTROL CAPACITOR VALUE DETERMINATION

CONFICURATION				1	VALUES OF	K	
CONFIGURATION	TA	Vcc	K1	K2	КЗ	K4	K5
$ \begin{array}{c c} C_X & \\ \hline X_1 & X_2 \\ \hline \end{array} $ With $C_X = \frac{K_1}{f_{OH}} - 5$,	suraliza un	5.0 V	385	150	600	110	1.0
$V_{in} \circ \circ f_{out} = \frac{V_{OH}}{f_{OL}} \le \frac{K2}{C_X}$	25°C ± 3°C	5.0 V ±5%	325	175	680	125	1.14
CXV		5.0 V ± 10%	290	190	750	140	1.25
$ \begin{array}{c c} \hline CXF \end{array} $ $ CX = CXV + CXF $	Ja L	5.0 V	335	165	660	120	1.10
Vin o— of fout	0°C to 75°C	5.0 V ±5%	280	190	750	140	1.25
Choose C _{XF} and C _{XV} such that C _X can be adjusted to:		5.0 V ± 10%	250	200	840	150	1.40
$\frac{K1}{fOH} - 5 \leqslant C \chi \leqslant \frac{K3}{fOH} - 5$	I	5.0 V	300	175	690	125	1.15
With $V_{\text{in}} = V_{\text{CC}} = 5.0 \text{ V}$, adjust C_{X} to obtain: $f_{\text{out}} = K5 (f_{\text{OH}})$ Then:	-55°C to 125°C	5.0 V ± 5%	260	200	780	145	1.30
$f_{OL} \leq \frac{K4}{K1} f_{OH}$		5.0 V ± 10%	230	210	860	155	1.45

Definitions: $f_{OH} = \text{Output frequency with V}_{in} = \text{V}_{CC}$ $f_{OL} = \text{Output frequency with V}_{in} = 2.5 \text{ V}$ (Frequencies in MHz, C_X in pF)

value in picofarads to obtain output frequency in megahertz. In Figure 6 the ordinate axis is multiplied by the capacitor value in picofarads to obtain the gain constant (Ky) in radians/second/volt.

Frequency Stability

When the MC4324/4024 is used as a fixed-frequency oscillator (V_{in} constant), the output frequency wll vary slightly because of internal noise. This variation is indicated by Figure 10 for the circuit of Figure 11. These variations are relatively independent (< 10%) of changes in temperature and supply voltage.

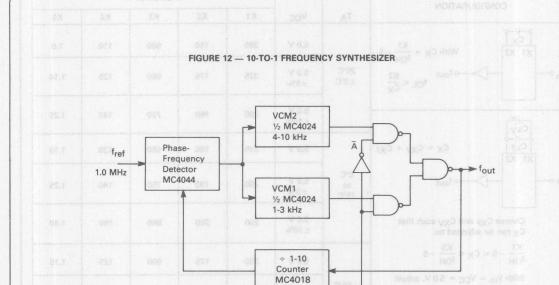
10-to-1 Frequency Synthesizer

A frequency synthesizer covering a 10-to-1 range is shown in Figure 14. Three packages are required to complete the loop: The MC4344/4044 phase-frequency detector, the MC4324/4024 dual voltage-controlled multivibrator, and the MC4318/4018 programmable counter.

Two VCM's (one package) are used to obtain the required frequency range. Each VCM is capable of operating over a 3-to-1 range, thus VCM1 is used for the lower portion of the times ten range and VCM2 covers the upper end. The proper divide ratio is set into the programmable counter and the VCM for that frequency is selected by control gates. The other VCM is left to be free running since its output is gated out of the feedback path.

Normally with a single VCM the loop gain would vary over a 10-to-1 range due to the range of the counter ratios. This affects the bandwidth, lockup time, and damping ratio severely. Utilizing two VCM's reduces this change in loop gain rom 10-to-1 to 3-to-1 as a result of the different sensitivities of the two VCM's due to the different requency ranges. This change of VCM sensitivity (3-to-1) is of such a direction of compensate for loop gain variations due to the programmable counter.

The overall concept of multi-VCM operation can be expanded for ranges greater than 10-to-1. Four VCM's (two packages) could be used to cover a 100-to-1 range.



D3 D2 D1 D0

fout	VCM2	VCM1			ut	Inp		
kHz	kHz	kHz	Α	D0	D1	D2	D3	÷N
	X	1	1	1	0	0	0	987 81
	X	2	1	0	1	0	0	2
3	X	3	1	-10	101	0	0	3
4	4	X	0	0	0	1	0	4
5	5	X	0	1100	0	10\1 sr	0	5
6	6	X	0	0	201	0 1	0	6
7	7	X	0	1 de	and a	1 1	0	7
8	8	X	0	0	0	0	V 1 and	8
9	9	X	0	1	0	0	1	9
10	10	X	0	0	1	0	1	10



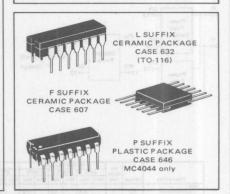
MC4344/ MC4044

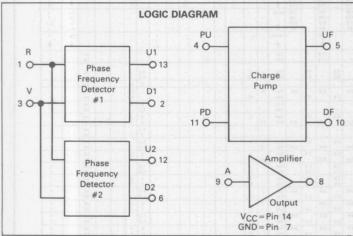
PHASE-FREQUENCY DETECTOR

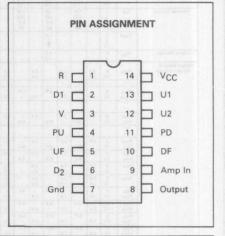
The MC4344/4044 consists of two digital phase detectors, a charge pump, and an amplifier. In combination with a voltage controlled multivibrator (such as the MC4324/4024 or MC1648), it is useful in a broad range of phase-locked loop applications. The circuit accepts TTL waveforms at the R and V inputs and generates an error voltage that is proportional to the frequency and/or phase difference of the input signals. Phase detector #1 is intended for use in systems requiring zero frequency and phase difference at lock. Phase detector #2 is used if quadrature lock is desired. Phase detector #2 can also be used to indicate that the main loop, utilizing phase detector #1, is out of lock.

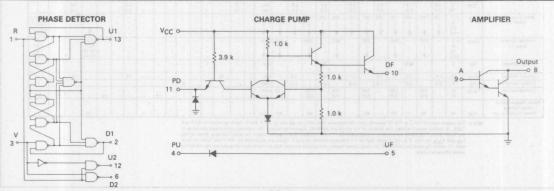
Input Loading Factor: R, V = 3
Output Loading Factor (Pin 8) = 10
Total Power Dissipation = 85 mW typ/pkg
Propagation Delay Time = 9.0 ns typ
(thru phase detector)

PHASE-FREQUENCY DETECTOR

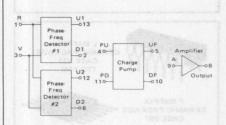








ELECTRICAL CHARACTERISTICS



INPUT	IN	TUP		OUT	PUT	
STATE	R	V	U1	D1	U2	D2
1	0	0	X	×	1	1
2	1	0	X	X	. 0	1
3	1	1	X	X	1	0
4	1	0	X	X	0	1
5	0	0	X	X	1	1
6	1	0	X	X	0	1
7	0	0	0	1	1	1
8	1	0	0	1	0	1
9	0	0	0	1	1	1
10	0	1	0	1	1	1
11	0	0	1	1	1	1
12	0	1	1	1	1	1
13	0	0	1	0	1	1
14	0	1	1	0	1	1
15	0	0	1	0	1	1
16	1	0	1	0	0	1
17	0	0	1	1	1	1

TRUTH TABLE

This is not strictly a functional truth table; i.e., it does not show all possible modes of operation. It is useful for dc testing.

- 1. X indicates output state unknown.
- 2. U1 and D1 outputs state unknown.
 i.e., they must be sequenced in order shown.
 3. U2 and D2 outputs are combinational; i.e., they need only inputs shown to obtain outputs.

						E31 C1	JKK	EN I/	VOLTA	GE VA	LUE	5			1
100			mA				0.1				Vo	ts			
Test erature	IOL	10Н1	IOH2	lin	IIC	IA	VIL	VIH	VIHH	VILT	VIHT	Vout	vcc	VCCL	VCCH
-55°C	20	-1.6	-1.0	-	-	0.002	0.4	2.4	-	1.1	2.0	1.5	5.0	4.5	5.5
+25°C	20	-1.6	-1.0	1.0	-10	0.002	0.4	2.4	5.5	1.1	1.8	1.5	5.0	4.5	5.5
125°C	20	-1.6	-1.0	-	-	0.002	0.4	2.4	-	0.9	1.8	1.5	5.0	4.5	5.5
0°C	20	-1.6	-1.0	(2)	433	0.002	0.4	2.5	8	1.1	2.0	1.5	5.0	4.75	5.25
+25°C	20	-1.6	-1.0	1.0	-10	0.002	0.4	2.5	5.5	1.1	1.8	1.5	5.0	4.75	5.25
+75°C	20	-1.6	-1.0	545	-	0.002	0.4	2.5	10027	0.9	1.8	1.5	5.0	4.75	5.25
	-55°C +25°C 125°C 0°C +25°C	erature OL -55°C 20 +25°C 20 125°C 20 0°C 20 +25°C 20	erature OL OH1 -55°C 20 -1.6 +25°C 20 -1.6 125°C 20 -1.6 0°C 20 -1.6 +25°C 20 -1.6	erature OL OH1 OH2 -65°C 20 -1.6 -1.0 +25°C 20 -1.6 -1.0 -1.0 -1.0 -1.0 -1.0 -1.0 -1.0 -1.0 -1.0 +25°C 20 -1.6 -1.0 -1.0 -1.0 -1.0 -1.0 -1.0 -1.0 -1.0 -1.0 -1.0 -1.0 -1.0 -1.0 -1.0 -1.0 -1.0 -1.0 -1.0 -1.0 -1.0 -1.0 -1.0 -1.0 -1.0 -1.0 -1.0 -1.0 -1.0 -1.0 -1.0 -1.0 -1.0 -1.0 -1.0 -1.0 -1.0 -1.0 -1.0 -1.0 -1.0 -1.0 -1.0 -1.0 -1.0 -1.0 -1.0 -1.0 -1.0 -1.0 -1.0 -1.0 -1.0 -1.0 -1.0 -1.0	erature OL OH1 OH2 In -55°C 20 -1.6 -1.0 -1.0 -1.25°C 20 -1.6 -1.0	erature OL OH1 OH2 Im ICC -55°C 20 -1.6 -1.0 - -25°C 20 -1.6 -1.0 -1.0 -125°C 20 -1.6 -1.0 - -25°C 20 -1.6 -1.0 -1.0 -20 -1.6 -1.0 -1.0 -20 -1.6 -1.0 -1.0 -25°C 20 -1.6 -1.0 -25°C 20 -1.6 -1.0 -1.0 -25°C 20 -1.6 -1.0 -25°C 20 -1.0 -25°C 20 -1.0 -1.0 -25°C 20 -1.0 -1.0 -	### 101 0H1 0H2 1n 1C 1A -55°C 20 1.6 -1.0 -1 0.002 -55°C 20 1.6 -1.0 1.0 1.0 -55°C 20 1.6 -1.0 -1 0.002 -55°C 20 1.6 -1.0 -1 0.002 -55°C 20 1.6 -1.0 1.0 0.002 -55°C 20 1.6 -1.0 1.0 0.002	######################################	No. No.	######################################	Nature 10,	######################################	######################################	######################################	######################################

	Levis	Pin	- 1	MC	4344	Test Lin	mits			Mo	4044	Test L	mits					TEC	T CIT	DOCA	TAIC		CF 40	01 150	TO DI	NIC C	STED	nrı ou			1
	- SOR	Under	-5	5°C	+2	5°C	+12	25°C	0	ос	+2	5°C	+7	5°C	T	1	-	TES	T	THEN	1770	LIM	GE AF	FLIED	TOPI	NS LI	SIEDI	BELUV	V.	-	4
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	lor	ГОН1	1 _{OH2}	lin	IIC	IA	VIL	VIH	VIHH	VILT	VIHI	Vout	Vcc	VCCL	VCCH	G
nput Forward Current	TIL	1	-	-48	-	-4.8	020	-4.8	-	-48	-	-4.8	-	-4.8	mAdc	-	anni.	-	172	-	-	1			1000	-		-		14	
		3	-	-4.8	1.3	-4.8		-4.8	-	-4.8	-	-4.8	-	-4.8	1	2	-	-	-		-	3	-	-	-	-	-			+	
Leakage Current	1	1	-	-1.6 120	-	120	-	120	-	-1.6	-	-1.6	-	-1.6	¥	-	-	-	-	-	-	11	-	-	-	-	-		-		+
Leakage Current	ЧН	3	-	120	-	120	-	120	It.	120	-	120	-	120	μAdc	1		-	13	1		1	3	HO	33	1				14	
	MANA	11	A.	5.0	-	5.0	-	5.0	-	5.0	-	5.0	145	5.0		-	-	-	1	-	-	-	-	-		-				4	
	Тінн	1	-	40	-	1.0	-	40	1	40	1	1.0	- 1	40	mAdc	-	1	-	-	100	1	-	11	1		-				14	-
		3	-	-	1	+		-	1	-	-			-	1	-	-	-	-	34		-	-	3	1					1	1
Clamp Voltage	VIC	11		-	-	-15	-	-	1	-	100	-1.5	2	1	Vdc	-	-	-	-	1	*	-	-	11	-	1			14	,	-
and total	*IC	3	-	-	10	-1.5	-	-		-	-	-1.5	-	-	Vdc	-	-	-	0	3		1	-	-	-	1	-	-	14		
Output (Note 1) Output Voltage				2								153								N.						13		183	19	- 3	
Output voltage	VOH	12	2.4	1	24	-	2.4		2.5		2.5	-	2.5	-	Vdc Vdc	10	6		12	-	-				1,3				14		
		-	-	100	-	-	-	-	14	-	-	-	-	-		-	1		-	-	12	100	-	-	3	1		1	14		
	VOL	6	2.4	0.4	-	0.4	. 3.	0.4	14	0.4	3.	0.4	-3	0.4	Vdc	6	-	-	-	=	-	-	-	40	1	1,3	- 34	21/20	14	- 1	
	VOH	12	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	Vdc	-	12	-	-	-	-	-	-	-	3	1,3	-	150	14		
		-	-	-	-	-	-	-	-		-	-		-	Vdc	-	-		-	-			-	-	1,3	13			14		
	VOH	6	2.4	-	2.4	-	2.4	-	2.5	1-1	2.5	-	2.5	-	Vdc	-	6	-	-	1	-	-	-	-	3	1			14		
	VOL	12	-	0.4	-	0.4	-	0.4	-	0.4	IF.	0.4	-	0.4	Vdc	12	-	-	-	18.	7	-	-	-	1.3	1			14	77	
	1	-	-	-	-	4 -	-	-	L	-	-	-	-	-	1	-	2	-	-	-	-	-	-	-	3	1			14	12 1	
	VOH	13	2.4	0.4	2.4	0.4	2.4	0.4	2.5	0.4	2.5	0.4	2.5	0.4	Vdc	13	2	-	-	-	-	-	-	-	1,3	-7	-	and the same of	14		
	VOH	2	2.4	0.4	2.4	0.4	2.4	0.4	2.5	0.4	2.5	0.4	2.5	0.4	Vdc	13	2	-	-	-	-	-	-	- 5	1,3	3		-	14		
	VOL	13	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	13	1	100	5	-				01-10	1	3	-		14	3	
	VOH	13	2.4		2.4	10	2.4	3	2.5	-	2.5		2.5		Vdc Vdc	-	13		-		-		-	-	1,3	-			14		
	VOH	2	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-1	2.5	-	Vdc	-	2		1-0	-	-	-		-	1	3		1	14	1.1	
	VOL	13	2.4	0.4	2.4	0.4	2.4	0.4	2.5	0.4	2.5	0.4	2.5	-	Vdc	-	13		-29	-	-	-	-	- 2	1	3		0.594	14		
	VOH	13	24	0.4	2.4	0.4	2.4	0.4	2.5	0,4	2.5	0.4	2.5	0.4	Vdc Vdc	2	13		-	Ī					1,3			- 23	14		
	VOL	2		0.4	-	0.4	-	0.4	-	0.4	100	0.4	7.5	0.4	Vdc	2	13	-	-	-	-	-	-	-	1	3	-		14		
	VOH	13	2.4	0.4	2.4	0.4	2.4	0.4	2.5	0.4	2.5	0.4	2.5	0.4	Vdc Vdc	2	13	-	-	-	-	~	-	-	1,3	3			14		
	VOH	13	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	Vdc	-	13		-			-	-		1,3		-		14		
	VOL	13	2.4	0.4	2.4	0.4	2.4	0.4	26	0.4	25	0.4	2.5	0.4	Vdc	2	12	4	-5	-		-	-	*	3	1			14		
	VOH	2	2.4		24	-	2.4	-	2.5	-	2.5	-7-1	2.5		Vdc Vdc	-	13	-	100	100	-	-		C.F.	1.3	1			14		1
	-011	13	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	Vdc	-	13		-	-		-	-	-	1,3		1		14		1
Short Circuit Current (Note 1)	los	• 2	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	mAdc	-						-	-	-	-	-	194	14		202	2,3,
		12									11					-						-			-			1			1,3,6
		* 13	*	4	- 9	4	4	4	-	4	4-	4	4	4		-	-	-	-	-	-	-1	-	-	-	- 1		4			1,3,7
(Note 1)	IOLK	• 2	-	250		250	-	250	1	250		250		250.	µAdc	-		-	3		3	3	-	-	-			2,14 6,14			1,3
		12	-		-				-							-						-	-	-		-	. 1	12,14			1,3
Diode Voltage	VF	*13	-	- 1	0.5	7	1.7	-	-		0.5		-	,	Vdc	-	- 1	0 1	5	-	-	-		-	-	-		13,14		1	1,3
								in el				1							-						200						34
Output Voltage	VEH	10	1.5		1.5	-	1.5	-	1.5	183	15	-	1.5	-	Vdc	-	-	10	-	-	-	-	-	-	11	- 1	17.	-	14	10	7
Output Current Leakage Current	10	8	0.2	120	0.8	120	1.0	120	0.5	- 120	0.8	- 120	1.0	- 100	mAdc	-		4	-	-	9	-	-	-	-	-	-	-	-	8	7
cranage current	OLK	10	-	5.0	-	5.0		120 5.0	-	120 5.0	-	120	. 5	120	µAdc µAdc	1	-	-	-	7	-	-	11	-		-	10		-	8	7.5
ower Requirements (Total Device) Power Supply Drain	lcc	14		40		40		40		40		40		40	mAdc					1								14			7

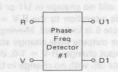
Note 1. The output state of Pin 2 or Pin 13 depends upon the securace that has been applied to the R and V inputs as shown in the Truth Table. In testing output voltage, the outputs of the device are tested by sequencing through the indicated input states according to the Truth Table. Procedures centerfied by a double astersis (**) are necessary to change the state of the sequential logic. When Table 10 produces acreased to the R and V inputs are sequenced per the Truth Table to input state 11 where the tests are performed. All nonly, power supply, and ground voltages must be maintained while sequencing and the se

APPLICATION

Operation of the MC4344/4044 is best explained by initially considering each section separately. If phase detector #1 is used, loop lockup occurs when both outputs U1 and D1 remain high. This occurs only when all the negative transitions on R, the reference input, and V, the variable or feedback input, coincide. The circuit responds only to transitions, hence phase error is independent of input waveform duty cycle or amplitude variation. Phase detector #1 consists of sequential logic circuitry, therefore operation prior to lockup is determined by initial conditions.

When operation is initiated, by either applying power to the circuit or active input signals to R and V, the circuitry can be in one of several states. Given any particular starting conditions, the flow table of Figure 1 can be used to determine subsequent operation. The flow table indicates the status of U1 and D1 as the R and V inputs are varied. The numbers in the table which are in parentheses are arbitrarily assigned labels that correspond to stable states that can result for each input combination. The numbers without parentheses refer to unstable conditions. Input changes are traced by horizontal movement in the table; after each input change, circuit operation will settle in the numbered state indicated by moving horizontally to the appropriate R-V column. If the number at that location is not in parentheses, move vertically to the number of the same value that is in parentheses. For a given input pair, any one of three stable states can exist. As an example, if R = 1 and V = 0, the circuit will be in one of the stable states (4), (8), or (12).

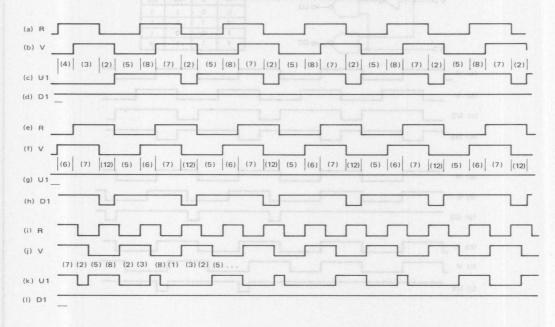
FIGURE 1 - PHASE DETECTOR #1 FLOW TABLE



R-V	R-V	R-V	R-V	P. P. IV	0.4
0-0	0-1	1-1	1-0	U1	D1
(1)	2	3	(4)	0	1
5	(2)	(3)	8	0	11
(5)	6	7	8	1	1
9	(6)	7	12	1	1
5	2	(7)	12	1	1
.1	2	7	(8)	1	+1
(9)	(10)	11	12	1	0
5	6	(11)	(12)	1	0

Use of the table in determining circuit operation is illustrated in Figure 2. In the timing diagram, the input to R is the reference frequency; the input to V is the same frequency but lags in phase. Stable state (4) is arbitrarily assumed as the initial condition. From the timing diagram and flow table, when the circuit is in stable state (4), outputs U1 and D1 are "0" an "1" respectively. The next input state is R-V = 1-1; moving horizontally from stable state (4) under R-V = 1-0 to the R-V = 1-1 column, state 3 is indicated. However, this is an unstable condition and the circuit will assume the state indicated by moving vertically in the R-V = 1-1 column to stable state (3). In this

FIGURE 2 — PHASE DETECTOR #1 TIMING DIAGRAM



mistarios, outputs or and Dr remain unchanged. The input states next become R-V = 0-1; moving horizontally to the R-V = 0-1 column, stable state (2) is indicated. At this point there is still no change in U1 or D1. The next input change shifts operation to the R-V = 0-0 column where unstable state 5 is indicated. Moving vertically to stable state (5), the outputs now change state to U1-D1 = 1-1. The next input change, R-V = 1-0, drives the circuitry to stable state (8), with no change in U1 or D1. The next input, R-V = 1-1, leads to stable state (7) with no change in the outputs. The next two input state changes cause U1 to go low between the negative transitions of R and V. As the inputs continue to change, the circuitry moves repeatedly through stable states (2), (5), (8), (7), (2), etc., as shown, and a periodic waveform is obtained on the U1 terminal while D1 remains high.

A similar result is obtained if V is leading with respect to R, except that the periodic waveform now appears on D1 as shown in rows e-h of the timing diagram of Figure 2. In each case, the average value of the resulting waveform is proportional to the phase difference between the two inputs. In a closed loop application, the error signal for controlling the VCO is derived by translating and filtering these waveforms.

The results obtained when R and V are separated by a fixed frequency difference are indicated in rows i-I of the timing system. For this case, the U1 output goes low when R goes low and stays in that state until a negative transition on V occurs. The resulting waveform is similar

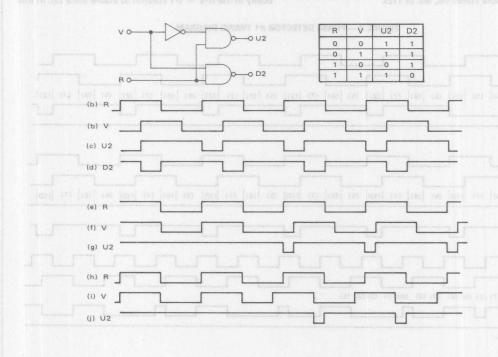
to the fixed phase difference case, but now the duty cycle of the U1 waveform varies at a rate proportional to the difference frequency of the two inputs, R and V. It is this characteristic that permits the MC4344/4044 to be used as a frequency discriminator; if the signal on R has been frequency modulated and if the loop bandwidth is selected to pass the deviation frequency but reject R and V, the resulting error voltage applied to the VCO will be the recovered modulation signal.

Phase detector #2 consists only of combinatorial logic, therefore its characteristics can be determined from the simple truth table of Figure 3. Since circuit operation requires that both inputs to the charge pump either be high or have the same duty cycle when lock occurs, using this phase detector leads to a quadrature relationship between R and V. This is illustrated in rows a–d of the timing diagram of Figure 3. Note that any deviation from a fifty percent duty cycle on the inputs would appear as phase

Waveforms showing the operation of phase detector #2 when phase detector #1 is being used in a closed loop are indicated in rows e-j. When the main loop is locked, U2 remains high. If the loop drifts out of lock in either direction a negative pulse whose width is proportional to the amount of drift appears on U2. This can be used to generate a simple loss-of-lock indicator.

Operation of the charge pump is best explained by considering it in conjunction with the Darlington amplifier included in the package (see Figure 4). There will be

FIGURE 3 — PHASE DETECTOR #2 OPERATION



a pulsed waveform on either PD or PU, depending on the phase-frequency relationship of R and V. The charge pump serves to invert one of the input waveforms (D1) and translates the voltage levels before they are applied to the loop filter. When PD is low and PU is high, Q1 will be conducting in the normal direction and Q2 will be off. Current will be flowing through Q3 and CR2; the base of Q3 will be two VRF drops above ground or approximately 1.5 volts. Since both of the resistors connected to the base of Q3 are equal, the emitter of Q4 (base of Q5) will be approximately 3.0 volts. For this condition, the emitter of Q5 (DF) will be on VBE below this voltage, or about 2.25 volts. The PU input to the charge pump is high (> 2.4 volts) and CR1 will be reverse biased. Therefore Q5 will be supplying current to Q6. This will tend to lower the voltage at the collector of Q7, resulting in an error signal that lowers the VCO frequency as required by a "pump down" signal.

FIGURE 4 — CHARGE PUMP OPERATION

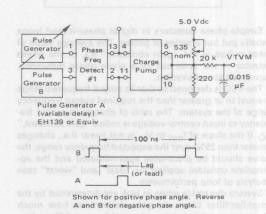
When PU is low and PD is high, CR1 is forward biased and UF will be approximately one VBE above ground (neglecting the VCE(sat) of the driving gate). With PD high, Q1 conducts in the reverse direction, supplying base current for Q2. While Q2 is conducting, Q4 is prevented from supplying base drive to Q5; with Q5 cut off and UF low there is no base current for Q6 and the voltage at the collector of Q7 moves up, resulting in an increase in the VCO operating frequency as required by a "pump up" signal.

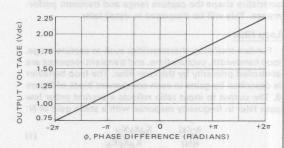
If both inputs to the charge pump are high (zero phase difference), both CR1 and the base-emitter junction of $\Omega 5$ are reverse biased and there is no tendency for the error voltage to change. The output of the charge pump varies between one VBE and three VBE as the phase difference of R and V varies from minus 2π to plus 2π . If this signal is filtered to remove the high-frequency components, the phase detector transfer function, K_{ϕ} , of approximately 0.12 volt/radian is obtained (see Figure 5).

The specified gain constant of 0.12 volt/radian may not be obtained if the amplifier/filter combination is improperly designed. As indicated previously, the charge pump delivers pump commands of about 2.25 volts on the positive swings and 0.75 volt on the negative swings for a mean no-pump value of 1.5 volts. If the filter amplifier is biased to threshold "on" at 1.5 volts, then the pump up

and down voltages have equal effects. The pump signals are established by VBFs of transistors with milliamperes of current flowing. On the other hand, the transistors included for use as a filter amplifier will have very small currents flowing and will have correspondingly lower VBEs — on the order of 0.6 volt each for a threshold of 1.2 volts. Any displacement of the threshold from 1.5 volts causes an increase in gain in one direction and a reduction in the other. The transistor configuration provided is hence not optimum but does allow for the use of an additional transistor to improve filter response. This addition also results in a non-symmetrical response since the threshold is now approximately 1.8 volts. The effective positive swing is limited to 0.45 volt while the negative swing below threshold can be greater than 1.0 volt. This means that the loop gain when changing from a high frequency to a lower frequency is less than when changing in the opposite direction. For type two loops this tends to increase overshoot when going from low to high and increases damping in the other direction. These problems and the selection of external filter components are intimately related to system requirements and are discussed in detail in the filter design section.

FIGURE 5 — PHASE DETECTOR TEST





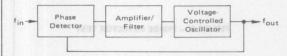
PHASE-LOCKED LOOP COMPONENTS General

A basic phase-locked loop, when operating properly, will acquire ("lock on") an input signal, track it in frequency, and exhibit a fixed phase relationship relative to the input. In this basic loop, the output frequency will be identical to the input frequency (Figure 6). A fundamental loop consists of a phase detector, amplifier/filter, and voltage-controlled oscillator (Figure 7). It appears and acts like a unity gain feedback loop. The controlled variable is phase; any error between fin and fout is amplified and applied to the VCO in a corrective direction.

FIGURE 6 — BASIC PHASE-LOCKED LOOP FREQUENCY RELATIONSHIP



FIGURE 7 — FUNDAMENTAL PHASE-LOCKED LOOP



Simple phase detectors in digital phase-locked loops usually put out a series of pulses. The average value of these pulses is the "gain constant," K_{ϕ} , of the phase detector — the volts out for a given phase difference, expressed as volts/radian.

The VCO is designed so that its output frequency range is equal to or greater than the required output frequency range of the system. The ratio of change in output frequency to input control voltage is called "gain constant," K_O. If the slope of fout to V_{in} is not linear (i.e., changes greater than 25%) over the expected frequency range, the curve should be piece-wise approximated and the appropriate constant applied for "best" and "worst" case analysis of loop performance.

System dynamics when in lock are determined by the amplifier/filter block. Its gain determines how much phase error exists between fin and fout, and filter characteristics shape the capture range and transient performance. This will be discussed in detail later.

Loop Filter

Fundamental loop characteristics such as capture range, loop bandwidth, capture time, and transient response are controlled primarily by the loop filter. The loop behavior is described by gains in each component block of Figure 8. The output to input ratio reflects a second order low pass filter in frequency response with a static gain of N:

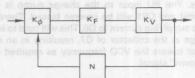
$$\frac{\theta_{O}(s)}{\theta_{\tilde{I}}(s)} = \frac{K_{\phi}K_{F}K_{V}}{s + \frac{K_{\phi}K_{F}K_{V}}{N}}$$
(1)

where: $K_F = \frac{1 + T_1 s}{T_2 s}$ (2)

 $T_1 = R_2C$ and $T_2 = R_1C$ of Figure 4. Therefore

$$\frac{\theta_{O}(s)}{\theta_{I}(s)} = \frac{N(1 + T_{1}s)}{\frac{s^{2}NT_{2}}{K_{A}K_{V}} + T_{1}s + 1}$$
(3)

FIGURE 8 — GAIN CONSTANTS



 K_{ϕ} = Phase Detector Gain (volts/radian)

K_F = Amplifier/Filter Gain

Ky = VCO Gain (radians/second/volt)

N = Integer Divisor

Both ω_n (loop bandwidth or natural frequency) and ζ (damping factor) are particularly important in the transient response to a step input of phase or frequency (Figure 9), and are defined as:

$$\omega_n = \sqrt{\frac{K_\phi K_V}{NT_2}} \tag{4}$$

$$\zeta = \sqrt{\frac{K_{\phi}K_{V}}{NT_{2}}} \left(\frac{T_{1}}{2}\right) \tag{5}$$

Using these terms in Equation 3,

$$\frac{\theta_{O}(s)}{\theta_{I}(s)} = \frac{N(1 + T_{1}s)}{\frac{s^{2}}{\omega_{n}^{2}} + \frac{2\zeta s}{\omega_{n}} + 1}$$
(6)

In a well defined system controlling factors such as ω_n and ζ may be chosen either from a transient basis (time domain response) or steady state frequency plot (roll-off point and peaking versus frequency). Once these two design goals are defined, synthesis of the filter is relatively straight-forward.

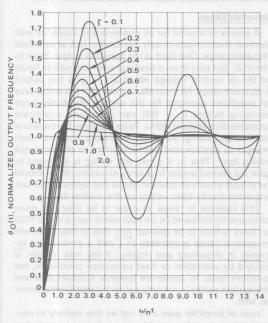
Constants $K_{d\nu}$, K_V , and N are usually fixed due to other design constraints, leaving T_1 and T_2 as variables to set ω_n and ζ . Since only T_2 appears in Equation 4, it is the easiest to solve for initially.

$$T_2 = \frac{K_\phi K_V}{N\omega_D^2} \tag{7}$$

From Equation 5, we find

$$T_1 = \frac{2\zeta}{\omega_n} \tag{8}$$





Using relationships 7 and 8, actual resistor values may be computed:

$$R_1 = \frac{K\phi K_V}{N\omega_D^2 C}$$
 (9)

$$R_2 = \frac{2\zeta}{\omega_n C} \tag{10}$$

Although fundamentally the range of R_1 and R_2 may be from several hundred to several thousand ohms, sideband considerations usually force the value of R_1 to be set first, and then R_2 and C computed.

$$C = \frac{K_{\phi}K_{V}}{N\omega_{n}^{2}R_{1}} \tag{11}$$

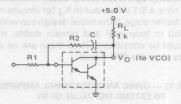
Calculation of passive components R_2 and C (in synthesizers) is complicated by incomplete information on N, which is variable, and the limits of ω_{Π} and ζ during that variance. Equally important are changes in K_V over the output frequency range. Minimum and maximum values of ω_{Π} and ζ can be computed from Equations 4 and 5 when the appropriate worst case numbers are known for all the factors.

Amplifier/filter gain usually determines how much phase error exists between f_{in} and f_{out} , and the filter characteristic shapes capture range and transient performance. A relatively simple, low gain amplifier may usually be used in the loop since many designs are not constrained so much by phase error as by the need to make f_{in} equal f_{out} . Unnecessarily high gains can cause

problems in linear loops when the system is out of lock if the amplifier output swing is not adequately restricted since integrating operational amplifier circuits will latch up in time and effectively open the loop.

The internal amplifier included in the MC4344/4044 may be used effectively if its limits are observed. The circuit configuration shown in Figure 10 illustrates the placement of R_1 , R_2 , C, and load resistor R_L (1 $k\Omega$). Due to the non-infinite gain of this stage (Ay \approx 30) and other non-ideal characteristics, some restraint must be placed on passive component selection. Foremost is a lower limit on the value of R_2 and an upper limit on R_1 . Placed in order of priority, the recommendations are as follows: (a) $R2 > 50~\Omega$, (b) $R2/R1 \leqslant 10$, (c) 1 $k\Omega < R1 < 5~k\Omega$.

FIGURE 10 — USING MC4344/4044 LOOP AMPLIFIER



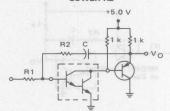
Limit (c) is the most flexible and may be violated with either higher sidebands and phase error $(R_1>5~k\Omega)$ or lower phase detector gain $(R_1<1~k\Omega)$. If limit (b) is exceeded, loop bandwidth will be less than computed and may not have any similarity to the prediction. For an accurate reproduction of calculated loop characteristics one should go to an operational amplifier which has sufficient gain to make limit (b) readily satisfied. Limit (a) is very important because T_1 in Equation 5 is in reality composed of three elements:

$$T_1 = C \left(R_2 - \frac{1}{g_m} \right) \tag{12}$$

where g_{m} = transconductance of the common emitter amplifier.

Normally g_m is large and T_1 nearly equals R_2C , but resistance values below 50 Ω can force the phase-compensating "zero" to infinity or worse (into the right half plane) and give an unstable system. The problem can be circumvented to a large degree by buffering the feedback with an emitter follower (Figure 11). Inequality (a) may then be reduced by at least an order of magnitude ($R_2 > 5 \Omega$) keeping in mind that electrolytic capacitors used

FIGURE 11 — AMPLIFIER CAPABLE OF HANDLING
LOWER R2



quency or interest (wn).

Larger values of R₁ may be accommodated by either using an operational amplifier with a low bias current (Ib < 1.0 μA) as shown in Figure 12 or by buffering the internal Darlington pair with an FET (Figure 13). It is vitally important, however, that the added device be operated at zero VGS. Source resistor R4 should be adjusted for this condition (which amounts to IDSS current for the FET). This insures that the overall amplifier input threshold remains at the proper potential of approximately two base-emitter drops. Use of an additional emitter follower instead of the FET and RA (Figure 14) gives a threshold near the upper limit of the phase detector charge pump, resulting in an extremely unsymmetrical phase detector gain in the pump up versus pump down mode. It is not unusual to note a 5:1 difference in Ko for circuits having the bipolar buffer stage. If the initial design can withstand this variation in loop gain and remain stable, the approach should be considered since there are no critical adjustments as in the FET circuit.

FIGURE 12 — USING AN OPERATIONAL AMPLIFIER TO EXTEND THE VALUE OF R1

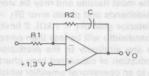


FIGURE 13 — FET BUFFERING TO RAISE AMPLIFIER INPUT IMPEDANCE

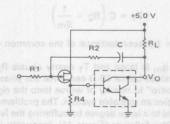
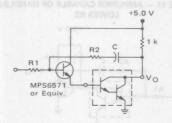


FIGURE 14 — EMITTER FOLLOWER BUFFERING OF AMPLIFIER INPUT



Dynamic Range

A source of trouble for all phase-locked loops, as well as most electronics is simply overload or lack of sufficient dynamic range. One limit is the amplifier output drive to the VCO. Not only must a designer note the outside limits of the dc control voltage necessary to give the output frequency range, he must also account for the worst case of overshoot expected for the system. Relatively large damping factors ($\zeta=0.5$) can contribute significant amounts of overshoot (30%). To be prepared for the worst case output swing the amplifier should have as much margin to positive and negative limits as the expected swing itself. That is, if a two-volt swing is sufficient to give the desired output frequency excursion, there should be at least a two-volt cushion above and below maximum expected steady-state values on the control line.

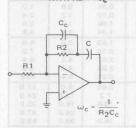
This increase in range, in order to be effective, must of course by followed by an equivalent range in the VCO or there is little to be gained. Any loss in loop gain will in general cause a decrease in ζ and a consequent increase in overshoot and ringing. If the loss in gain is caused by saturation or near saturation conditions, the problem tends to accelerate towards a situation where the system settles in not only a slow but oscillator manner as well.

Loss of amplifier gain may not be due entirely to normal system damping considerations. In loops employing digital phase detectors, an additional problem is likely to appear. This is due to amplifier saturation during a step input when there is a maximum phase detector output simultaneous with a large transient overshoot. The phase detector square wave rides on top of the normal transient and may even exceed the amplifier output limits imposed above. Since the input frequency will exceed the R2C time constant, gain KF for these annoying pulses will be R₂/R₁. Ordinarily this ratio will be less than 1, but some circumstances dictate a low loop gain commensurate with a fairly high ω_n . For these cases, R_2/R_1 may be higher than 10 and cause pulse-wise saturation of the amplifier. Since the dc control voltage is an average of phase detector pulses, clipping can be translated into a reduction in gain with all the "benefits" already outlined, i.e., poor settling time. An easy remedy to apply in many cases is a simple RC low pass section preceding or together with the integrator-lag section. To make transient suppression independent of amplifier response, the network may be imbedded within the input resistor R1 (Figure 15) or be implemented by placing a feedback capacitor across R2 (Figure 16). Besides rounding off and inhibiting pulses, these networks add an additional pole to the loop and may cause further overshoot if the cutoff frequency (ω_{C}) is too close to $\omega_{\Pi}.$ If at all possible the cutoff point should be five to ten times ω_n . How far ω_c can be placed from ω_n depends on the input frequency relationship to ω_n since f_{in} is, after all, what is being filtered. A side benefit of this simple RC pulse "flattener" is a reduction in fin sidebands around fout for synthe-

sizers with N > 1. However, a series of RC filters is not recommended for either extended pulse suppression or sideband improvement as excess phase will begin to build up at the loop crossover ($\approx \omega_n$) and tend to cause instability. This will be discussed in more detail later.

FIGURE 15 — IMPROVED TRANSIENT SUPPRESSION WITH R1 — $C_{\rm G}$

FIGURE 16 — IMPROVED TRANSIENT SUPPRESSION WITH R2 — $C_{\rm C}$



Spurious Outputs

Although the major problem in phase-locked loop design is defining loop gain and phase margin under dynamic operating conditions, high-quality synthesizer designs also require special consideration to minimize spurious spectral components — the worst of which is reference-frequency sidebands. Requirements for good sideband suppression often conflict with other performance goals — loop dynamic behavior, suppression of VCO noise, or suppression of other in-loop noise. As a result, most synthesizer designs require compromised specifications. For a given set of components and loop dynamic conditions, reference sidebands should be predicted and checked against design specifications before any hardware is built.

Any steady-state signal on the VCO control will produce sidebands in accordance with normal FM theory. For small spurious deviations on the VCO, relative sideband-to-carrier levels can be predicted by:

$$\frac{\text{sidebands}}{\text{carrier}} \cong \frac{V_{\text{ref}}K_{\text{V}}}{2\omega_{\text{ref}}}$$
 (13)

where $V_{\text{ref}} = \text{peak voltage value of spurious frequency}$ at the VCO input.

Unwanted control line modulation can come from a variety of sources, but the most likely cause is phase detector pulse components feeding through the loop fil-

ter. Although the filter does establish loop dynamic conditions, it leaves something to be desired as a low pass section for reference frequency components.

For the usual case where ω_{ref} is higher than 1/T₂, the K_F function amounts to a simple resistor ratio:

$$K_F(j\omega)$$
 $\cong -\frac{R_2}{R_1}$ (14) $\omega = \omega_{ref}$

By substitution of Equations 9 and 10, this signal transfer can be related to loop parameters.

$$K_{F}(j\omega) = \frac{2\zeta N\omega_{\Pi}}{K_{\phi}K_{V}} = \frac{V_{ref}}{V_{\phi}}$$

$$\omega = \omega_{ref}$$
(15)

where V_{ref} = peak value of reference voltage at the VCO input, and

 V_{ϕ} = peak value of reference frequency voltage at the phase detector output.

Sideband levels relative to reference voltage at the phase detector output can be computed by combining Equations 13 and 15:

$$\frac{\text{sideband level}}{\text{f}_{\text{out level}}} = V_{\phi} \left(\frac{\zeta N \omega_n}{\omega_{\text{ref}} K_{\phi}} \right) \tag{16}$$

From Equation 16 we find that for a given phase detector, a given value of R_1 (which determines V_ϕ), and given basic system constraints (N, f_{ref}), only ζ and ω_{Π} remain as variables to diminish the sidebands. If there are few limits on ω_{Π} , it may be lowered indefinitely until the desired degree of suppression is obtained. If ω_{Π} is not arbitrary and the sidebands are still objectionable, additional filtering is indicated.

One item worthy of note is the absence of K_V in Equation 16. From Equation 15 it might be concluded that decreasing K_V would be another means for reducing spurious sidebands, but for constant values of ζ and ω_n this is not a free variable. In a given loop, varying K_V will certainly affect sideband voltage, but will also vary ζ and ω_n .

On the other hand, the choice of ω_{n} may well affect spectral purity near the carrier, although reference sideband levels may be quite acceptable.

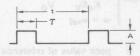
In computing sideband levels, the value of V_{ϕ} must be determined in relation to other loop components. Residual reference frequency components at the phase detector output are related to the dc error voltage necessary to supply charge pump leakage current and amplifier bias current. From these average voltage figures, spectral components of the reference frequency and its harmonics can be computed using an approximation that the phase detector output consists of square waves τ seconds

wide repeated at t second intervals (Figure 17). A Fourier analysis can be summarized for small ratios of τ/t by:

- (1) the average voltage (Vava) is A(τ/t)
- (2) the peak reference voltage value (V_φ) is twice V_{avg}, and
- (3) the second harmonic (2f_{ref}) is roughly equal in amplitude to the fundamental.

By knowing the requirements for (1) due to amplifier bias and leakage currents, values for (2) and (3) are uniquely determined.

FIGURE 17 — PHASE DETECTOR OUTPUT



An example of this sideband approximation technique can be illustrated using the parameters specified for the synthesizer design included in the applications information section.

$$\begin{array}{lll} N_{max} = 30 & \omega_{n} = 4500 \; rad/s \\ K_{V} = 11.2 \times 10^{6} \; rad/s/V & R_{1} = 2 \; k\Omega \\ K_{\phi} = 0.12 \; V/rad & f_{ref} = 100 \; kHz \end{array}$$

Substituting these numbers into Equation 16:

$$\frac{\text{sideband}}{f_{\text{out}}} = V_{\phi} \frac{(0.8)(30)(4500)}{2\pi(10^5)(0.111)}$$

$$= V_{\phi} (1.55)$$
(17)

The result illustrates how much reference feedthrough will affect sideband levels. If 1.0 mV peak of reference appears at the output of the phase detector, the nearest sideband will be down 56.2 dB.

If the amplifier section included in the MC4344/4044 is used, with $R_L=1~k\Omega$, some approximations of the value of V_{ϕ} can be made based on the input bias current and the value of R_1 . The phase detector must provide sufficient average voltage to supply the amplifier bias current, I_b , through R_1 ; when the bias current is about 5.0 μA and R_1 is 2 $k\Omega$, V_{avg} must be 10 mV. From the assumptions earlier concerning the Fourier transform, and with the help of Figure 18, we can see that the phase detector duty cycle will be about 1.7% (A = 0.6 V), giving a fundamental (reference) of 20 mV peak. If this value for V_{ϕ} is substituted into Equation 18, the resulting sideband ratio represents 30 dB suppression due to this component alone.

In addition to the amplifier bias current, another factor to consider is transistor Q5 reverse leakage current I_L flowing into pin 10 of the MC4344/4044 charge pump. I_L is generally less than 1.0 μA and is no more than 5.0 μA over the temperature range. A typical design value for 25°C is 0.1 μA. Both I_L and amplifier bias current I_B are

in a direction to deplenish the charge on filter capacitor C. A second charge pump leakage, $I_L{}^\prime$, attributed by diode CR1 flows out of pin 5. This current, however, is in a direction to help supply I_B and I_L and thus tends to minimize the discharge of C. Typically $I_L{}^\prime$ is much less than I_L and, since it is also in a direction to minimize discharge of the filter capacitor, it will be ignored in the following discussion. The total charge removed from C must be replaced by current supplied by the charge pump during the next up-date opportunity. This current flows through R1. To minimize the effects of I_B and I_L a relative small value of R1 should be chosen. A minimum value of 1 k Ω is a good choice.

FIGURE 18 — OUTPUT ERROR CHARACTERISTICS

DUTY CYCLE (%)	PHASE ERROR (Deg)	V _{avg}	V _φ (peak) (mV)
0.1	0.36	0.6	1.2
0.2	0.72	1.2	2.4
0.3	1.08	1.8	3.6
0.4	1.44	2.4	4.8
0.5	1.80	3.0	6.0
0.6	2.16	3.6	7.2
0.7	2.52	4.2	8.4
0.8	2.88	4.8	9.6
0.9	3.24	5.4	10.8
1.0	3.60	6.0	12.0
2.0	7.2	12.0	24.0
3.0	10.8	18.0	35.9
4.0	14.4	24.0	47.9
5.0	18.0	30.0	59.8
6.0	21.6	36.0	71.6
7.0	25.2	42.0	83.3
8.0	28.8	48.0	95.0
9.0	32.4	54.0	106.6
10.0	36.0	60.0	118.0

After values for C and R₂ have been computed on the basis of loop dynamic properties, the overall sideband to f_{out} ratio computation can be simplified.

Since

$$\begin{array}{l} V_{\phi} = 2 \ V_{avg} \\ V_{avg} = (I_b + I_L) \ R_1 \\ V_{\phi} = 2 \ (I_b + I_L) \ R_1 \\ \end{array} \\ = 2R_1 \ (I_b + I_L) \left(\frac{R_2}{R_1}\right) \\ \\ V_{ref} = V_{\phi} \ \left(\frac{R_2}{R_1}\right) \\ \end{array}$$

we find that

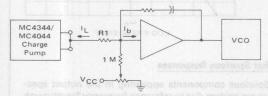
$$\frac{\text{sideband}}{f_{\text{out}}} = \frac{V_{\text{ref}}K_{\text{V}}}{2\omega_{\text{ref}}}$$
 (19)

$$\frac{\text{sideband}}{f_{\text{out}}} = \frac{2R_2(I_b + I_L)K_V}{2\omega_{\text{ref}}}$$
 (20)

Equation 20 indicates that excellent suppression could be achieved if the bias and leakage terms were nulled by current summing at the amplifier input (Figure 19). This has indeed proved to be the case. Experimental results indicate that greater than 60 dB rejection can routinely

be achieved at a constant temperature. However when nulling fairly large values (> 100 nA), the rejection becomes quite sensitive since leakages are inherently a function of temperature. This technique has proved useful in achieving improved system performance when used in conjunction with good circuit practice and reference filtering.

FIGURE 19 — COMPENSATING FOR BIAS AND LEAKAGE CURRENT



Additional Loop Filtering

So far, only the effects of fundamental loop dynamics on resultant sidebands have been considered. If further sideband suppression is required, additional loop filtering is indicated. However, care must be taken in placement of any low pass rolloff with regard to the loop natural frequency $(\omega_{n}).$ On one hand, the "corner" should be well below (lower than) ω_{ref} and yet far removed (above) from $\omega_{n}.$ Although no easy method for placing the roll-off point exists, a rule of thumb that usually works is: $\omega_{\text{C}} = 5\omega_{\text{D}} \tag{21}$

Reference frequency suppression per pole is the ratio of ω_C to $\omega_{ref}.$

$$SB_{dB} \cong n \ 20 \ log_{10} \left(\frac{\omega_{C}}{\omega_{ref}}\right)$$
 (22)

where n is the number of poles in the filter.

Equation 22 gives the <u>additional</u> loop suppression to ω_{ref} ; this number should be added to whatever suppression already exists.

For non-critical applications, simple RC networks may suffice, but if more than one section is required, loop dynamics undergo undesirable changes. Loop damping factor decreases, resulting in a high percentage of overshoot and increased ringing since passive RC sections tend to accumulate phase shift more rapidly than signal suppression and part of this excess phase subtracts from the loop phase margin. Less phase margin translates into a lower damping factor and can, in the limit, cause outright oscillation.

A suitable alternative is an active RC section, Figure 20, compatible with the existing levels and voltages. An active two pole filter (second order section) can realize a more gradual phase shift at frequencies less than the cutoff point and still get nearly equal suppression at frequencies above the cutoff point. Sections designed with a slight amount of peaking ($\zeta \cong 0.5$) show a good compromise between excess phase below cutoff (ω_{C}), without peaking enough to cause any danger of raising the loop gain for frequencies above ω_{D} . A fairly non-critical section may simply use an emitter follower as the active device

with two resistors and capacitors completing the circuit (Figure 21). This provides a -12 dB/octave (-40 dB/decade) rolloff characteristic above ω_{n} , though the attenuation may be more accurately determined by Equation 22. If the sideband problem persists, an additional section may be added in series with the first. No more than two sections are recommended since at that time either (1) the constraint between ω_{n} and ω_{ref} is too close, or (2) reference voltage is modulating the VCO from a source other than the phase detector through the loop amplifier.

FIGURE 20 — OPERATIONAL AMPLIFIER LOW PASS FILTER

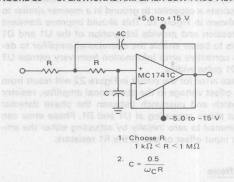
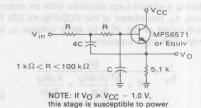


FIGURE 21 — EMITTER FOLLOWER LOW PASS FILTER



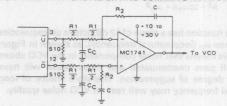
Operation without charge pump phase detector #1 of the MC4344/4044 can be implemented quite successfully in many applications without using the charge pump and internal darlington amplifier approach. An operational amplifier filter can be used to process the error information appearing at U1 and D1 (pins 13 and 2) directly (Figure 22). This phase detector/filter approach offers a potentially superior performing system because:

a. Charge pump delay time is eliminated.

supply noise.

 b. Charge pump input signed threshold level need not be overcome before error information is obtained.
 This can result in a substantial improvement in the

FIGURE 22—TYPICAL FILTER AND SUMMING NETWORK



- c. The filter amplifier ground location can be separated from the phase detector ground.
- d. An "optimum" filter amplifier input threshold of approximately two diode drops need not be established.

The filter discussions and relationships developed for integrator-log filter sections can be applied to the system of Figure 22 and the previously derived equations can be used to determine values for R1, R2 and C.

It may be desirable to split each of the R1 resistors and incorporate a capacitor to ground in a manner similar to that shown in Figure 15. This should improve transient suppression and provide integration of the U1 and D1 signals to better enable the operational amplifier to develop corrective error information from very narrow U1 and D1 pulse widths.

Phase error for the circuit in Figure 22 will result from input offset voltage in the operational amplifier, resistor mismatch and mismatch between the phase detector output states appearing at U1 and D1. Phase error can be trimmed to zero initially by adjusting either the amplifier input offset or one of the R1 resistors.

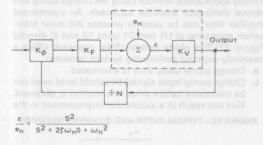
VCO Noise

Effects of noise within the VCO itself can be evaluated by considering a closed loop situation with an external noise source, e_n , introduced at the VCO (Figure 23). Resultant modulation of the VCO by error voltage, ϵ , is a second order high pass function:

$$\frac{\varepsilon}{e_{n}} = \frac{S^{2}}{S^{2} + \frac{ST_{1}K\phi K_{V}}{T_{2}N} + \frac{K\phi K_{V}}{T_{2}N}}$$

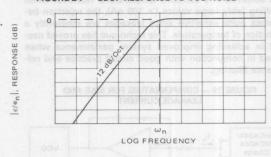
$$= \frac{S_{2}}{S^{2} + 2\zeta\omega_{n}S + \omega_{n}^{2}}$$
(23)

FIGURE 23 — EFFECTS OF VCO NOISE



This function has a slope of 12 dB/octave at frequencies less than ω_{n} (loop natural frequency), as shown in Figure 24. This means that noise components in the VCO above ω_{n} will pass unattenuated and those below will have some degree of suppression. Therefore choice of loop natural frequency may well rest on VCO noise quality.

FIGURE 24 - LOOP RESPONSE TO VCO NOISE

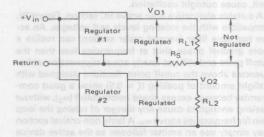


Other Spurious Responses

Spurious components appearing in the output spectrum are seldom due to reference frequency feedthrough alone. Modulation of any kind appearing on the VCO control line will cause spurious sidebands and can come in through the loop amplifier supply, bias circuitry in the control path, a translator, or even the VCO supply itself. Some VCOs have a relatively high sensitivity to power supply variation. This should be investigated and its effects considered. Problems of this nature can be minimized by operating all devices except the phase detector, charge pump, and VCO from a separate and well isolated supply. A common method uses a master supply of about 10 or 12 volts and two regulators to produce voltages for the PLL - one for all the logic (including the phase detector) and the other for all circuitry associated with the VCO control line.

Sideband and noise performance is also a function of good power supply and regulator layout. As mentioned earlier, extreme care should be exercised in isolating the control line voltage to the VCO from influences other than the phase detector. This not only means good voltage regulation but ac bypassing and adherence to good grounding techniques as well. Figure 25 shows two separate regulators and their respective loads. Resistor $R_{\rm S}$ is a small stray resistance due to a common thin ground return for both R_{L1} and R_{L2} . Any noise in R_{L2} is now reproduced (in a suppressed form) across R_{L1} . Load current from R_{L1} does not affect the voltage across R_{L2} . Even though the regulators may be quite good, they can hold $V_{\rm O}$ constant only across their outputs, not necessarily across the load (unless remote sensing is used).

FIGURE 25 — LOOP VOLTAGE REGULATION



One solution to the ground-coupled noise problem is to lay out the return path with the most sensitive regulated circuit at the farthest point from power supply entry as shown in Figure 26.

Even for regulated subcircuits, accumulated noise on the ground bus can pose major problems since although the cross currents do not produce a differential load voltage directly, they do produce essentially common mode noise on the regulators. Output differential load noise then is a function of the input regulation specification. By far the best way to sidestep the problem is to connect each subcircuit ground to the power supply entry return line as shown in Figure 27.

FIGURE 26 - REGULATOR LAYOUT

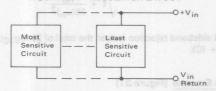
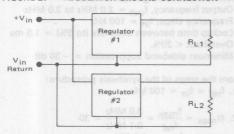


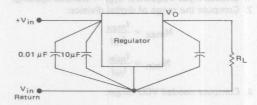
FIGURE 27 — REGULATOR GROUND CONNECTION



In Figures 25 and 27, R_{L1} and R_{L2} represent component groups in the system. The designer must insure that all ground return leads in a specific component group are returned to the common ground. Probably the most overlooked components are bypass capacitors. To minimize sidebands, extreme caution must be taken in the area immediately following the phase detector and through the VCO. A partial schematic of a typical loop amplifier and filter is shown in Figure 28 to illustrate the common grounding technique.

Bypassing in a phase-locked loop must be effective at both high frequencies and low frequencies. One capacitor in the 1.0-to-10 μF range and another between 0.01 and 0.001 μF are usually adequate. These can be effectively utilized both at the immediate circuitry (between supply and common ground) and the regulator if it is some distance away. When used at the regulator, a single electrolytic capacitor on the output and a capacitor pair at the input is most effective (Figure 29). It is important, again, to note that these bypasses go from the input/output pins to as near the regulator ground pin as possible.

FIGURE 29 — SUGGESTED BYPASSING PROCEDURE



APPLICATIONS INFORMATION

Frequency Synthesizers

The basic PLL discussed earlier is actually a special case of frequency synthesis. In that instance, $f_{Out}=f_{in},$ although normally a programmable counter in the feedback loop insures the general rule that $f_{Out}=Nf_{in}$ (Figure 30). In the synthesizer f_{in} is usually constant (crystal controlled) and f_{Out} is changed by varying the programmable divider (\div N). By stepping N in integer increments, the output frequency is changed by f_{in} per increment. In com-

FIGURE 30 — PHASE-LOCKED LOOP WITH PROGRAMMABLE COUNTER

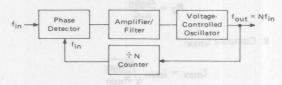
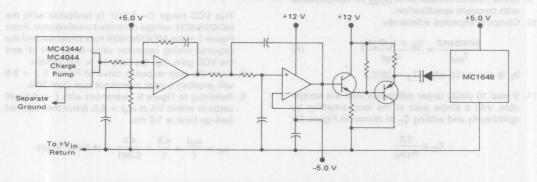


FIGURE 28 — PARTIAL SCHEMATIC OF LOOP
AMPLIFIER AND FILTER



munication use, this input frequency is called the "channel spacing" or, in general, it is the reference frequency.

There is essentially no difference in loop dynamic problems between the basic PLL and synthesizers except that synthesizer designers must contend with problems peculiar to loops where N is variable and greater than 1. Also, sidebands or spectral purity usually require special attention. These and other aspects are discussed in greater detail in AN-535. The steps for a suitable synthesis procedure may be summarized as follows:

Synthesis Procedure

- 1. Choose input frequency. (fref = channel spacing)
- 2. Compute the range of digital division:

$$N_{max} = \frac{f_{max}}{f_{ref}}$$

$$N_{min} = \frac{f_{min}}{f_{ref}}$$

3. Compute needed VCO range:

$$(2f_{max} - f_{min}) < f_{VCO} < (2f_{min} - f_{max})$$

- 4. Choose minimum ζ from transient response plot, Figure 9. A good starting point is $\zeta = 0.5$.
- 5. Choose ωn from needed response time (Figure 9):

$$\omega_n = \frac{\omega_n t}{t}$$

6. Compute C:

$$C = \frac{K_{\phi}K_{V}}{N_{max}\omega_{p}^{2}R_{1}}$$

7. Compute R2:

$$R_2 = \frac{2\zeta_{min}}{\omega_n C}$$

8. Compute ζmax:

$$\zeta_{\text{max}} = \zeta_{\text{min}} \sqrt{\frac{N_{\text{max}}}{N_{\text{min}}}}$$

- Check transient response of \(\zeta_{max}\) for compatibility with transient specification.
- 10. Compute expected sidebands:

$$\frac{\text{sideband}}{f_{out}} \cong \frac{(I_b + I_L)R_2K_V}{\omega_{ref}}$$
 (A)

(IL is about 100 nA at TJ = 25°C.)

11. If step 10 yields larger sidebands than are acceptable, add a single pole at the loop amplifier by splitting R₁ and adding C_C as shown in Figure 15:

$$C_C \cong \frac{0.8}{R_1 \omega_D}$$

Added sideband suppression (dB) is:

$$dB \approx 20 \log_{10} \frac{1}{\sqrt{1 + \frac{\omega_{ref}^2}{25(\omega_{D})^2}}}$$
 (B)

12. If step 11 still does not give the desired results, add a second order section at $\omega_{\text{C}}=5~\omega_{\text{N}}$ using either the configuration of Figure 20 or 21. The expected improvement is twice that of the single pole in step 11

dB
$$\approx 40 \log_{10} \frac{1}{\sqrt{1 + \frac{\omega_{\text{ref}}^2}{25(\omega_{\text{n}})^2}}}$$
 (C)

Total sideband rejection is then the total of 20 $log_{10}(A) + (B) + (C)$.

Design Example (Figure 31)

Assume the following requirements:

Output frequency, $f_{out} = 2.0$ MHz to 3.0 MHz

Frequency steps, $f_{in} = 100$ kHz

Lockup time between channels (to 5%) = 1.0 ms

Overshoot < 20%.

Minimum sideband suppression = -30 dB

From the steps of the synthesis procedure:

1. $f_{ref} = f_{in} = 100 \text{ kHz}$

2.
$$N_{max} = \frac{f_{max}}{f_{ref}} = \frac{3.0 \text{ MHz}}{0.1 \text{ MHz}} = 30$$

$$N_{min} = \frac{f_{min}}{f_{ref}} = \frac{2.0 \text{ MHz}}{0.1 \text{ MHz}} = 20$$

3. VCO range:

The VCO output frequency range should extend beyond the specified minimum-maximum limits to accommodate the overshoot specification. In this instance fout should be able to cover an additional 20% on either end. End limits on the VCO are:

$$f_{out}$$
max $\ge 3.0 + 0.2(1.0) = 3.2 \text{ MHz}$
 f_{out} min $\le 2.0 - 0.2(1.0) = 1.8 \text{ MHz}$

This VCO range (\approx 1.8:1) is realizable with the MC4324/4024 voltage controlled multivibrator. From Figure 7 of the MC4324/4024 data sheet we find the required tuning capacitor value to be 120 pF and the VCO gain, Ky, typically 11×10^6 rad/s/v.

- From the step response curve of Figure 9, ζ = 0.8 will produce a peak overshoot less than 20%.
- 5. Referring to Figure 9, overshoot with $\zeta=0.8$ will settle to within 5% at $\omega_{n}t=4.5$. Since the required lock-up time is 1.0 ms,

$$\omega_{n}\,=\,\frac{\omega_{n}t}{t}\,=\,\frac{4.5}{t}\,=\,\frac{4.5}{0.001}\,=\,(4.5)(10^{3}) rad/s$$

6. In order to compute C, phase detector gain and R1 must be selected. Phase detector gain, K_{ϕ} , for the MC4344/4044 is approximately 0.1 volt/radian with R₁ = 1 k Ω . Therefore,

$$C = \frac{(0.1)(11 \times 10^6)}{(30)(4.5 \times 10^3)^2(10^3)} = 1.8 \ \mu F$$

7. At this point, R2 can be computed:

$$R_2 = \frac{2\zeta_{min}}{\omega_n C} = \frac{1.6}{(4.5 \times 10^3)(1.8 \times 10^{-6})} = 200 \ \Omega$$

8.
$$\zeta_{\text{max}} = \zeta_{\text{min}} \sqrt{\frac{N_{\text{max}}}{N_{\text{min}}}} = 0.98$$

 Figure 9 shows that ζ = 0.98 will meet the settling time requirement.

 Sidebands may be computed for two cases: (1) with I_L (charge pump leakage current) nominal (100 nA), and (2) with I_L maximum (5.0 μA). A value of 5 μA will also be assumed for the amplifier bias current, ib.

$$\frac{\text{sideband}}{f_{\text{out}}} = \frac{(10 \times 10^{-6})(200)(11 \times 10^{6})}{6.28 \times 10^{5}} \approx 35 \times 10^{-3}$$

The sideband-to-center frequency ratio nominally will be:

$$\frac{\text{sideband}}{f_{\text{out}}}\bigg|_{\text{nom}} = \frac{5.1}{10} \times 35 \times 10^{-3}$$
$$= 20 \log_{10}(17.85 \times 10^{-3}) \cong -35 \text{ dB}$$

If desired additional sideband filtering can be obtained as noted in steps 11 and 12.

 By splitting R₁ and C_C, further attenuation can be gained. The magnitude of C_C is approximately:

$$C_C = \frac{0.8}{R_1 \omega_D} = \frac{0.8}{(103)(4.5)(103)} \approx 0.18 \ \mu F$$

Improvement in sidebands will be:

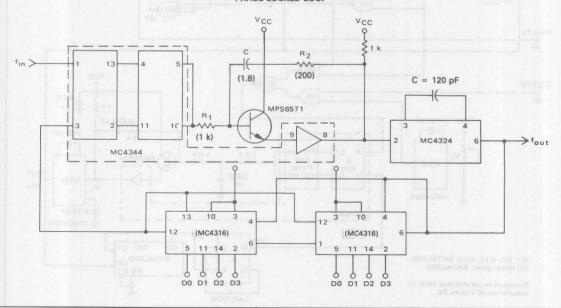
$$20 \log_{10} \frac{1}{\sqrt{1 + \frac{(2\pi \times 10^5)^2}{25(4.5 \times 10^3)^2}}} = -28 \text{ dB}$$

Nominal suppression is now -63 dB. Worst-case is 6 dB higher than nominal suppression of -57 dB. This is well within the -30 dB design requirement, step 12 is included for completeness only.

12. Attenuation of a second order filter is double that of the single order filter section described in step11. The calculations for a second order filter indicate an additional – 56 dB of sideband rejection. Figures 20 and 21 show two second order filter configurations. If R is assigned a value of 10 k Ω then C may be calculated.

$$C \, = \, \frac{0.1}{\omega_{n} R} \, = \, \frac{0.1}{(4.5 \, \times \, 10^{3})(10^{4})} \, = \, 0.0022 \, \, \mu F \label{eq:constraint}$$

FIGURE 31 — CIRCUIT DIAGRAM OF TYPE 2 PHASE-LOCKED LOOP



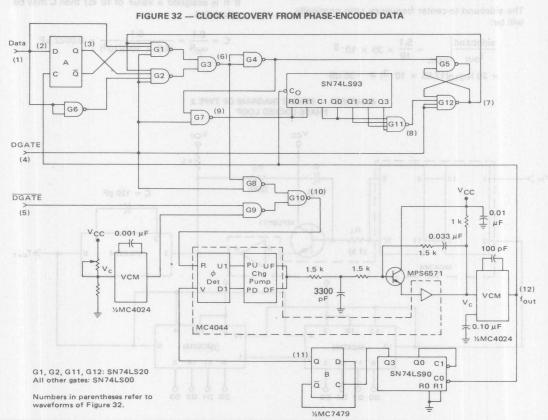
The electro-mechanical system used for recording digital data on magnetic tape often introduces random variations in tape speed and data spacing. Because of this and the encoding technique used, it is usually necessary to regenerate a synchronized clock from the data during this read cycle. One method for doing this is to phaselock a voltage controlled multivibrator to the data as it is read (Figure 32).

A typical data block using the phase encoded format is shown in row 1 of Figure 33. The standard format calls for recording a preamble of forty "0"s followed by a single "1"; this is followed by from 18 to 2048 characters of data and a postamble consisting of a "1" followed by forty "0"s. The encoding format records a "0" as a transition from low to high in the middle of a data cell. A "1" is indicated by a transition from high to low at the data cell midpoint. When required, phase transitions occur at the end of data cells. If a string of either consecutive "0"s or consecutive "1"s is recorded, the format duplicates the original clock; the clock is easily recovered by straight forward synchronization with a phase-locked loop. In the general case, where the data may appear in any order, the phase-encoded data must be processed to obtain a single pulse during each data cell before it is applied to the phase detector. For example, if the data

encoded format would result in a waveform equal to onehalf the original clock frequency. If this were applied directly to the loop, the VCM would of course move down to that frequency. The encoding format insures that there will be a transition in the middle of each data time. If only these transitions are sensed they can be used to regenerate the clock. The schematic diagram of Figure 32 indicates one method of accomplishing this.

The logic circuitry generates a pulse at the midpoint of each data cell which is then applied to the reference input of the phase detector. The loop VCM is designed to operate at some multiple of the basic clock rate. The VCM frequency selected depends on the decoding resolution desired and other system timing requirements. In this example, the VCM operates at twenty-four times the clock rate (Figure 33, Row 12).

Referring to Figure 32 and the timing diagram of Figure 33, the phase-encoded data (Figure 33, Row 1) is combined with a delayed version of itself (output of flip-flop A row 3) to provide a positive pulse out of G3 for every transition of the input signal. Portions of the data block are shown expanded in row 2 of Figure 33. Flip-flop A delays the incoming data of one-half of a VCM clock period. Gates G1, G2 and G3 implement the logic Exclusive OR of waveforms 1 and 3 except when inhibited by DGATE (row 4) or the output of G12 (row 7). DGATE and



7

its complement, DGATE, serve to initialize the circuitry and insure that the first transition of the data block (a phase transition) is ignored. The MC7493 binary counter and the G5-G12 latch generate a suitable signal for gating out G3 pulses caused by phase transitions at the end of a data cell, such as the one shown dashed in row 6.

The initial data pulse from G3 sets G12 low and is combined with DGATE in G7 to reset the counter to its zero state. Subsequent VCM clock pulses now cycle the counter and approximately one-third of the way through the next data cell the counter's full state is decoded by G11, generating a negative transition. This causes G12 to go high, removing the inhibit signal until it is again reset by the next data transition. This pulse also resets the counter, continuing the cycle and generating a positive pulse at the midpoint of each data cell as required.

Acquisition time is reduced if the loop is locked to a frequency approximately the same as the expected data rate during inter-block gaps. In Figure 32, this is achieved by operating the remaining half of the dual VCM at slightly less than the data rate and applying it to the reference input of the phase detector via the G8-G9-G10 data selector. When data appears, DGATE and DGATE cause the output of G3 to be selected as the reference input to the loop.

The loop parameters are selected as a compromise between fast acquisition and jitter-free tracking once synchronization is achieved. The resulting filter component values indicated in Figure 32 are suitable for recovering the clock from data recorded at a 120 kHz rate, such as would result in a tape system operating at 75 i.p.s. with a recording density of 1600 b.p.i. Synchronization is achieved by approximately the twenty-fourth bit time of the preamble. The relationship between system requirements and the design procedure is illustrated by the following sample calculation:

Assume a -3.0 dB loop bandwidth much less than the input data rate (~ 120 kHz), say 10 kHz. Further, assume a damping factor of $\zeta = 0.707$. From the expression for loop bandwidth as a function of damping factor and undamped natural frequency, ω_n , calculate ω_n as:

$$\omega_{-3 dB} = \omega_{n} \left(1 + 2\zeta^{2} + \sqrt{2 + 4\zeta^{2} + 4\zeta^{4}} \right)^{\frac{1}{2}}$$
 (24)

or for ω_{-3} dB = $(2\pi)10^4$ rad/s and $\zeta = 0.707$:

$$\omega_{\text{n}} = \frac{(2\pi)10^4}{2.06} = (3.05)10^4 \text{ rad/s}$$

As a rough check on acquisition time, assume that lockup should occur not later than half-way through a 40bit preample, or for twenty 8.34 µs data periods.

$$\omega_{\rm p}t = (3.05)10^4(20)(8.34)10^{-6} = 5.1$$
 (26)

From Figure 9, the output will be within 2 to 3% of its final value for $\omega_n t \approx 5$ and $\zeta = 0.707$. The filter components are calculated by:

$$\frac{K_{\phi}K_{V}}{R_{1}CN} = \omega_{n}^{2} \tag{27}$$

and

$$\frac{K_{\phi}K_{V}R_{2}}{R_{1}N} = 2\zeta\omega_{n} \tag{28}$$

 $K_{\phi} = 0.115 \text{ v/rad}$

K_V = (18.2) 10⁶ rad/s/volt N = 24 = Feedback divider ratio

 $\omega_n = (3.05) \, 10^4 \, \text{rad/s}$

$$\frac{\ddot{\zeta} = 0.707}{\frac{K_{\phi}K_{V}}{N}} = \frac{(0.115)(18.2)10^{6}}{24} = (8.72)10^{4}$$

From Equation 27:

$$R_1C = \frac{K_{\phi}K_V}{N\omega_n^2} = \frac{(8.72)10^4}{(3.05)^210^8} = (9.34)10^{-5}$$

From Equation 28:

$$\frac{R_2}{R_1} = \frac{2\zeta \omega_n N}{K_0 K_V} = \frac{2(0.707)(3.05)10^4}{(8.72)10^4} = 0.494 \approx \frac{1}{2}$$

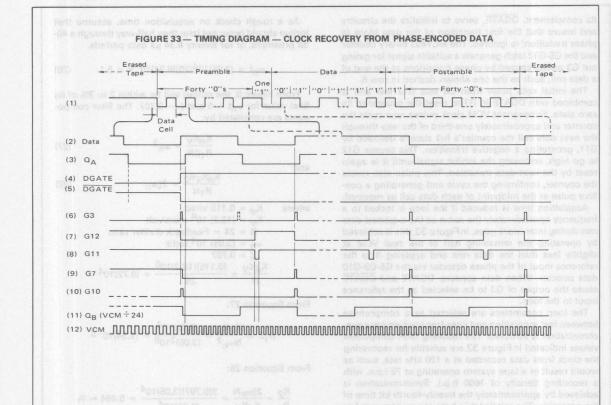
Let R₁ = 3.0 k Ω ; then R₂ = 1.5 k Ω and

$$C = \frac{(9.34)10^{-5}}{(3.0)10^3} = (3.1)10^{-8}$$

or using a close standard value, use C = 0.033 µF. Now add the additional prefiltering by splitting R1 and selecting a time constant for the additional section so that it is large with respect to R2C2.

$$10(\frac{1}{2}R_1)C_C = R_2C$$

$$C_C = \frac{2R_2C}{10R_1} = \frac{2(1.5)10^3(3.3)10^{-8}}{10(3.0)10^3} = 3300 \text{ pF}$$





MC12002/ MC12502

ANALOG MIXER

The MC12002/MC12502 is a double balanced analog mixer, including an input amplifier feeding the mixer carrier port and a temperature compensated bias regulator. The input circuits for both the amplifier and mixer are differential amplifier circuits. The on-chip regulator provides all of the required biasing.

This circuit is designed for use as a balanced mixer in high-frequency wide-band circuits. Other typical applications include suppressed carrier and amplitude modulation, synchronous AM detection, FM detection, phase detection, and frequency doubling, at frequencies up to UHF.

ANALOG MIXER



L SUFFIX CERAMIC PACKAGE CASE 632-02





LOGIC DIAGRAM Local Carrier Oscillator Amplifier Output Port 11 Inputs VR Mixer Signal Signal Port Inputs VR VB Bias Regulator

PIN ASSIGNMENT Regulator 14 VCC Bypass Local Oscillator 13 Resistor Load Input Local Oscillator 3 12 Data Output Input Alternate 11 Data Output Signal 4 Input Regulator Null Adjust 5 Bypass Mixer Signal Input Null Adjust 6 Mixer Signal VEE 7 Input

ELECTRICAL CHARACTERISTICS

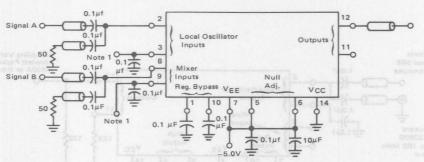
	TEST VO	LTAGE VA	LUES
	- E	Volts	
	VIHmax	VILmin	VCC
MC12502	+2.9	+2.0	+5.0
MC12002	+2.9	+2.0	+5.0

and the state of t

12 2	- 5	100	100		MC12	502 Te	nt Lim	ite	1	16	1	BAC 12	002 Te	at Line	ine	1		27			56
1	TTT	Pin	-5	5°C	_	5°C	_	5°C	1 1 8	2	o°C	1	002 Te	+85			VOL		APPLIED ED BELO		1000
Characteristic	Symbol	Under Test	Min	Max	Min	Max	Min	Max	Unit	Min	Max	Min	Max	Min	Max	Unit	VIH	T	VILmin	Vcc	Gnd
Power Supply Drain	Icc	14			- 5	16	-	-	mAdc	1	- 3	3-0	16		-	mAdc	-		_	11,12,14	5,6,7
Input Current	linH	2 3 8 9	8 - 1	-	-	0.75 0.75 0.75 0.75	-	-	mAdc mAdc mAdc mAdc	8-			0.75 0.75 0.75 0.75	-	-	mAdc mAdc mAdc	3 8	3	-	11,12,14 11,12,14 11,12,14 11,12,14	5,6,7 5,6,7
	linL	2 3 8 9	-	- - - -	-0.7 -0.7 -0.7 -0.7	- - - -		-	mAdc mAdc mAdc mAdc	-		-0.7 -0.7 -0.7 -0.7	1 1,3190	1 labat	1 1 901	mAdc mAdc mAdc mAdc	-		2 3 8 9	11,12,14 11,12,14 11,12,14 11,12,14	5,6,7 5,6,7 5,6,7
Output Current	101	11 12	-9	1 - 1	0.7	1.3	-	-	mAdc mAdc	-	_	0.7	1.3	al als	- I	mAdc mAdc			=	11,12,14 11,12,14	7 7
	102	11 12	-	-	2.1	3.9 3.9	-	_	mAdc mAdc	_	-	2.1	3.9 3.9		PH-18	mAdc mAdc	-		_	11,12,14 11,12,14	100
	lout	11 11 12 12	1 - 1		4.2 4.2 4.2 4.2	7.8 7.8 7.8 7.8			mAdc mAdc mAdc mAdc	-	-	4.2 4.2 4.2 4.2	7.8 7.8 7.8 7.8	dienienie	Personal Property	mAdc mAdc mAdc mAdc	2, 3, 2, 3,	,8	1111	11,12,14 11,12,14 11,12,14 11,12,14	5,6,7 5,6,7
Differential Current	ΔIO ₁ ΔIO ₂	11,12 11,12	-50 -100	+50 +100	-50 -100	+50 +100	-50 -100	+50 +100	μAdc μAdc	-100 -200	+100 +200	-100 -200	+100 +200	-100 -200	+100 +200	μAdc μAdc	程:		Ξ	11,12,14 11,12,14	7 5,6,7
Bias Voltage	V _{Bias}	1 4 5 6 10	2.34 390 275 275 1.300	2.54 590 415 415 1.500	2.32 400 285 285 1.185	2.52 600 425 425 1.385	2.29 420 305 305 1.050	2.49 620 445 445 1.250	Vdc mVdc mVdc mVdc Vdc	2.33 390 275 275 1.260	2.53 590 415 415 1.460	2.32 400 285 285 1.185	2.52 600 425 425 1.385	2.30 410 295 295 1.105	2.50 610 435 435 1.305	Vdc mVdc mVdc mVdc Vdc	KOJAMA	-		11,12,14 11,12,14 11,12,14 11,12,14 11,12,14	5,6,7 7 7
		100		. 1									COSTRE	ON-DATE	Parts by	Shrik Str.	Pulse In	Pulse Out	-3.0 V	Gnd	VEE
AC Gain (See Figure 1) (Frequency = 100 MHz) *Note	Av	11	5 -2		0.33	-	_	-	V/V V/V	-	-	0.28	100	A 20 0	The such	V/V V/V	8	11	3	14	7

*Note: AC Gain is a function of collector load impedance.

FIGURE 1 — A.C. GAIN TEST



Note 1:

 $V_{1L} = -3.0 \text{ V}$ on pin 3 when pin 8 is under test. $V_{1L} = -3.0 \text{ V}$ on pin 9 when pin 2 is under test.

Signal A = 30 mV p-p

Signal B = 300 mV p-p

Freq. = 100 MHz as but such HA

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable.
The unused output is connected to a 50-ohm resistor to ground.

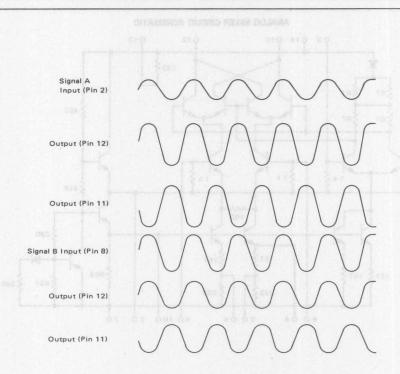
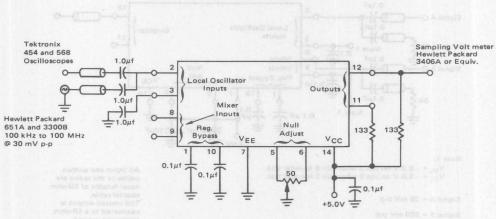
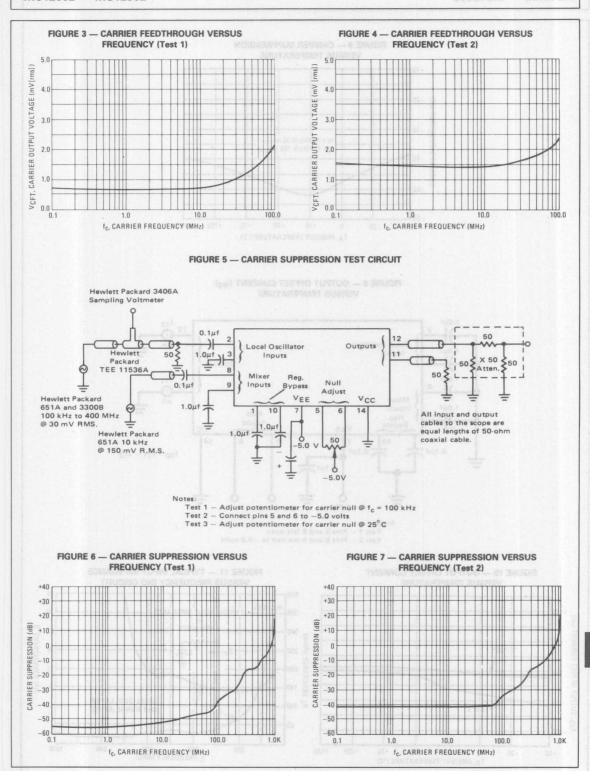


FIGURE 2 — CARRIER FEEDTHROUGH-TEST CIRCUITS



Notes: Test 1—Adjust potentiometer for carrier null at f_{C} = 100 kHz. Test 2—Connect pins 5 and 6 to Gnd.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable.



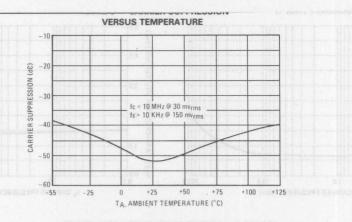
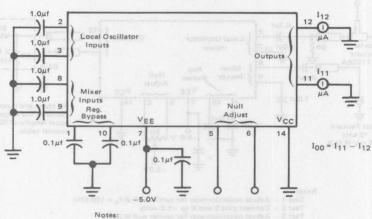
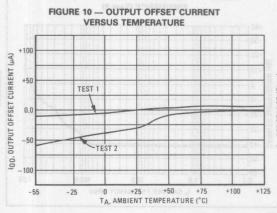
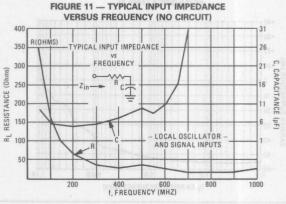


FIGURE 9 — OUTPUT OFFSET CURRENT (I₀₀) VERSUS TEMPERATURE



Test 1 — Pins 5 and 6 left open
Test 2 — Pins 5 and 6 are tied to —5.0 volts







MC12009 MC12509 MC12011 MC12511 MC12013 MC12513

Advance Information

TWO-MODULUS PRESCALER

These devices are two-modulus prescalers which will divide by 5 and 6, 8 and 9, and 10 and 11, respectively. A MECL-to-MTTL translator is provided to interface directly with the MC12014 Counter Control Logic. In addition, there is a buffered clock input and MECL bias voltage source.

- 600 MHz (Typ) Toggle Frequency
- MC12009 (÷ 5/6), MC12011 (÷ 8/9), MC12013 (÷ 10/11)
- MECL to MTTL Translator on Chip
- MECL and MTTL Enable Inputs
- +5.0 or -5.2 V Operation*
- Buffered Clock Input Series Input RC Typ, 20 Ohms and 4 pF
- V_{BB} Reference Voltage
- 310 Milliwatts (Typ)

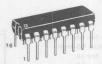
*When using a +5.0 V supply, apply +5.0 V to Pin 1 (V_{CCO}), Pin 6 (MTTL V_{CC}), Pin 16 (V_{CC}), and ground Pin 8 (V_{EE}). When using -5.2 V supply, ground Pin 1 (V_{CCO}), Pin 6 (MTTL V_{CC}), and Pin 16 (V_{CC}) and apply -5.2 V to Pin 8 (V_{EE}). If the translator is not required, Pin 6 may be left open to conserve dc power drain.

MECL PLL COMPONENTS

TWO-MODULUS PRESCALER



L SUFFIX CERAMIC PACKAGE CASE 620



PSUFFIX
PLASTIC PACKAGE
CASE 648

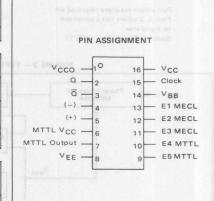
MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
(Ratings above which device life may be impa	aired)		
Power Supply Voltage (V _{CC} = 0)	ASSISTANT NO VEE NO	-8.0	Vdc
Input Voltage (V _{CC} = 0)		0 to VEE	Vdc
Output Source Current Continuous Surge	lo sru J'alr	< 50 < 100	mAdo
Storage Temperature Range	Teto	-65 to +175	°C

(Recommended Maximum Ratings above which performance may be degraded)

Operating Temperature Range	TA		oC
MC12009, MC12011, MC12013		-30 to +85	
MC12509, MC12511, MC12513		-55 to +125	
*DC Fan-Out (Gates and Flip-Flops)	n	70	_

*AC fan-out is limited by desired system performance.



This document contains information on a new product. Specifications and information herein are subject to change without notice. 7-49

7-50

ELECTRICAL CHARACTERISTICS Supply Voltage -5.2 V

These devices are designed to meet the dc specifications shown in the test table after thermal equilibrium has been established. Outputs are terminated through a 50-ohm resistor to $-2.0 \, \text{Vdc}$.

		7.00	TE	ST VOLT	AGE/	CURRI	ENT V	LUES	1114			
			1.15712		V	olts	0.19		111		mA	
@Test	4 1	4										
Temperature	VIHmax	VILmin	VIHAmin	VILAmax	VIH	VIL	VIHT	VILT	VEE	IL	IOL	ІОН
-30°C	-0.890	-1.990	-1.205	-1.500	-2.8	4.7	-3.2	-4.4	-5.2	-0.25	16	-0.40
			-1.105									
+85°C	-0.700	-1.925	-1.035	-1.440	-2.8	4.7	-3.2	-4.4	-5.2	-0.25	16	-0.40

Characteristic	Symbol	Pin Under Test	MC12009, MC12011, MC12013								TECT	VOLTACE	CUBBEN	TAR	DLIED	TORI	10 1 10	TED BE	LOW			1	
			-30°C		+25°C			+85°C				IEST	ST VOLTAGE/CURRENT APPLIED TO PINS LI						TED BELOW.				
			Min	Max	Min	Тур	Max	Min	Max	Unit	V_{IHmax}	VILmin	VIHAmin	VILAmax	V.IH	VIL	VIHT	VILT	VEE	IL	IOL	ІОН	Gnd
Power Supply Drain	1001	8	-88		-80	-		-80		mAdc							1000		8				1,10
Current	1CC2	6		5.2		-	5.2	4 1	5.2	mAdc	4	5							8	15			6
Input Current	INHI	15		375			250		250	μAdc	15	14.1	987 89				-		8				1.16
	THE P	11	100		- Sen N					Type !	11						9,10		0.9	-14-			1974
		12 13							*		12						9,10						
	INH2	4	1.7	6.0	2.0		6.0	2.0	6.4	mAdc	5	4					7	1900	8				6
	100.12	5	1.7	6.0	2.0		6.0	2.0	6.4	mAdc	5	4							8				6
	INH3	5	0.7	3.0	1.0	2914 113	3.0	1.0	3.6	mAdc	4	5	36 26		9103				8				6
	INH4	9		-	100		100		100	μAdc	34 1				9	831			8				1,1
		10		P. 1	100		100		100	μAdc				17.5	10	10			8			12.11	1,1
Leakage Current	IINL1	15	-10	Mark of	-10			-10		μAdc		-				0.70	100		8,15			100	1,1
	1 NREE	11		SAK S			120		300	De la	18	- 1							8,11				18
	16.60	12		0.5			25		43		040.0	-							8,12				
	1.66	13	V		V			V				- 1			1013				8,13				V
	INL2	9	-1.6	[A]**=	-1.6	- 10	Nex.	-1.6	0,54	mAdc	STATE OF THE PARTY	Name of Street	Ste Novemb	11 STATES	A THY	9	ATTE	W	8	p	100	Turn J	1,10
		10	-1.6	46	-1.6	VSTA C		-1.6	- C	mAde		45.00	-	over 100 to the		10	-	-	8	14			1,10
Reference Voltage	VBB	14		**	-1.360	MOSTERN	-1 160			Vdc	1000						-			14	.,		
Logic "1" Output Voltage	V _{OH1}	2	-1.100 -1.100	-0.890 -0.890	-1.000 -1.000		-0.810	-0.930 -0.930	-0.700 -0.700	Vdc Vdc	ed 200	11,12,13		19 100	23	9,10	150	15.8	8	0.30	181	11-10	1,1
		3	-2.8	-0.690	-2.6		-0.810	-2.4	-0.700	Vdc	5	4	12.400-F		31	3,10	1000	108	8	12.00	100	7	6
Logic "0" Output Voltage	VOH2	,	177.53	1.075	1.00			77.27	4.045	Vdc	3	11,12,13	P.J. 1865. 1.	15 15 16 16	0.3	9.10	COVE	15.00	8	1	180	741	-
Logic O Output Voltage	VOL1	2	-1.990 -1.990	-1.675 -1.675	-1.950 -1.950		-1.650 -1.650	-1.925 -1.925	-1.615 -1.615	Vdc	W. T.	11,12,13		Pr. Assessed	A	9,10	ASS		8	111	1167	10.5	1,1
	VOL2	7	-1.550	-4.26	-1.550	-	-4.40	-1.525	-4 48	Vdc	4	5			2-	10,10		-	8		7	-	6
Logic "1" Threshold	VOHA	2	-1.120	4.20	-1.020	114	-	-0.950	-4.40	Vdc	-		11,12,13	IL NOT LO		1000	9.10	135.5	8			-	1,1
Voltage	2	3	-1.120		-1.020			-0.950	16.1	Vdc			11,12,13				9,10	-	8		-	-	1,1
Logic "O" Threshold	VOLA	2		-1.655	-	-	-1.630	**	-1.595	Vdc	177			11,12,13		7.4		9,10	8			-	1,1
Voltage	3	3		-1.655	- A	1	-1.630		-1.595	Vdc				11,12,13	-	-	2	9,10	8	-	-		1,1
Short Circuit Current	los	7	-65	-20	-65		-20	-65	-20	mAdc	5	4		-	-	7		-	8	-	-	-	6

① Test outputs of the device must be tested by sequencing through the truth table. All input, power supply and ground voltages must be maintained between tests. The clock input is the waveform shown.

D In addition to meeting the output levels specified, the device must divide by 5, 8, or 10 during this test. The clock input is the waveform shown.

1 In addition to meeting the output levels specified, the device must divide by 6, 9, or 11 during this test. The clock input is the waveform shown.

VILmin Clock Input

ELECTRICAL CHARACTERISTICS Supply Voltage +5.0 V

These devices are designed to meet the dc specifications shown in the test table after thermal equilibrium has been established. Outputs are terminated through a 50-ohm resistor to +3.0 Vdc.

		1	Т	EST VOLT	AGE/CL	JRREN	TVAL	UES				
@ Test		Torres.		7-1-1-1	Vol	ts					mA	
Temperature	VIHmax	VILmin	VIHAmin	VILAmax	VIH	VIL	VIHT	VILT	Vcc	IL	IOL	Іон
-30°C	+4.110	+3.070	+3.795	+3.500	+2.4	+0.5	+2.0	+0.8	+5.0	-0.25	16	-0.40
+25°C	+4.190	+3.110	+3.895	+3.525	+2.4	+0.5	+2.0	+0.8	+5.0	-0.25	16	-0.40
+85°C	+4.300	+3.135	+3.965	+3.560	+2.4	+0.5	+2.0	+0.8	+5.0	-0.25	16	-0.40

case / garlier yearnin /	in Other		11108	-0 840	-1 000		-0 0/0	-0/8/90	-0.50	+85°C	+4.300	+3.135	+3.965	+3.560	+2.4	+0.5	+2.0	+0.8	+5.0	-0.25	16	-0.40	1726
	MAG I	Pin			MC12009,		, MC12013			Ales		TEC	TVOLTAG	GE/CURRE	ALT ADI	21.150	TO BIN	C		0111			DH
		Under	-3	0°C	-18	+25°C		+8	5°C	Lower		IES	IVOLIA	SE/CURRE	NI API	PLIED	IOPIN	S LIST	FDRFI	LOW:			(VEE
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	VIHmax	VILmin	VIHAmin	VILAmax	VIH	VIL	VIHT	VILT	Vcc	1L	IOL	ІОН	Gnd
Power Supply Drain	Icc1	8	-88		-80	-	-	-80		mAdc					1				1,16				8
Current	ICC2	6	19	5.2		-	5.2	100	5.2	mAdc	4	- 5			1				6				8
Input Current	JINH1	15	i direct	375			250		250	μAdc	15	The same				-			1,16				8
	FIDE T	11			11-10					11111	11			12.03		9,10			19/15				1310
		12			100						12				188	9,10							11111
	THE PER P	13			150		No.		ADD	V	13				0.0	9,10			1				1 1
	INH2	4 5	1.7	6.0	2.0		6.0	2.0	6.4	mAdc	5	4							6				8
		-	-	6.0	-		6.0	2.0	6.4	mAdc	5	4	-	-					6				1
	INH3	5	0.7	3.0	1.0		3.0	1.0	3.6	mAde	4	5	1						6				8
	INH4	9		100			100		100	μAde μAde	12				9		0.50		1,16				8
Leakage Current	Land	15	-10	100	-10		100	-10	100	µAde	18		-	-	10		-Wilb		1,16				8,15
	INLI	11	-10		1		E al.	-10		µAdc.	14						E (0)		1,10				8,11
	1000	12		236			3.60		389	1 2 100	18			-	-	-		-					8,12
	The state of	13		9.5	1		8.5	1	1	1	N. A.	1 2			1				1				8,13
	IINL2	9	-1.6	5494	~1.6	135	-	-1.6	1	mAdc	T	To Lift terms	LA DESCRIPTION	PER WAR	KH	9	JYE	AHI	1,16		nr	Series	8
Proposition 1		10	-1.6	28.7	-1.6		Lia.	-1.6		mAdc	Mr.	1 100	1751	1000	100	10	LACT .	MAN-	1,16				8
Reference Voltage	VBB	14			3.67		3.87		130	Vdc		182	LAGELY	PENGRES	W.T. A.	BELED	18 81	102 1112	1,16	14	1		8
Logic "1" Output Voltage	V _{OH1}	2	3.900	4.110	4.000		4.190	4.070	4.300	Vdc	-	11,12,13			-	9,10			1,16		-		8
	0	3	3.900	4.110	4.000		4.190	4.070	4.300	Vdc	1 79 366	11,12,13	11,024	1 440	148	9,10	23	3.4	1,16	0.58	1.12	29,78	8
	VOH2	7	2.4		2.6			2.8		Vdc	5	4	1 7 705	2 7 7 16	1133	100	3.3	0.0	6	9.08		7	8
Logic "0" Output Voltage	VOL1	2	3.070	3.385	3.110		3.410	3.135	3.445	Vdc		11,12,13		1 1100	1.28	9,10		100	1,16	EN 28		L.CE. GT	8
	1	3	3.070	3.385	3.110		3.410	3.135	3.445	Vdc	Vittora	11,12,13	VIMAM	CAVIL Manu	W.IN	9,10	-AB-EL	WH. T	1,16	1 1	3038	HON	8
	VOL2	7		0.94			0.80		0.72	Vdc	4	5							6		7		8
Logic "1" Threshold	VOHA	2	3.880		3.980			4.050		Vdc			11,12,13			Miles	9,10		1,16		ES		8
Voltage	2	3	3.880		3.980			4.050		Vdc			11,12,13		AGN	27198	9,10	ET CHE	1.16				8
Logic "0" Threshold	VOLA	2		3.405			3.430		3.465	Vdc				11,12,13				9,10	1,16				8
Voltage	3	3		3.405			3.430	-	3.465	Vdc				11,12,13				9,10	1,16				8
Short Circuit Current	105	7	-65	-20	-65		-20	-65	-20	mAdc	5	4				7			6				8

① Test outputs of the device must be tested by sequencing through the truth table. All input, power supply and ground voltages must be maintained between tests. The clock input is the waveform shown.

② In addition to meeting the output levels specified, the device must divide by 5, 8, or 10 during this test. The clock input is the waveform shown.

In addition to meeting the output levels specified, the device must divide by 6, 9, or 11 during this test. The clock input is the waveform shown.

Clock Input
VIHmos

7-53

These devices are designed to meet the dc specifications shown in the test table after thermal equilibrium has been established. Outputs are terminated through a 100-ohm resistor to -2.0 Vdc.

			TE	ST VOLT	AGE/	CURRI	ENT V	ALUES	10			
Age		1164	573		V	olts	10		E		mA	1 8
@Test		THE R	13			10	0.		100			8
Temperature	VIHmax	VILmin	VIHAmin	VILAmax	VIH	VIL	VIHT	VILT	VEE	IL :	IOL	ЮН
-55°C	-0.880	-2.020	-1.255	-1.500	-2.8	-4.7	-3.2	4.4	-5.2	-0.25	16	-0.40
+25°C	-0.780	-1.950	-1.105	-1.475	-2.8	-4.7	-3.2	-4.4	-5.2	-0.25	16	-0.40
+125°C	-0.630	-1,920	-1.000	-1.400	-2.8	-4.7	-3.2	4.4	-5.2	-0.25	16	-0.40

	0.77	Pin	MA I d	N	1C12509, N	MC12511,	MC12513				1117	TECT	VOLTAGE	CUBBEA	T AD	LIED	TORIN	10 1 10	TED OF	LOW			
har " Output Vottage V	MIN 1	Under	-55	°C	130	+25°C	830 179	+12	5°C		174.1	1531	VOLTAGE	CORREN	II API	LIED	TOPI	42 L12	EDBE	LUVV			
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit	VIHmax	VILmin	VIHAmin	VILAmax	VIH	VIL	VIHT	VILT	VEE	IL	IOL	ІОН	Gno
Power Supply Drain	Icc1	8	-88		-80	-		-80	1-	mAdc							-		8	-		1- 1	1,16
Current	ICC2	6	VII-	5.2	7		5.2		5.2	mAdc	4	5						- 1	8	-	-	1	6
Input Current	INH1	15	-	400	6 -		250		250	иAdc	15							= Dis	8	-	-	1 + 1	1.16
		11	-		4 T					111	11					9,10				+		To	61
state product	APP I	12	0 7		10 "			0 1			12					9,16			- 9			1 18	
		13						100			1			- 10		9,10						1	1
	INH2	4	1.7	6.0	2.0		6.0	2.0	6.4	mAdc mAdc	5	4	- 4 1						8	1	1	1 1	6
		-	1.7	-	-	-	-	20	6.4		5												-
	INH3	5		N - 1	1.0	0	3.0	5 7 0	Faw.	mAdc	4	.5						1 1	8			7	6
	INH4	9	-	100	0 -		100	0 7 0	100	µАdc	+		1		9				8	-		+ 1	1,16
		10		100	-		100		100	μAdc					10	-	100		8	-		1	1,16
Leakage Current	INL1	15	-10		-10			-10	1 1	μAdc		1				ar .		1	8,15	-	1	1	1,16
	- P	12							1 1							9 "			8,11			I	
tor Current	Det 9	13					10		THE THEFT								I		8.13				
Current	Livia	9	-1.6	_	-1.6	- 1 2		-1.6	5 1 13190	mAdc						9			8				1,16
	INL2	10	-1.6		-1.6			-1.6	Links	mAdc	100	1000 C 1000	1111111			10		H.	8		-		1.16
Reference Voltage	VBB	14			-1.360		-1.160	100	1100	Vdc	100	- A 171		The state of the s	4,	-10-	- 1.00		8	14	-	-	1,16
Logic "1" Output Voltage	VOH1	2	-1.120	-0.880	-0.970	100	-0.780	-0.865	-0.630	Vdc		11.12.13	TAGEROL	MERKE W	107 15	9.10	ndg r	o sign	8	-		1000	1,16
Logic i Output voitage	0	3	-1.120	-0.880	-0.970		-0.780	-0.865	-0.630	Vdc		11,12,13	-			9,10		200	8	-	-	-	1,16
	V _{OH2}	7	-2.8	-	-2.5	-		-2.2	-	Vdc	5	4	100			7	-	-	8			7	6
Logic "0" Output Voltage	VOL1	2	-2.020	-1.655	-1.950	-	-1.620	-1.920	-1.545	Vdc	30 1-7	11,12,13	135 1 13.	126 11771	-	9,10	101 1	2 1 10	8	TO A STATE OF		-	1,16
	1	3	-2.020	-1.655	-1.950	-	-1.620	-1.920	-1.545	Vdc	00 1 +30	11,12,13	44 1 13	600 1 - 2 4		9,10	011		8	MET !	120	101	1,16
	VOL2	7	_	-4.20	-	_	-4.40	-	-4.54	Vdc	4	5	1000	CHERO L A 14	-				8		7		6
Logic "1" Threshold	VOHA	2	-1.140	_	-0.990	_	_	-0.885	-	Vdc			11,12,13		101/2		9.10		8	-	1		1.16
Voltage	2	3	-1.140	_	-0.990		_	-0.885	-	Vdc	-		11,12,13	TOL TARR	CURE	SVL1 /	9,10	2 _	8	-	-	1	1,16
Logic "0" Threshold	VOLA	2	-	-1.635	-	-	-1.600		-1.525	Vdc		-	- 1	11,12,13	-	-	-	9,10	8	-	-	-	1,16
Voltage	3	3	-	-1.635	-	-	-1.600	-	-1.525	Vdc	-	-	-	11,12,13	-	-	-	9,10	8	-	-	-	1,16
Short Circuit Current	los	7	-65	-20	-65	-	-20	-65	-20	mAdc	5	4	-	-		7		-	8	-	-	-	6

Test outputs of the device must be tested by sequencing through the truth table. All input, power supply and ground voltages must be maintained between tests. The clock input is the waveform shown.

go In addition to meeting the output levels specified, the device must divide by 5, 8, or 10 during this test. The clock input is the waveform shown.

3 In addition to meeting the output levels specified, the device must divide by 6, 9, or 11 during this test. The clock input is the waveform shown.

Clock Input VIHmax VILmin

Short Circuit Current

These devices are designed to meet the dc specifications shown in the test table after thermal equilibrium has been established. Outputs are terminated through a 100-ohm resistor to +3.0 Vdc.

-65

los

-20

-65

										+25°C	+4.220	+3.110	+3.895	+3.525	+2.4	+0.5		-	+5.0	-	16	-0.40	-
				/30 1 -03	ten lara	30 1	-0	ANN	900	+125°C	+4.370	+3.140	+4.000	+3.560	+2.4	+0.5	+2.0	+0.8	+50	-0.25	16	-0.40	
	es vo	Pin		15217	1C12509, N		MC12513	AND DESCRIPTION OF THE PARTY OF	0-	630		TES	TVOLTAG	E/CURREI	NT API	PLIED	TO PIN	SLIST	ED BEI	ow:			
Characteristic	Symbol	Under	Min	5°C Max	Min	+25°C	Max	Min	25°C Max	Unit		1	lv		T.v	Ť.		\/ -	1/		1		(VE
Power Supply Drain	ICC1	8	-88	IVIAX	-80	ТУР	IVIAX	-80	IVIAX	mAdc	VIHmax	VILmin	VIHAmin	VILAmax	VIH	VIL	VIHT	VILT	V _C C	'L	IOL	ІОН	Gn 8
Current	1002	6	-00	5.2	-00	I	5.2	-80	5.2	mAdc	4	5						-	6				8
Input Current	INHI	15	5.	400			250		250	μAdc	15					-			1,16				8
		11									11				1	9,10			2				
	1 1100	12			1 -						12					9,10		7-		121			
	1.1.00	4	1.7	6.0	2.0		0.0	200	0.1	10 V	13					9,10							V
	INH2	5	17	6.0	2.0		6.0	2.0	6.4	mAdc mAdc	5	4							6				8
	INH3	5	-		1.0		3.0	2.0		mAdc	4	5							6				8
	INH4	9		100			100		100	μAdc					9				1,16				8
		10		100			100		100	μAdc			-		10			-	1,16				8
Leakage Current	INL1	15	-10	1 4	-10			-10		μAdc	0	2 - 1 1			THE	1	POR I		1,16				8,15
	Mark J	11		100								1-1-1				1 III	(B)						8,11
	11140	13		90			1 38					e j											8,12
	INL2	9	-1.6		-1.6			-1.6		mAdc	William .					9			1,16				8
	IIVLZ	10	-1.6		-1.6			-1.6	9 1	mAdc						10			1,16	-			8
Reference Voltage	VBB	14	100	100	3.67		3.87	100		Vdc	- N.	T A	75		13		T. IV	1/3	1,16	14		1 3	8
Logic "1" Output Voltage	VOH1	2	3.880	4.120	4.030	701	4.220	4.135	4 3 70	Vdc		11,12,13	TREADE	EVERTON	HEM	9.10	ED IT	BAME.	1,16	Ser	nia.		8
	1	3	3.880	4.120	4.030	GB MC IS	4 220	4 135	4 3 70	Vdc		11,12,13				9,10			1,16	-			8
	VOH2	7	2.4		2.7			3.0		Vdc	5	4	350 1 1	300 -18	00]	2813	1317	19/17	6	2 30	38	7	8
Logic "0" Output Voltage	VOL1	2	3.040	3.405	3.110		3.440	3.140	3.515	Vdc		11,12,13	ePG-1 -1-	105 1 14	18- 1	9,10		3 7	1,16	2 70		6 1 6	8
	1	3	3.040	3 405	3.110		3.440	3.140	3.515	Vdc	E,G 18	11,12,13	030-1 -1	182 7 9 1	00 1	9.10	104.8	1317	1,16	313	32	0 -0	8
11477 Th	VOL2	7	0.000	1.00	1010		0 80		0.66	Vdc	4	5	ALL VIN	Amin VILA	701	100 1	12 N	MT VI	6	1	7	77 1 18	8
Logic "1" Threshold Voltage	VOHA	2 3	3.860		4.010			4.115		Vdc Vdc			11,12,13	1		1	9,10	1	1.16	-			8
Logic "O" Threshold	VOLA	2	3.000	3.425	7.010		3.460	4.113	3.535	Vdc			11,12,13	11,12,13		75010	5,10	9,10	1,16		-	9	8
Voltage	3	3		3.425			3.460		3.535	Vdc				11.12.13	11 12	PE WILL	H IN RIGHT	9.10	1.16	-			8

-20 mAdc

Temperature VIHmax VILmin VIHAmin VILAmax

-55°C +4.120 +3.040 +3.745 +3.500

-20 ① Test outputs of the device must be tested by sequencing through the truth table. All input, power supply and ground voltages must be maintained between tests. The clock input is the waveform shown.

-65

② In addition to meeting the output levels specified, the device must divide by 5, 8, or 10 during this test. The clock input is the waveform shown.

3 In addition to meeting the output levels specified, the device must divide by 6, 9, or 11 during this test. The clock input is the waveform shown.



TEST VOLTAGE/CURRENT VALUES

VIH VIL VIHT VILT VCC

+2.4 +0.5 +2.0 +0.8 +5.0 -0.25 16 -0.40

IL IOL IOH

FIGHER 4 - CETTIS AND DELEGE THE WAVE CORKE

SWITCHING CHARACTERISTICS

Land V		Pin	1		M	C12009	9, MC1	2011,	MC120	13			TEST V	OLTAG	ES/WAY	/EFORMS	APPLIED	TO PIN	SLISTE	BELOW
mmH /		Under	1	-30°C	Oal	- 1	+25°C		Sant	+85°C		+	Pulse	Pulse	Pulse	VIHmin	VILmin	VE	VEE	Vcc
Characteristic	Symbol	Test	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit	Gen.1	Gen.2	Gen.3	†	1	-3.0 V	-3.0 V	+2.0
Propagation Delay	115+2+	2	100	-0	8.1		-	8.1	19.7	-	8.9	ns	15	1-	-	/ - N	11,12,13	9,10	8	1,6,16
(See Figures 3 and 5)	115+2-	2	1	1-	7.5	-1	1-	7.5	lewes.	-	8.2	1	15	-	land	2401	11,12,13	9,10	8	1,6,16
	15+7+	7	-	-	8.4	-	V 8	81	-	-	8.9		A	-	-		-	441 8	8	1,6,16
02:01	15-7-	7	-	-	6.5	1-		6.5	un d	-	7.1	V	A	45	-	and A	- 1	-	8	1,6,16
Setup Time	I _{setun1}	. 11	5.0	-		5.0	-	-	5.0	-	-	ns	15		100	-		9,10	8	1,6,16
(See Figures 4 and 5)	tsetup2	9	5.0	- L	-	5.0	-	-	5.0		14	ns	15	CARRY TO	B. 40	Divide	11,12,13		8	1,6,16
Release Time	trei1	11	5.0	100	***	5.0	_	-	5.0	- 1	-	ns	15		42-44	-		9,10	8	1,6,16
(See Figures 4 and 5)	t _{rel2}	9	5.0	-	-	5.0	-	-	5.0		-	ns	15	-		-	11,12,13		8	1,6,16
Toggle Frequency (See Figure 6)	fmax	2		7.1								MHz								
MC12009 : 5.6			440	-	9 = 1	480	_P	UDB	440	HI:	A	0.38	FIGU	-	-	11		-	8	16
MC12011 : 8/9			500	-	2	550			500	-	-			-		11			8	16
MC12013 10/11			500	-	- 1	550	-	-	500	-	- 27		-		-	11 -	7401	2 -	8	16

^{&#}x27;Test inputs sequentially, with Pulse Generator 2 or 3 as indicated connected to input under test, and the voltage indicated applied to the other input(s) of the same type (i.e., MECL or MTTL).

	-30°C	+25°C	+85°C	
† VIHmin	+1.03	+1.115	+1.20	Vdc
† VILmin	+0.175	+0.200	+0.235	Vdc

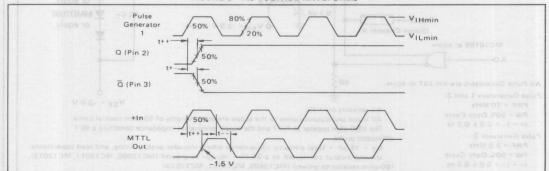
SWITCHING CHARACTERISTICS

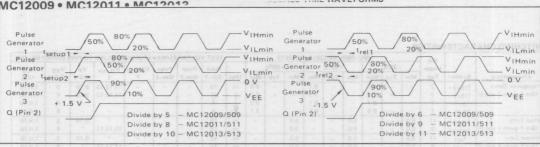
		Pin			MC12	2509, N	AC1251	11, MC	12513				TEST V	OLTAG	ES/WAY	/EFORMS	APPLIED	TO PIN	SLISTE	BELOV
		Under		-55°C	1		+25°C			125°C			Pulse	Pulse	Pulse	VIHmin	VILmin	VE	VEE	Vcc
Characteristic	Symbol	Test	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit	Gen.1	Gen.2	Gen.3	1	1	-3.0 V	-3.0 V	+2.0
Propagation Delay	115+2+	2	-		8.1	*/	-9-	8.1	-		9.4	ns	15	-	1-	+ -	11,12,13	9,10	8	1,6,16
(See Figures 3 and 5)	t15+2-	2	- 3	P	7.5	-	242	7.5	-	-53	8.7	95	15	- 20	-	1	11,12,13	9,10	8	1,6,16
	15+7+	7	-	-	8.4	-	-	8.1	-		9.4		A	-	-	13	-	-	8	1,6,16
	15-7-	7	-	-	6.5	1	-	6.5	14 3	-61	7.6	-	A	-	-	1-	-	-	8	1,6,16
Setup Time	t _{setup1}	11	5.0	-	000	5.0	-	-	5.0	-	-	ns	15			93-		9,10	8	1,6,16
(See Figures 4 and 5)	tsetup2	9	5.0	-		5.0			5.0		-	ns	15			Sub-	11,12,13	otesas	8	1,6,16
Release Time	trel1	-11 0	5.0			5.0		+	5.0	100	-	ns	15		-	-		9,10	8	1,6,16
(See Figures 4 and 5)	trel2	9	5.0	-	-	5.0	4		5.0		-	ns	15		- 04	M.Sa	11,12,13		8	1,6,16
Toggle Frequency	fmax	2	201				-04	- 12				MHz				4	85.3			
(See Figure 6)		- 1		-	5 19			111				-0.8		MY				1	-	
MC12509:5/6			420	-	-	480	-	-	420	-	-	200	-	-	-	11	241	-	8	16
MC12511:8/9			500	-	-	550		-	500	-	-		- 20	-	- :	11	-	-	8	16
MC12513:10/11		DV	500	-	-	550	-		500	-	-	-	-	-	-	11	- 7as	- 1	8	16

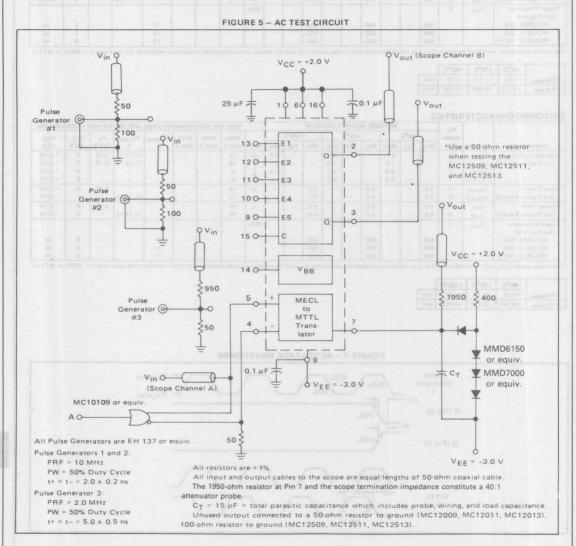
^{*}Test inputs sequentially, with Pulse Generator 2 or 3 as indicated connected to input under test, and the voltage indicated applied to the other input(s) of the same type (i.e., MECL or MTTL).

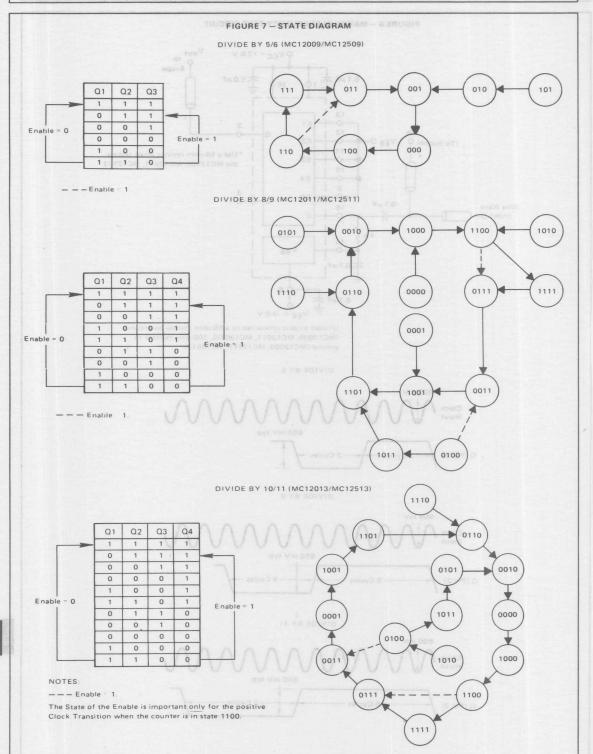
	-55°C	+25°C	+125°C	
† V _{IHmin}	+1.02	+1.15	+1.27	Vdc
† VILmin	+0.165	+0.215	+0.260	Vdc

FIGURE 3 - AC VOLTAGE WAVEFORMS









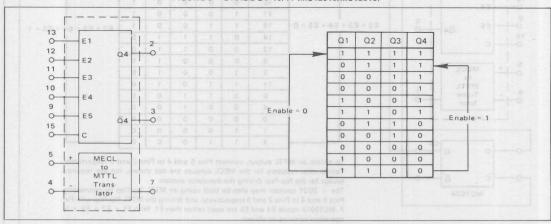
APPLICATIONS INFORMATION

The primary application of these devices is as a high-speed variable modulus prescaler in the divide by N section of a phase-locked loop synthesizer used as the local oscillator of two-way radios. The theory and advantages of variable modulus prescaling, along with typical applications, are covered in Motorola's "Electronic Tuning Address Systems" (SG72).

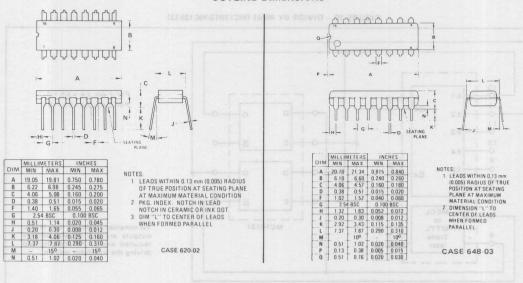
Proper VHF termination techniques should be followed when the clock is separated from the prescaler by any appreciable distance.

In their basic form, these devices will divide by 5/6, 8/9, or 10/11. Division by 5, 8, or 10 occurs when any one or all of the five gate inputs E1 through E5 are high. Division by 6, 9, or 11 occurs when all inputs E1 through E5 are low. (Unconnected MTTL inputs are normally high, unconnected MECL inputs are normally low). With the addition of extra parts, many different division configurations may be obtained (20/21, 40/41, 50/51, 100/101, etc.) A few of the many configurations are shown below, only for the MC12013/MC12513.

FIGURE 8 - DIVIDE BY 10/11 (MC12013/MC12513)



OUTLINE DIMENSIONS



and yet oblivib liliw assivab as of FIGURE 9 - DIVIDE BY 20/21 (MC12013/MC12513) (ab as of the moltastings yis ming of T

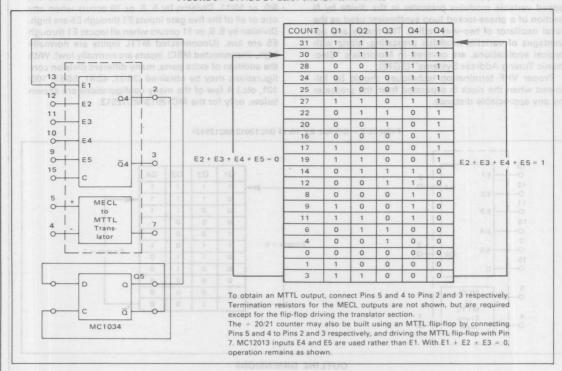
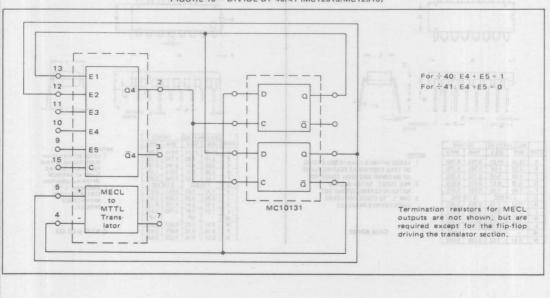


FIGURE 10 - DIVIDE BY 40/41 (MC12013/MC12513)



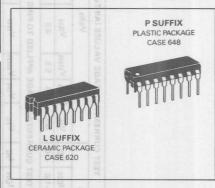


MC12014/ MC12514

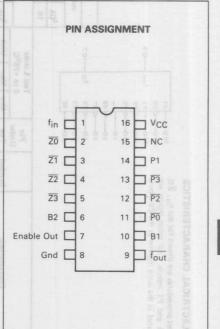
COUNTER CONTROL LOGIC

The MC12014 monolithic counter control logic unit is designed for use with the MC12013 Two-Modulus Prescaler and the MC4016 Programmable Counter to accomplish direct high-frequency programming. The MC12014 consists of a zero detector which controls the modulus of the MC12013, and an early decode function which controls the MC4016. The early decode feature also increases the useful frequency range of the MC4016 from 8.0 MHz to 25 MHz.

COUNTER CONTROL LOGIC

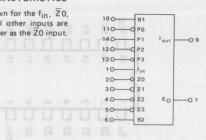


LOGIC DIAGRAM Early Decode B1 10 0 G2 P1 14 0-G4 G6 +0 9fout P0 11 0- $\overline{P}2$ G1 P3 13 0 G7 G5 G3 fin (Clock) **Enable Reset** G8 G10) G11 G9 V_{CC} = Pin 16 Gnd = Pin 8 Zero Detector G12 G13 ZO G14 ٠Z1 G15 G19 Z2 Enable Out G16 Z3 G18 G17 B2



ELECTRICAL CHARACTERISTICS

Test procedures are shown for the f_{in} , $\overline{Z}0$, B1 and P1 inputs. All other inputs are tested in the same manner as the $\overline{Z}0$ input.



NV.	TE	EST CU	RRENT	VOLT	AGE VAL	UES (AII	Tempera	tures)	
m	A	0 8	or see			Volts			3
IOL	ІОН	lic	VIL	VIH	VIHH	VRH	Vcc	VCCL	Vcch
16	-1.6	-10	0.5	2.4	5.5	4.5	5.0	4.75	5.25

						10	-1.0	-10	0.5	2.4	5.5	4.5	3.0	4.75	3.20	
603		Pin Under		Test Lir 0 to +7!			TEST	CURF	RENT/VOL	TAG	E APPL	IED TO PINS	LISTE	D BELOV	N .	
Characteristic	Symbol	Test	Min	Max	Unit	IOL	ІОН	11C	VIL	VIH	VIHH	VRH	Vcc	VCCL	VCCH	Gnd
Input Forward Current	IIL.	1 2 10 14	-	6.4 -1.6	mAdc		-	Noge Pri	1 2 10 14			1111	1 1 100	1 - 910	16	8,10 8 1,8,11,12,13 1,8,11,12,13
Leakage Current	Тин	1 2 10 14		160 40	μAdc	- 1 - 1 - 1 - 1		196 901	=	1 2 10 14	1111	1-1-1-1	dels jate		16	8,10 8 1,8,11,12,13 1,8,11,12,13
	Тинн	1 2 10 14	=	1.0	mAdc	1	-/		TĪ l		1 2 10 14	1 - 1 - 1	spinyligh settyligh		16	8 8 1,8,11,12,13 1,8,11,12,13
Clamp Voltage	VIC	1 2 10 14	7	-1.2	Vdc	E	-	1 2 10 14	1 - 1	- Mariana		ord the	D PARTON	16 	1 1 1	8
Output Output Voltage	VOL*	7 9	F	0.5	Vdc Vdc	7 9	=/	=	11,12,13 11,12,13	Sic on	-	2,3,4,5,10,11 10,14	OLUMBUT	16 16	Too	8 8
	VOH	7 9**	2.4		Vdc Vdc	17-1	7 9	-	2,3,4,5	_6	_	6 11,12,13	8 4	16 16	- 3	8 8
Short-Circuit Current	los	7 9**	-20 -20	-65 -65	Vdc Vdc	-	74	=	2,3,4,5	-	-	6 11,12,13	16 16	18-81 8-3	= "	7,8 8,9
Power Requirements Power Supply Drain	Icc	16	-	35	mAdc	-	Le	1		-	-	- 10	16	0.5	-	1,8

Waveform 1:

Waveform 2:

^{*}Output level to be measured after waveform 1 is applied to f_{in} , pin 1. **Output level to be measured after waveform 2 is applied to f_{in} , pin 1.

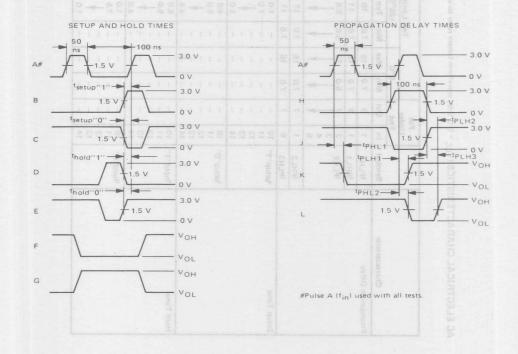
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, waveform letters refer to waveforms on next page.)

	1	Ur	in ider	100			Limits	(ns)	E E E	9	Pulse (Gen. 1	Pulse (Gen. 2	Pulse	Out	Voltage Appl Listed E	
Characteristic	Symbol	In	est Out	Min	PC Max	Min	+25°C	Max	+75 Min	Max	Wave- form	Pin	Wave- form	Pin	Wave- form	Pin	V _{II} = 0.5 V	V _{IH} = 2.4 \
Propagation Delay	tPLH1	1	9	7.0	15	7.0	10	15	7.0	17	А	1	J	10	K	9	11,12,13	14
	tPHL1	1	9	7.0	16	7.0	11	16	7.0	18	Α	1	J	10	K	9	11,12,13	14
	^t PLH2	2 3 4 5	7	5.0	12	5.0	8.5	12	5.0	14	A	1	H — ¥	2 3 4 5	L	7	3,4,5,11,12,13 2,4,5,11,12,13 2,3,5,11,12,13 2,3,4,11,12,13	6,10,14
	tPHL2	1	7	7.0	16	7.0	11	16	7.0	18	А	1	Н	2	L	7	3,4,5,11,12,13	6,10,14
	tPLH3	6	7	7.0	16	7.0	11	16	7.0	18	Α	1	J	6	L	7	2,3,4,5,11,12,13	-10,14
Setup Time	^t setup''1''	10 11 12 13 14		11111	1 1 1 1		1.0 7.0 1.0	2.0	F FORM	deska Jed	A	1	B	10 11 12 13 14	G F—▼ G	9	11,12,13 12,13 11,13 11,12 11,12,13	14 10,14 ↓ 10
	tsetup''0''	10 11 12 13	F 0 1 1 1	3.0.0 1 1 1 1 1	1 1 12 10 1	1 1 1 1	4.5 5.0 4.5	8.0 9.0 V 8.0	The Times	to de festado	A	1	C	10 11 12 13	F G -> F	9	11,12,13 12,13 11,13 11,12 11,12,13	14 10,14 10
Hold Time	^t hold"1"	10 11 12 13 14	1	1111		1.1.1.1 3FD LIMES	4.0 5.0	8.0		La La La La La La La La La La La La La L	A	1	D	10 11 12 13 14	G F G	9	11,12,13 12,13 11,13 11,13 11,12 11,12,13	14 10,14
	thold"0"	10 11 12 13 14	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	4-14-4-4	V 21 1 1 2	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1.0 7.5 V	2.0	21111	1111	Â	100000000000000000000000000000000000000	E TOTAL	10 11 12 13 14	F G F	9	11,12,13 12,13 11,13 11,12 11,12,13	14 10,14 10

Two pulse generators are required and must be slaved together to provide the waveforms shown.

 C_{T} = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.



The MC12014 Counter Control Logic incorporates two features for enhancing operation of the MC4016/4018 Programmable Counters. 1 Maximum operating frequency of the counters is limited by the time required for re-programming at the end of each count-down cycle. Operation can be extended to approximately 25 MHz by using the "early decode" feature included in the MC12014. The appropriate connections are shown in Figure 2. Only three counter stages are shown; however, up to eight stages can be satisfactorily cascaded. Note the following differences between this and the non-extended method: the counter gate inputs are not connected to the input clock; all parallel enables are connected to the Q output (fout) of a type D flip-flop formed by gates G2 through G7 in the MC12014 package; the bus terminal of the least significant stage is grounded; all other bus terminals and one internal resistor, R, are connected together and serve as a data input, B1, to the flip-flop. Four additional data inputs, P0 through P3, serve to decode the "two" state of the least significant counter stage. Circuit operation is illustrated in waveforms of Figure 2, where the timing for the end of a count-down cycle is shown in expanded form. The counter parallel inputs are assumed to have N=245 programmed. Timing is not shown for the third stage since it has already been counted down to the all zero state. As the next-to-least significant stage reaches zero, the common bus line goes high. Count down of the least significant stage continues until the "two" state is reached, causing the remaining data inputs to the flipflop to go high. The next-to-last clock pulse of the cycle then triggers the flip-flop \overline{Q} output low. This takes the parallel enables of all three counter stages low, resetting

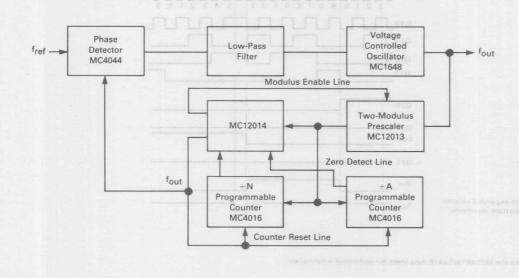
the programmed data to the outputs. The next input pulse clocks $\overline{\mathbf{Q}}$ back to the high state since the data inputs to the flip-flop are no longer all high. The resulting negative output pulse at \mathbf{f}_{Out} is one input clock period in duration. Note that division by N equal to 001 or 002 is not available using this method.

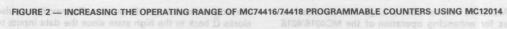
The frequency synthesizer shown in Figure 8 requires that the programmable counters be quickly stopped after reaching their terminal (zero) count. This can be simply accomplished by taking the master reset of all stages low at the appropriate time. The bus output of the counters could be used for this function since a transition there signals the end of a count-down sequence. However, due to the relatively long delay between the last positive clock transition and the bus transition a faster method is required in this application.

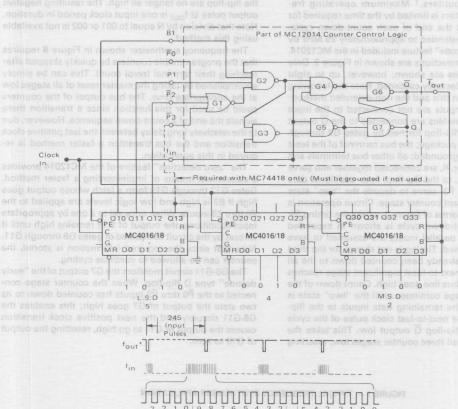
The "zero detection" feature of the MC12014 provides a convenient means of implementing a faster method. Gates G12 through G19 form a latch whose output goes high if B2 is high and low logic levels are applied to the Z0 thru Z3 inputs. When once set to a one by appropriate input conditions, the output of G19 remains high until it is reset by the circuit comprised of gates G8 through G11. Note that since the required information is stored, the counter can be allowed to continue cycling.

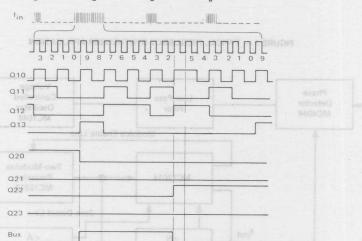
The G8-G11 circuit monitors the G7 output of the "early decode" type D flip-flop. When the counter stage connected to the P0 thru P3 inputs has counted down to its two state the output of G7 goes high; this enables the G8-G11 circuitry and the next positive clock transition causes the output of G11 to go high, resetting the output of G19 to zero.

FIGURE 1 — TYPICAL FREQUENCY SYNTHESIZER APPLICATION









*Non-expanded version of bottom waveform.

1 See the MC54416/54418 data sheet for additional information.

fout

thumbwheel switches.

Operation of the Counter Control Logic can be further clarified by considering a typical system application for programmable counters illustrated in the frequency synthesizer shown in Figure 3. There the counter provides a means of digitally selecting some integral multiple of a stable reference frequency. The circuit phase locks the output, f_{VCO}, of a voltage controlled oscillator to a reference frequency, f_{ref}.² Circuit operation is such that f_{VCO} = Nf_{ref}, where N is the divider ratio of the feedback counter, permitting frequency selection by means of

In many synthesizer applications the VCO is operated at VHF frequencies too high for direct division by TTL counters. In these cases the VCO output is usually prescaled by using a suitable fixed divide-by-M ECL circuit as

shown in Figure 4. For this configuration, $f_{VCO} = NMf_{ref}$, where N is variable (programmable) and M is fixed. Design of the optimum loop filter requires that the input reference frequency be as high as possible where the upper limit is established by the required channel spacing. Since $f_{VCO} = Nf_{ref}$ in the non-prescaled case, if N is changed by one; the VCO output changes by f_{ref} , or the synthesizer channel spacing is just equal to f_{ref} . When the prescaler is used as in Figure 4, $f_{VCO} = NMf_{ref}$, and a change of one in N results in the VCO changing by Mf_{ref} , i.e., if f_{ref} is set equal to the minimum permissible channel spacing as is desirable, then only every M channels in a given band can be selected. One solution is to set $f_{ref} = \text{channel spacing/M}$ but this leads to more stringent loop filter requirements.

FIGURE 3 — TTL PHASE-LOCKED LOOP

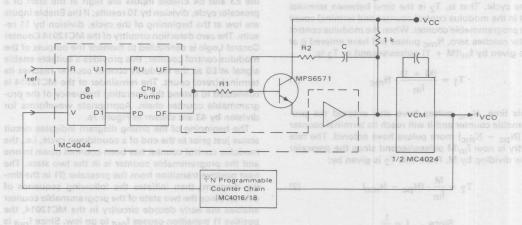
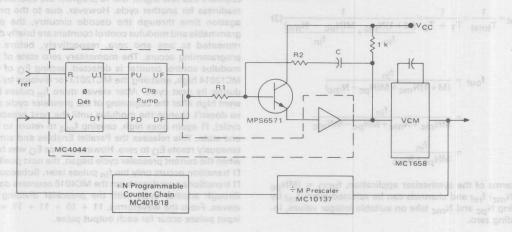


FIGURE 4 — TTL-MECL PHASE-LOCKED LOOP



2 See Motorola Application Notes AN-535, AN-532, and the MC4344/4044 Data Sheet for detailed explanation of over-all circuit operation.

7

On alternate approach that avoids this problem is provided by the counter configuration shown in Figure 5. It too uses a prescaler ahead of a programmable counter, however the modulus of the prescaler is now controlled by a third counter, causing it to alternate between M and M + 1. Operation is best explained by assuming that all three counters have been set for the beginning of a cycle: the prescaler for division by (M + 1), the modulus control counter for division by N_{mc}, and the programmable counter for division by Npc. The prescaler will divide by (M + 1) until the modulus control counter has counted down to zero; at this time, the all zero state is detected and causes the prescaler to divide by M until the programmable counter has also counted down to zero. When this occurs, a cycle is complete and each counter is reset to its original modulus in readiness for the next cycle.

To determine the relationship between f_{out} and f_{in} , let T_1 be the time required for the modulus control counter to reach its terminal count and let T_2 be the remainder of one cycle. That is, T_2 is the time between terminal count in the modulus control counter and terminal count in the programmable counter. When the modulus control counter reaches zero, N_{mc} pulses will have entered it at a rate given by $f_{in}/(M+1)$ pulses/second or T_2 is:

$$T_1 = \frac{(M+1)}{f_{in}} \cdot N_{mc} \tag{1}$$

At this time, N_{mc} pulses have also entered the programmable counter and it will reach its terminal counter after ($N_{pc}-N_{mc}$) more pulses have entered. The rate of entry is now f_{in}/M pulses/second since the prescaler is now dividing by M. From this T_2 is given by:

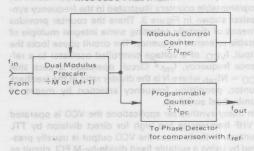
$$T_2 = \frac{M}{f_{in}} \cdot (N_{pc} - N_{mc})$$
 (2)
Since $f = \frac{1}{T}$:

$$f_{out} = \frac{1}{T_{total}} = \frac{1}{T_1 + T_2} = \frac{1}{\frac{(M+1)N_{mc}}{f_{in}} + \frac{M(N_{pc} - N_{mc})}{f_{in}}} (3)$$

$$\begin{split} f_{out} &= \frac{f_{in}}{(M+1)N_{mc} + M(N_{pc} - N_{mc})} \\ &= \frac{f_{in}}{MN_{mc} + N_{mc} + MN_{pc} - MN_{mc}} \\ &= \frac{f_{in}}{MN_{pc} + N_{mc}} \end{split}$$

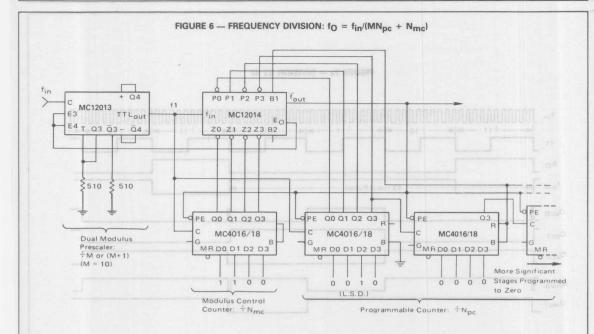
In terms of the synthesizer application, $f_{VCO} = (MN_{pc} + N_{mc})$ fref and channels can be selected every fref by letting N_{pc} and N_{mc} take on suitable integer values, including zero.

FIGURE 5 — FEEDBACK COUNTERS WITH DUAL MODULUS PRESCALER



A simplified example of this technique is shown in Figure 6. The MC12013 Dual Modulus Prescaler divides by either 10 or 11 when connected as shown in Figure 6. If the E3 and E4 Enable inputs are high at the start of a prescaler cycle, division by 10 results; if the Enable inputs are low at the beginning of the cycle, division by 11 results. The zero detection circuitry of the MC12014 Counter Control Logic is connected to monitor the outputs of the modulus control counter; this provides a suitable enable signal at E0 as the modulus control counter reaches its terminal (zero) count. The remainder of the MC12014 is connected to extend the operating frequency of the programmable counter chain. Appropriate waveforms for division by 43 are shown in Figure 7a.

The beginning of the timing diagram indicates circuit status just prior to the end of a countdown cycle, i.e., the modulus control counter has been counted down to one and the programmable counter is in the two state. The next positive transition from the prescaler (f1 in the timing diagram) then initiates the following sequence of events. Since the two state of the programmable counter enables the early decode circuitry in the MC12014, the positive f1 transition causes fout to go low. Since fout is connected to the Parallel Enables of all the MC4016 counters this low signal will re-program the counters in readiness for another cycle. However, due to the propagation time through the decode circuitry, the programmable and modulus control counters are briefly decremented to one and zero, respectively, before reprogramming occurs. The momentary zero state of the modulus control counter is detected, setting Eo of the MC12014 high, enabling the MC12013 for division by ten during its next cycle. After eleven more fin pulses (EO went high after the beginning of the prescaler cycle and so doesn't change the modulus until the next prescaler cycle), f1 again goes high, causing fout to return to the one state. This releases the Parallel Enables and simultaneously resets Eo to zero. However, since Eo was high when the current prescaler cycle began, the next positive f1 transition occurs only ten fin pulses later. Subsequent f1 transitions now decrement the MC4016 counters down through another cycle with the prescaler dividing by eleven. From the waveforms, 11 + 10 + 11 + 11 = 43input pulses occur for each output pulse.



Division by 42 is shown in Figure 7b. Operation is similar except that the modulus control counter reaches its terminal count one f1 cycle earlier than before. Since E_O is reset by the trailing edge of the f_{Out} pulse, E_O now remains high for two prescaler cycles leading to 10 + 10 + 11 + 11 = 42 input pulses for each output pulse.

Other combinations lead to similar results, however note that N_{pc} must be greater than or equal to N_{mc} for operation as described. If N_{mc} is greater than N_{pc} erroneous results are obtained, however this is not a serious restriction since N_{pc} is greater than N_{mc} in most practical applications.

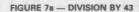
The synthesizer shown in Figure 8 generates frequencies in the range from 144 to 178 MHz with 30 kHz channel spacing. It uses the dual modulus prescaler approach discussed earlier. General synthesizer design considerations are detailed in the publications listed in footnote

2, hence only the feedback counter is discussed here. Requirements for the feedback divider are determined from:

Minimum Divider Ratio =
$$N_{Tmin} = \frac{144.00 \text{ MHz}}{30 \text{ kHz}} = 4800$$

Maximum Divider Ratio =
$$N_{Tmax} = \frac{177.99 \text{ MHz}}{30 \text{ kHz}} = 5933$$

If the prescaler divides by at least ten, the maximum input frequency to the TTL counters will be 17.799 MHz, allowing use of MC4016 Programmable Counters with the MC12014 frequency extension feature.



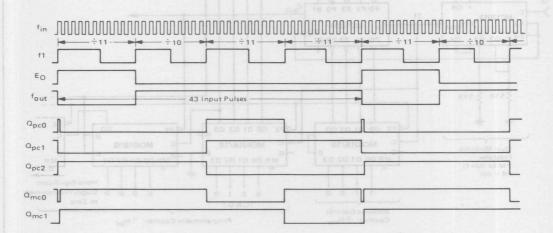
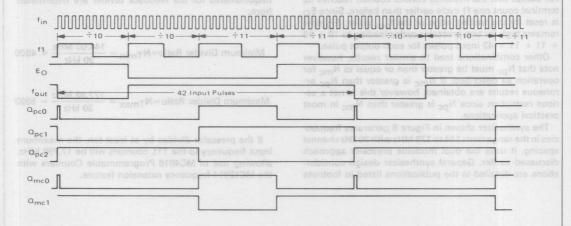


FIGURE 7b - DIVISION BY 42



	SW	SW		SV	V #	1		SI	N #	2	PROM	ō.		P	RO	M	רטכ	rPU	T		
	#1	#2			A5	A4	АЗ	A2	A1	A0	WORD	3	M.	S.B			L	S.B.		Npc	-
(144 MHz)		4	0	1	0	0	0	1	0	0	4 ()	0	1	0	0	1	0	0	0	48	48
		5	0	1	0	0	0	1	0	1	-5	0	-1	0	0	1	0	0	0	48	H
	4	6	0	1	0	0	0	1	1	0	6	0	1	0	0	1	0	0	0	48	
		7	0	1	0	0	0	1	1	1	7	0	1	0	0	1	0	0	1	49	
		8	0	1	0	0	1	0	0	0	8	0	1	0	0	1	0	0	1	49	Н
	4	9	0	1	0	0	1	0	0	1	9	0	1	0	0	1	0	0	1	49	
	5	0	0	1	0	1	0	0	0	0	16	0	1	0	1	0	0	0	0	50	
	. 5	1	0	1	0	1	0	0	0	1	17	0	1	0	1	0	0	0	0	50	
	5	2	0	1	0	1	0	0	1	0	18	0	1	0	1	0	0	0	0	50	
	5	3	0	1	0	1	0	0	1	. 1	19	0	1	0	1	0	0	0	1	51	
	5	4	0	1	0	1	0	1	0	0	20	0	1	0	1	0	0	0	1	51	
	5	5	0	1.	0	1	0	1	0	1	21	0	1	0	1	0	0	0	1	51	
	5	6	0	1	0	1	0	1	-1	0	22	0	1	0	1	0	0	1	0	52	1
	5	7	0	1	0	1	0	1	1	1	23	0	1.	0	1	0	0	1	0	52	L
	5	8	0	1	0	1	1	0	0	0	24	0	1	0	1	0	0	1	0	52	1
	5	9	0	1	0	1	1	0	0	1	25	0	1	0	1	0	0	1	1	53	7
		0	0	1	-1	0	0	0	0	0	32	0	1	0	1	0	0	1	1	53	
	6	1	0	1	1	0	0	0	0	1	33	0	1	0	1	0	0	1	1	53	
	6	2	0	1	1	0	0	0	1	0	34	0	1	0	1	0	1	0	0	54	1
		3	0	1	1	0	0	0	1	1	35	0	1	0	1	0	1	0	0	54	
	6	4	0	1	1	0	0	1	0	0	36	0	1	0	1	0	1	0	0	54	1
		5	0	1	1	0	0	1	0	1	37	0	1	0	1	0	1	0	1	55	1
		6	0	1	1	0	0	1	1	0	38	0	1	0	1	0	1	0	1	55	
2	-	7	0	1	1	0	0	1	1	1	39	0	1	0	1	0	1	0	1	55	1
		8	0	1	1	0	1	0	0	0	40	0	1	0	1	0	1	-1	0	56	1
		9	0	1	1	0	1	0	0	1	41	0	1	0	1	0	1	-1	0	56	
	- 11	0	0	1	1	1	0	0	0	0	48	0	1	0	. 1	0	1	1	0	56	1
	7		0	1	1	1 -	0	0	0	1	49	0	1	0	1	0	1	1	1	57	1
		2	0	1	1	1	0	0	1	0	50	0	1	0	1	0	1	1	1	57	1
		3	0	1	1	1	0	0	1	1	51	0	1	0	1	0	1	1	1	57	-
		4	0	1	1	1	0	1	0	0	52	0	1	0	1	1	0	0	0	58	1
	7		0	1	1	1	0	1	0	1	53	0	1	0	1	1	0	0	0	58	
The same of the same of		6	0	1	1	1	0	1	1	0	54	0	1	0	1	1	0	0	0	58	1
177 MHz)	7	7	0	1	1	1	0	1	1	1	55	0	1	0	1	1	0	0	1	59	5

The required divider range, 4800 to 5933, is obtained in the following manner: the MC12013 Dual Modulus Prescaler is connected in the divide by 10/11 mode; the modulus control counter uses two MC4016 stages with N_{mc} ranging from 00 to 99, establishing the two least significant digits of N_{T} . The remaining two digits of N_{T} are obtained from a three stage programmable counter generating N_{pc} . The least significant stage of the N_{pc} counter is fixed programmed to zero. The required programming for all remaining stages is derived from four channel selector BCD thumbwheel switches. The relationship between N_{T} and the counters is given by N_{T} = MN $_{pc}$ + N $_{mc}$; for a typical channel, say 144.33 MHz, N_{T} = 4811 requires that M = 10, N_{pc} = 480, and N_{mc} = 11, or N_{T} = (10)(480) + 11 = 4811.

A general problem associated with synthesizer design arises from the fact that there is not always a one-to-one correspondence between the code provided by the channel selector switches and the code required for proper programming of the counters. For instance, in the example above where 144.33 MHz was selected, the channel selector switches are set to 44.33 while the required divider ratio is 4811. There are numerous solutions for a given translation requirement, however the method shown here using read only memories offers a straightforward design method. While field programmable read only memories (PROMs)3 are shown, they would normally be used only during development; suitable fixed ROMs are more economical in production quantities. The design procedure for the code conversion is illustrated in Figure 9. The required programming for the two most

1	WORD	7	6	5	4	3	2	1	0
ł	0		-	-	_	-	-	-	
l	0 1	-	-	1	-		-	-	-
Ì	2	4	-	-	-	-		-	-
	3		-	-	_	-	-		-
	4	0	1	0	0	1	0	0	0
Ì	5	0	1	0	0	1	0	0	0
	6	0	1	0	0	1	0	0	0
	7	0	1	0	0	1	0	0	1
	8	0	1	0	0	1	0	0	1
	9	0	1	0	0	1	0	0	1
	10	- 3	-	-	-		_	_	
	11		-			-1		-	-
	12	_	122	1/3			-	-	
	13		192	-7	-				
	14	-	927	-	-	-		-	-
ł	15	-	100				-	_	-
ŀ	16	0	1	0	1	0	0	0	0
ŀ	17	0	1	0	1	0	0	0	0
۱	18	0	1	0	1	0	0	0	0
l	19	0	1	0	1	0	0	0	1
۱	20	0	1	0	1	0	0	0	1
ĺ	21	0	1	0	1	0	0	0	- 1
ĺ	22	0	1	0	1	-	0	1	0
ĺ		-	=1		-	0			
ĺ	23	0	1	0	1	0	0	1	0
ŀ				-		0		1	0
ĺ	25	0	1	0	1	0	0	1	1
ŀ	26	-	-	-		-		-	-
ŀ	27	-	-	-	-	-		-	-
ŀ	- 28	-	-	-//		-		-	-
ŀ	29	-	-	-	-	-	-	-	-
ŀ	30	-	-	9-1		-	-	-	-
ļ	31	-	-	-	-	-	5 -	-	100
ļ	32	0	1	0	1	0	0	1	1
ļ	33	0	1	0	1.	0	0	1	1
ļ	34	0	1	0	1	0	1	0	0
l	35	0	1	0	1	0	1	0	0
	36	0	1	0	1	0	1	0	0
į	37	0	1	0	1	0	1	0	1
ļ	38	0	1	0	-1	0	1	0	1
l	39	0	1	0	1	0	1	0	1
	40	0	1	0	12	0	1	1	0
	41	0	1	0	1	0	1	1	0
	42	- 5	- 3	-	-	-	-	-	-
	43	- 1	-	-1	-	-	-	-	-
ĺ	44	- 3	-	-	-	-	-	-	-
	45	- 9	- 1	بالنصور	-		-	-	-
	46	-	-	1-8	-		-	-	-
	47	- 1	-	-	23	-	-	-	-
ĺ	48	0	1	0	1	0	1	1	0
ľ	49	0	. 1	0	1	0	1	1	1
ĺ	50	0	1	0	1	0	1	1	1
ľ	51	0	1	0	1	0	1	1	1
ĺ	52	0	1	0	1	1	0	0	0
ĺ	53	0	11	0	1	1	0	0	0
	54	0	1	0	1	1	0	0	0
ĺ	55	0	1	0	1	1	0	0	1
ĺ	56	-	2	-	_	-	_	-	_
į	57	-	1-2	-		-	- 4	-	_
ĺ	58	_	-	-	_	-	-	_	_
ĺ	59	_	_		-	-	-		
	60						H_ (-
	61					70	7		
	62			-				_	
	63	-	_		_	_	_	_	_
	03	-	-	-	-	-	_	-	

BIT

³ See the MCM5003 data sheet and AN-550 for details of operation; briefly, one of 64 eight-bit output words is selected by a six-bit address applied to the input. The word located at each address can be field programmed by the user.

FIGURE 10 — N_{mc} PROM #1 PROGRAMMING

	SW	SW		SV	V #	3		SW	#4		PROM			P	RO	MC	וטכ	PU	Т	
	#3	#4			A5	A4	А3	A2	A1	A0	WORD		M.	S.B			L	S.B.		Nmo
(144)	0.0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	00
	0.0	3	0	0	0	0	0	0	1	1	3	0	0	0	0	0	0	0	1	01
	.0	16	0	0	0	0	0	1	1	0	6	0	0	0	0	0	0	1	0	02
		9	0	0	0	0	1	0	0	.1	9	0	0	0	0	0	0	1	1	03
	1		0	0	0	1	0	0	1	0	18	0	0	0	0	0	1	0	0	04
	1.1	5	0	0	0	1	0	1	0	1	21	0	0	0	0	0	1	0	1	05
	9.1	8	0	0	0	1	1	0	0	0	24	0	0	0	0	0	1	1	0	06
	.2	1 0	0	0	1	0	0	0	0	1	33	0	0	0	0	0	1	1	1	07
	.2	4	0	0	1	0	0	1	0	0	36	0	0	0	0	1	0	0	0	08
80 5	.2	7	0	0	1	0	0	1	1	1	39	0	0	0	0	1	0	0	1	09
	.3	0	0	0	1	1	0	0	0	0	48	0	0	0	1	0	0	0	0	10
40.1	.3	3	0	0	1	1	0	0	1	1	51	0	0	0	1	0	0	0	1	11
	.3	6	0	0	1	1	0	1	1	0	54	0	0	0	1	0	0	1	0	12
	.3	9	0	0	1	1	1	0	0	1	57	0	0	0	1	0	0	1	1	13
	.4	2	0	1	0	0	0	0	1	0	2	0	0	0	1	0	1	0	0	14
	.4	5	0	1	0	0	0	- 1	0	1	5	0	0	0	1	0	1	0	1	15
	.4		0	1	0	0	1	0	0	0	8	0	0	0	1	0	1	1	0	16
	.5	1	0	1	0	1	0	0	0	.1	17	0	0	0	1	0	1	1	1	17
	.5		0	1	0	1	0	1	0	0	20	0	0	0	1	1	0	0	0	18
	.5		0	1	0	1	0	1	1	1	23	0	0	0	-1-	1	0	0	1	19
2.1	.6	0	0	1	1	0	0	0	0	0,	32	0	0	1	0	0	0	0	0	20
-	.6	3	0	1	1	0	0	0	1	1	35	0	0	1	0	0	0	0	1	21
-	.6		0	1	1	0	0	1	.1	0	38	0	0	1	0	0	0	1	0	22
	.6	9	0	1	1	0	1	0	0	1	41	0	0	-1	0	0	0	1	1	23
- F - F - F	0.7	2	0	1	1	1	0	0	1	0	49	0	0	01	0	0	1	0	0	24
200	.7		0	1	1	1	0	1	0	1	53	0	0	1	0	0	1	0	1	25
	.7	8	0	1	1	1	1	0	0	0	56	0	0	1	0	0	1	1	0	26
	.8		1	0	0	0	0	0	0	1	1	0	0	1	0	0	1	1	1	27
	.8		1	0	0	0	0	1	0	0	4	0	0	1	0	1	0	0	0	28
	.8	7	1	0	0	0	0	1	1	1	7	0	0	1	0	1	0	0	1	29
	.9	0	1	0	0	1	0	0	0	0	16	0	0	1	1	0	0	0	0	30
	.9		1	0	0	1	0	0	1	1	19	0	0	1	1	0	0	0	1	31
100	.9		1	0	0	1	0	1	1	0	22	0	0	1	1	0	0	1	0	32
(144)	.9	9	1	0	0	1	-1	0	0	1	25	0	0	1	1	0	0	1	1	33

Use with frequency ranges:

significant digits of Npc is shown versus the code provided by switches #1 and #2 of the channel selector. If the four outputs of switch #2 and the two least significant outputs of switch #1 are regarded as address bits A0 through A5 for an MCM5003 PROM, a memory location can be associated with each switch setting. The required N_{DC} programming for each switch setting is then set into the appropriate memory location by the user. In Figure 9, the required programming has been transferred into a truth table to be used while programming the PROM. A similar result for the N_{mc} programming is shown in Figure 10. Note that the PROM shown, N_{mc} PROM #1, selects only N_{mc} numbers 00 through 33. This means that the synthesizer as shown in Figure 8 selects only the adjacent channels in a one megahertz slice of the total band. The frequency ranges that can be selected using N_{mc} PROM #1 are summarized in Figure 10. For other ranges, N_{mc} PROM #1 must be replaced by one of two additional PROMs required for generating the remaining Nmc numbers. Appropriate truth tables along with the ranges they can be used with are shown in Figures 11 and 12.

			,	-	IT			
WORD	7	6	5	4	3	2	1	(
0	0	0	0	0	0	0	0	
1	0	0	1	0	0	1	1	
2	0	0	0	1	0	1	0	(
3	0	0	0	0	0	0	0	1
4	0	0	1	0	1	0	0	(
5	0	0	0	1	0	1	0	1
				0		0	1	(
6	0	0	0	-	0	-	-	
7	0	0	1	0	1	0	0	
8	0	0	0	1	0	1	1	(
9	0	0	0	0	0	0	1	1
10	-0.	-0	-0	-7	-1	0	-	-
11	-	-	-	-	-	-	0	-
12	-	11-				-	- 1	-
13	1-	-	-	-		-	- 3	-
14	-	-	1		-	100	1- 8	-
15	-	11-		1-1		1	- 1	
16	0	0	1	1	0	0	0	0
17	0	0	0	10	0	1	1.6	1
18	0	0	0	0	0	10	0	C
19	0	0	1	1	0	0	0	1
20	0	0	0	10	1	0	0	(
21	0	0	0	0	0	10	0	1
22	0	0	1	1	-	+	1	_
			-		0	0		. (
23	0	00	0	10	1	0	0	1
24	0	0	0	0	0	10	1.5	0
25	0	0	10	1	0	0	1	1
26	1 -0.	-0	1-1	1-0		()	- 3	2 -
27	-	1-	-	-	-	-	- 0	-
28	-	-	-	-	-	-	- 5	-
29			-	-	1 -	11-	12.3	5 -
30	-	1	-	1	140	-	1008	-
31	-	14	12	-	-	-	1 40	
32	0	0	1	0	0	0	0	0
33	0	0	0	00	0	10	1 0	1
34	T.		-				1	
35	0	0	1	0	0	0	0	1
36	0	0	0	0	_	0	0	0
	U	0	0	0	1	0	-	0
37	-		-	1	-		111 39	
38	0	0	1:	0	0	0	1 1	0
39	0	0	0	0	1.	0	0	1
40	1	-	-	-		-	- 8	8
41	0	0	1	0	0	0	1 0	1
42	-0	1-0	-0	-0	-1	-0	- 1	-
43	-	-	-	-	-	-	- 9	5 -
44	-	-		-	-	-	1 - 0	b -
45	-	-		-		-	- 3	6 -
46	-	-	-	-	-	-	- 8	-
47	_	1-	1-	-	-	-	- 0	
48	0	0	0	1	0	0	0	0
49	0	0	1	0	0	1	0	0
50	3			-0	-	100	-	0
51	0	0	0	10	0	0	0	
	0	0	0	10	0	0	0	1
52	-	-	-	-	-	-	-	-
53	0	0	1	0	0	10	0	1
54	0	0	0	10	0	0	1 1	0
55	-		-	-		-	-	-
56	0	0	11	0	0	10	1	0
57	0	0	0	1.0	0	0	1	1
58	-	-	-				- 5	0 -
59	-	-	-				-	-
60	-				-	-	1-3	8 -
61	-	_	1_	_	-	-	-	0 -
62				_	-	_		9 -
63	-	_			-		- 4	
	-	-	-	-	-	_	-	

	100		18		-	-	1	1
0 1	-	6		BI		1	1 GM	JIN I
WORD	7	6	5	4	3	2	1 0	0
0	0	10	1	0	0	0	0	0
0 1 0	0	1	0	0	0	1	1	1
2 0	0	0	1	1	0	1	0	0
3	0	1	1	0	0	0	0	1
4	0	1	0	0	1	0	0	0
5	0	0	1	1	0	1	0	1
6	0	1	10	0	0	0	1	0
7	0	10	0	0	1	0	0	1
8	0	0	1	10	0	1	1	0
9	0	1	1	0	0	0	10	1
10				-	-	1-	1 _ 0	1
11		1	_	-	_		1 - 3	-
12					7		1 6	
13		1					2	
14	-	-		-	-		1 - 0	
150	- 0	To an	1		79	1.0		
	-	***	0		0	0	-	0
16	0	1	0	10	0	0	0	0
17 0	0	0	10	10	0	10	1	1
18	0	1	1	0	0	18	0	0
0 19 0	0	1	0	10	0	0	0	1
20	0	0	1	1	10	0	0	0
21	0	1	1	0	0	1	0	1
22	0	11	0	10	0	0	1	0
23	0	0	10	1	10	0	0	1
24	0	10	1	0	0	1	1	0
25	0	1	0	1	0	0	1	1
26	-7	1-0			-		- 1	-
27		-	-			1	1 - 0	-
28		1			Den.		1 - 1	-
29	-			1	1-1		- 0	1 - 1
30		1-	-	-	1-0	1	1-16	
31 0	-0	1 0	1 -0	1.7	1-0	_0	1 - 9	-
32	0	10	0	0	0	. 0	0	0
33				1			1 . 6	
34	0	19	0	1	0	10	0	0
35	0	1	00	0	0	0	0	1
36								
0 37 1	0	10	0	1	0	19	0	1
38	0	1	0	0	00	0	1	0
39	-	1	0	0	0	0	0	0
40	0	10	0	1	0	10	1 1	0
41	0	1-	0	0	0	0	1 1	
_	_		-				1 1	1
42				-01		1-1	-	-
	1			4/1-		-	1 - 8	-
44	100	1	-	1	-	-	- 0	-
45			-	-		-	- 0	-
46			1	1	1-		1	1 -
0 47 0	-0	1-0		1.0	-0	1-0	- 8	N
0 48 0		1-0	-()	To Table	1-0	= 0	- 8	
49	0	1_	0 -	1_	0	1_	1 0	1
50	0	10	0	0	00	110	0	0
51				-			- 5	-
52	0	10	00	11	10	00	0	0
53 1	0	10	0	0	0	10	0	1
54		1 -	1		-		- 8	-
55	0	1.0	0	1	10	0	0	1
56	0	10	0	0	0	1.0	1	0
57				1		1	- 0	-
58	-		1		-		- 10	8 -
59			1				1 - 10	-
60				1	-	1	-	6 -
- 61	1-0	1-		1	-	-	- 1	1 -
62	100				1-	13		-
02							1	

Use with free	quency ranges:
145.02 - 145.98	163.02 163.98
148.02 - 148.98	166.02 - 166.98
151.02 - 151.98	169.02 - 169.98
154.02 - 154.98	172.02 - 172.98
157.02 - 157.98	175.02 - 175.98
160.02 - 160.98	

63

R R M	-01	1 2008	0.4.1.6	ВІ	Thank	A	5%	5.4
WORD	7	6	5	4	3	2	1	0
0	1	0	0	0	0	0	0	0
1	0	1	1	0	0 .	1	1	1
2	1	0	0	1	0	1	0	0
3	1	0	0	0	0	0	0	- 1
4	0	1	010	0	1	0	0	0
5 0	0 1	0	0	010	0	1 0	0	1
6	1	0	0	0	0	0	1	0
7 0	0	1	1	0	1	0	0	1
8	1	0	0	1	0	1	1	0
9	1	0	0	0	0	0	1	1
10	0 + I	ca-	130	0-1	7	0.0	-	-
11	0 +	0 - 1	0-1	0-17	4	+ 0	- 5	-
12 0	7 +	2 -	1-0	1-0	-0	+ 0	- 2	h
13		8 -	0_0	9-5	10	1 4 0	- 1	-
14	_ T	-			-	"	-	-
15	-	- 1	7-7		-	7.0	-	-
16	0	1	010	010	0	0	0	0
17	1	0	0	1 1	0	1	1	1
18	0 1	0	0	100	0	0	0	0
19	0	0	0	910	0	0	0	0
21	1	0	0	0	0	1	0	1
21	0	1	1	1	0	0	1	0
23	1	0	0	1	1	0	0	1
24	1	0	0	0	0	1	1	0
25	0	1	010	0.10	0	0	1 0	1
26		87 _	7-5	0.0		0.1	- 8	0 _
27	8	15	9_1	1.7		0.0	_ 8	-
28		-	1 0	9 1		9.1		-
29	_	-	-	-	-		-	
30	-	-	-	-	-	-	-	-
31	-	-enti	101-6	sugar!	ets La s	eur :	-	_
32	1-1	-	1000	-	-	-		-
33	1	0	0	0	0	1 .	1 1	1
34	0	0.01	- 01 0	1 1 0	0	- 01,1	0	0
35	- 4	0.621	- 190 . 8	H _ :8	0.027	100 0	-	-
36	+ 3	S 1 1 1	00.1	- "	5.65	77.7		-
37	0	1	1	1 1	0	1 0	0	1
38	1	0	0	0	1	0	0	0
39	1.	0	0	0	1/4	0	0	1
40	0	1	1	1	0	1	. 1	0
41	-	-		-	-	e to a	111577	2000
42	SBE C	WENT	G DU	Marie II	IDDW	t An		-
43	ALTO.	05-U	DUTE!	10T 5	1071	r 11-4	INTO.	U 78
44	nom.	6.14	UP	100	W.J.	7.66	101 0	2.4
46	-JUST	735gs 1	ofive	e due	D Die	VV 128	IN DRO	4.5
47	Pi-Sv	19550	desir	ve-ris	00-10	I PO	men	100
48	1	0	0	1	0	0	0	0
49	0		1	1	0	1	1	1
50	DU.	1390	9921	SATIST.	THE	1014	OWN	UET
51	1	0	0	1	0	0	0	1
52	0	1	noto	1	-1-11	0	0	0
53	7	-		201		-	-	-
54	1	0	0	1	0	0	1	0
55	0	1010	1111	118	1	0	0	1
56	988	97510	13-11	nitro	12-81	7654	ertin	73-3
57	1	0	0	0	0	0	1	1
58	-	-	1	71	- 1	127	-	- 2
	18_81	1 ITO	TEN	998	TEI A	DE LINE	DATIL	SIL
59				inam	and the last of	FINE.	* 45	17)43
60	181	D14 P	i less	O DESTRU	1112345		37. 13	100
	desta	DIT /	n Ed	4pTun	175k	1.0510	g -	LAT.

146.01 - 146.97 149.01 - 149.97 152.01 - 152.97 155.01 - 155.97 158.01 - 158.97 161.01 - 161.97 164.01 - 164.97 167.01 - 167.97 170.01 - 170.97 173.01 - 173.97 176.01 - 176.97

MC12015 MC12016 MC12017



Advance Information

LOW-POWER TWO-MODULUS PRESCALER

The MC12015, MC12016 and MC12017 are two-modulus prescalers which will divide by 32 and 33, 40 and 41, and 64 and 65 respectively. An internal regulator is provided to allow these devices to be used over a wide range of power-supply voltages. Regulated operation is obtained by connecting supply voltages of 4.5 to 5.5 V to both Pin 7 and Pin 8. Unregulated operation is obtained by connecting voltages greater than 5.5 to Pin 8 and leaving Pin 7 open.

- 225 MHz Toggle Frequency
- Low-Power—7.5 mA Max at 6.8 V
- Control Input and Output are Compatible with Standard CMOS
- Connecting Pins 2 and 3 Allows Driving One TTL Load
- Supply Voltage 4.5 V to 9.5 V

MECL PLL COMPONENTS

LOW-POWER TWO-MODULUS PRESCALER



P SUFFIX PLASTIC PACKAGE CASE 626

MAXIMUM RATINGS

Characteristic	Symbol	Range	Unit
Regulated Voltage, Pin 7	V _{reg}	8.0	Vdc
Power Supply Voltage, Pin 8	Vcc	10.0	Vdc
Operating Temperature Range	TA	-40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +175	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.5 to 9.5, V_{reg} = 4.5 to 5.5 V T_A = -40°C to +85°C)

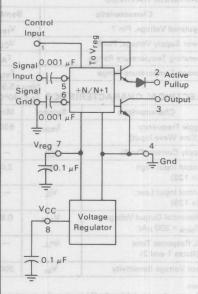
Characteristic	Symbol	Min	Тур	Max	Unit
Toggle Frequency	fmax	225	-	V820184	MHz
(Sine wave input)	fmin	_	_	35	MHz
Supply Current	Icc	_	6.0	7.8	mA
Control Input High (÷32, 40 or 64)	Vreg 7	2.0	MHIZ	-	V
Control Input Low (÷33, 41 or 65)	1.05	-	-Am	0.8	OV
Output Voltage High* (I _{source} = 50 μA)	VOH	2.5		80	V
Output Voltage Low* (Isink = 2 mA)	Voi	-	- v	0.5	V
Input Voltage Sensitivity 35 MHz 50-225 MHz	Vin	400 200	Tah	800 800	mVPF
PLL Response Time (Notes 1 and 2)	tPLL OF THE PARTY	!	igo Vm	t _{out} -70	ns

Notes

- tp_L = the period of time the PLL has from the prescaler rising output transition (50%) to the modulus control input edge transition (50%) to ensure proper modulus selection.
- 2. tout = period of output waveform.

*Pin 2 connected to Pin 3

PRESCALER BLOCK DIAGRAM



- Vreg @ pin 7 is not guaranteed to be between
 4.5 and 5.5 V when Vcc is being applied to pin 8.
 Pin 7 is not to be used as a source of regulated.
- Pin 7 is not to be used as a source of regulated output voltage.

7

Product Preview

÷128/129 520 MHz LOW-POWER TWO-MODULUS PRESCALER

The MC12018 is a two-modulus prescaler which divides by 128 and 129. An internal regulator is provided to allow this device to be used over a wide range of power-supply voltages. Regulated operation is obtained by connecting supply voltages of 4.5 to 5.5 V to both Pin 7 and Pin 8. Unregulated operation is obtained by connecting voltages greater than 5.5 to Pin 8 and leaving Pin 7 open.

- 520 MHz Toggle Frequency
- Low-Power—8.0 mA Typical

MC12017

- Control Input Is Compatible with Standard CMOS and TTL
- Supply Voltage 4.5 V to 9.5 V
- The Specifications of This Product Preview Are Design Goals Only

MAXIMUM RATINGS

Characteristic	Symbol	Range	Unit
Regulated Voltage, Pin 7	V _{reg}	8.0	Vdc
Power Supply Voltage, Pin 8	Vcc	10.0	Vdc
Operating Temperature Range	TA	-40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +175	°C

(V_{CC} = 5.5 to 9.5, V_{reg} = 4.5 to 5.5 V ELECTRICAL CHARACTERISTICS TA = -40°C to +85°C)

Characteristic	Symbol	Min	Тур	Max	Unit
Toggle Frequency (Sine Wave Input)	fmax	520	-	-	MHz
Supply Current (Pin 8)	lcc	-	8.0	10.2	mA
Control Input High (÷ 128)	VIH	2.0		-	٧
Control Input Low (÷ 129)	VIL	-		0.8	V
Differential Output Voltage (I _{sink} = 200 μA)	Vout	0.8	1.0	-	V
PLL Response Time (Notes 1 and 2)	tPLL	-	99Vm	tout 50	ns
Input Voltage Sensitivity	Vin	200	8/1	800	mVpp

- 1. tpLL = the period of time the PLL has from the prescaler rising output transition (50%) to the modulus control input edge transition (50%) to ensure proper modulus selection.
- 2. tout = period of output waveform

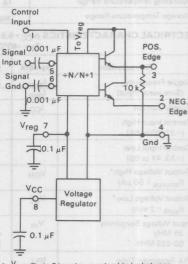
MECL PLL COMPONENTS

÷128/129 LOW-POWER TWO-MODULUS PRESCALER



P SUFFIX PLASTIC PACKAGE **CASE 626**

PRESCALER BLOCK DIAGRAM



V_{reg} @ pin 7 is not guaranteed to be between 4.5 and 5.5 V when Vcc is being applied to pin 8. 2. Pin 7 is not to be used as a source of regulated output voltage.

This document contains information on a new product. Specifications and information herein are subject to change without notice. 7-76



MC12019



Advance Information

LOW-POWER TWO-MODULUS PRESCALER

The MC12019 is a divide by 20 and 21 two-modulus prescaler. It will divide by 20 when the modulus control input is high and by 21 when the modulus control input is low.

- 225 MHz Toggle Frequency
- Low-Power—7.5 mA Max at 5.5 V
- Control Input Compatible with Standard Motorola CMOS Synthesizers
- Emitter Follower Outputs

MECL PLL COMPONENTS

LOW-POWER TWO-MODULUS PRESCALER ÷20/21



P SUFFIX PLASTIC PACKAGE CASE 626

MAXIMUM RATINGS

Characteristic	Symbol	Range	Unit	
Power Supply Voltage, Pin 7	Vcc	8.0	Vdc	
Operating Temperature Range	TA	-40 to +85	°C	
Storage Temperature Range	T _{stg}	-65 to +175	0.8 °C	

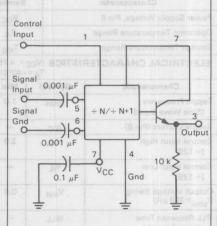
ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V, T_A = -40° to +85° C)

Characteristic	Symbol	100-4	0°C	2	5°C	8	5°C	Unit
	0,	Min	Max	Min	Max	Min	Max	100
Toggle Frequency (Sine wave input)	f _{max} f _{min}	225	35	225	35	225	35	MH2 MH2
Supply Current	Icc	100.0	7.5	-	7.5	_	7.5	mA
Control Input High (÷20)		2.0	-	2.0	Act	2.0	4 -	V
Control Input Low (÷20)	914	1.05	0.8		0.8	-	0.8	V
Output Voltage Swing	V _{out}	Phon	600		600	- 51	600	mVp
Input Voltage Sensitivity 35 MHz 50-225 MHz	V _{in}	400 200	800	400 200	800 800	400 200	800 800	
PLL Response Time (Notes 1 and 2)	tPLL	-	t _{out} -70	E	t _{out} -70	- 10	t _{out} -70	ns

Notes

- tp_{LL} = the time the PLL has from the prescaler rising output transition (50%) to the modulus control input edge transition (50%) to ensure proper modulus selection.
- 2. tout = period of output waveform.

PRESCALER BLOCK DIAGRAM



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MC12022



Product Preview

÷128/129 1.0 GHz LOW-POWER TWO-MODULUS PRESCALER

The MC12022 is a two-modulus prescaler which divides by 128 and 129. An internal regulator is provided to allow this device to be used over a wide range of power-supply voltages. Regulated operation is obtained by connecting supply voltages of 4.5 to 5.5 V to both Pin 7 and Pin 8. Unregulated operation is obtained by connecting voltages greater than 5.5 to Pin 8 and leaving Pin 7 open.

- 1.0 GHz Toggle Frequency
- Low-Power 14 mA Typical
- Control Input Is Compatible with Standard CMOS and TTI.
- Supply Voltage 4.75 V to 5.25 V
- Propagation Delay 25 ns Typical
- The Specifications of This Product Preview Are Design Goals Only

MAXIMUM RATINGS

Characteristic	Symbol	Range	Unit
Power Supply Voltage, Pin 8	Vcc	8.0	Vdc
Operating Temperature Range	TA	-40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +175	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.75 to 5.25 V T_{Δ} = -40°C to +85°C)

	'A				
Characteristic	Symbol	Min	Тур	Max	Unit
Toggle Frequency (Sine Wave Input)	f _{max}	1.0	Sm 2.1		GHz
Supply Current (Pin 8)	lcc	1594	14	20.0	mA
Control Input High (÷ 128)	VIH	2.0	V 8.0		V
Control Input Low (÷ 129)	VIL	1-1	Na 00	0.8	V
Output Voltage Swing (I _{sink} = 200 μA)	Vout	0.8	1.0	460	V _{p-p}
PLL Response Time (Notes 1 and 2)	tPLL		770 ma	t _{out} -35	ns
Input Voltage Sensitivity	Vin	200		800	mVpp

Notes

- tpLL = the period of time the PLL has from the prescaler rising output transition (50%) to the modulus control input edge transition (50%) to ensure proper modulus selection.
- 2. tout = period of output waveform.

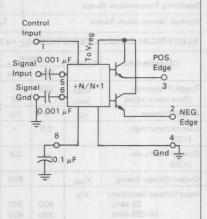
MECL PLL COMPONENTS

÷128/129 LOW-POWER TWO-MODULUS PRESCALER



P SUFFIX PLASTIC PACKAGE CASE 626

PRESCALER BLOCK DIAGRAM





Advance Information

÷ 64, 225 MHz, LOW-POWER PRESCALER

The MC12023 is a new member of Motorola's PLL family. The MC12023 is a prescaler which will divide by 64. This device may be operated over a wide range of supply voltages (3.2 to 5.5 V). Because of this range of supply voltages the MC12023 is very suitable for hand-held, battery-operated devices.

- 225 MHz Toggle Frequency
- Low Power—4.8 mA Maximum at 5.5 V
- Operating Supply Voltage 3.2 V to 5.5 V
- Connecting Pins 2 and 3 Allows Driving One TTL Load

MAXIMUM RATINGS

Characteristic (Sept. 1995)	Symbol	Range	Unit	
Power Supply Voltage	Vcc	0 to + 8.0	Vdc	
Operating Temperature Range	TA	0 to +70	°C	
Storage Temperature Range	T _{stg}	-65 to +175	°C	

ELECTRICAL CHARACTERISTICS (V_{CC} = 3.2 to 5.5 V, T_A = 0°C to +70°C)

Characteristic	Symbol	Min	Тур	Max	Unit
Toggle Frequency	fmax	225	_	_	MHz
(Sine wave input)	fmin	-	_	35	MHz
Supply Current @ 5.5 V	lcc	_	3.5**	4.8	mA
Output Voltage High* (I _{source} = 50 μA, V _{CC} = 3.2 V)	VOH	1.2	1.4	XXX	× V
Output Voltage High* (I _{source} = 50 μA, V _{CC} = 5.0 V)	VOH	2.5	-	XXX	×V
Output Voltage Low* (I _{sink} = 2.0 mA)	VOL	-	-	0.5	V
Input Voltage Sensitivity 35 MHz	Vin	400	_	800	mVpp
50–225 MHz		200	-	800	0 1
AC Input Resistance	Rin	_	TBA		kΩ
Input Capacitance	Cin		TBA	0-H 1	pF

^{*}Pin 2 connected to Pin 3

**VCC = 4.5 V

TBA — To Be Announced.

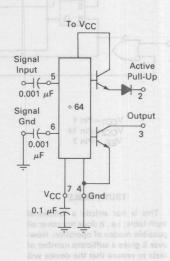
LOW-POWER PRESCALER ÷ 64

MECL PLL COMPONENTS



P SUFFIX
PLASTIC PACKAGE
CASE 626

PRESCALER BLOCK DIAGRAM



7

PHASE-FREQUENCY DETECTOR

The MC12040 is a phase-frequency detector intended for use in systems requiring zero phase and frequency difference at lock. In combination with a voltage controlled oscillator (such as the MC1648), it is useful in a broad range of phase-locked loop applications. Operation of this device is identical to that of Phase Detector #1 of the MC4044. A discussion of the theory of operation and applications information is given on the MC4344/4044 data sheet.

Operating Frequency = 80 MHz typical

PHASE-FREQUENCY DETECTOR

Advance Inform

+ 64, 225 MHz, LOW-POWIE

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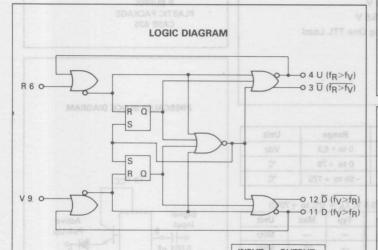
P SUFFIX

QUE TO SIGNED SOME PLASTIC PACKAGE

CASE 646



L SUFFIX CERAMIC PACKAGE CASE 632-02



V _{CC1} = Pin	1
VCC2 = Pin	14
VEE = Pin	7

TRUTH TABLE

This is not strictly a functional truth table; i.e., it does not cover all possible modes of operation. However it gives a sufficient number of tests to ensure that the device will function properly in all modes of operation.

1	Τ	PU	INPUT				
1	D	Ū	D	U	RV		
1	X	X	X	X	0	0	
l	X	X	X	X	1	0	
١	X	X	X	X	1	1	
	X	X	X	X	1	0	
l	1	0	0	1	1/	1	
ı	1	0	0	1	1	0	
ľ	1	0	0	1	1	1	
	1	0	0	1	0	1	
	1	1	0	0	1	1	
	1	1	0	0	0	1	
ŀ	0	1	1	0	1	. 1	
	0	1	1	0	0	1	
	0	1	1	0	1	1	
	0	1	1	0	1	0	
	1	1	0	0	1	1	

X = Don't Care

PIN ASSIGNMENT

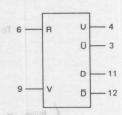


NC — No Connection

IMC12040

ELECTRICAL CHARACTERISTICS

The MC12040 has been designed to meet the dc specifications shown in the test table after thermal equilibrium has been established. Outputs are terminated through a 50 ohm resistor to +3.0 V for +5.0 V tests and through a 50 ohm resistor to -2.0 V for -5.2 V tests.



TEST VOLTAGE VALUES												
(Volts)												
VIH max	VIL min	VIHA min	VILA max	VEE								
-0.840	-1.870	-1.145	-1.490	-5.2								
-0.810	-1.850	-1.105	-1.475	-5.2								
-0.720	-1.830	-1.045	-1.450	-5.2								
	-0.840 -0.810	V _{IH max} V _{IL min} -0.840 -1.870 -0.810 -1.850	VIH max VIL min VIHA min -0.840 -1.870 -1.145 -0.810 -1.850 -1.105	VIH max VIL min VIHA min VILA max -0.840 -1.870 -1.145 -1.490 -0.810 -1.850 -1.105 -1.475								

Supply Voltage = -5.2V

apply voltage oil									,, ,	0.720		11010			
	V 0.8-	Pin		-4		MC12040	_			TEST VO	L TAGE APP	LIED TO PIN	IS LISTED BE	LOW:	
	4 0.0	Under	0'	C.	25	°C	+7!	5°C		120, 10					(Vcc)
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Unit	V _{IH} max	VIL min	VIHA min	VILA max	VEE	Gnd
Power Supply Drain Current	1E	7		-	-120	-60	-	-	mAdc	-	-	-	-	7	1,14
Input Current	INH	6 9	-	-	-	350 350	-	-	μAdc μAdc	6 9	-	-	-	7 7	1,14
Logic "1" Output Voltage	VOH 1	3 4 11 12	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	Vdc			1 1 1 1	1111	7	1.14
Logic "0" Output Voltage	v _{OL} ①	3 4 11 12	-1.870	-1.635	-1.850	-1.620	-1.830	-1.595	Vdc	- ens	egoes en	t of-seld o legan	so lugtua O Qd ta	bolt h	1,14
Logic "1" Threshold Voltage	VOHA 2	3 4 11	-1.020	9 - 6	-0.980	-	-0.920	109L 100-	Vdc	E 01 1	etognbo	6,9	and_outs	,	1,14
Logic "0" Threshold Voltage	V _{OLA} ②	3 4 11 12	-	-1.615	7	-1.600		-1.575	Vdc	premon notice a	estudign estudign estudign	9 6 9 6	6 9 6 9	7	d v

	TEST VOLTAGE VALUES											
MBAN	(Volts)											
@ Test emperature	V _{IH} max	VIL min	VIHA min	VILA max	Vcc							
0°C	+4.160	+3.130	+3.855	+3.510	+5.0							
25°C	+4.190	+3.150	+3.895	+3.525	+5.0							
75°C	+4.280	+3.170	+3.955	+3.550	+5.0							

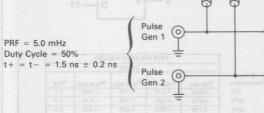
Supply Voltage = +5.0V

			97777	1	,	MC12040						7			-
	VOLTA	Pin	0'	°С	25	200000000000000000000000000000000000000	+7	5°C	A STATE OF	TEST VOLTAGE APPLIED TO PINS LISTED BELOW:					(VEE
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Unit	VIH max	VIL min	VIHA min	VILA max	Vcc	Gnd
Power Supply Drain Current	ΙĘ	7	-	15-15	-115	-60	100		mAdc		TENNO.	togn()	-	1,14	7
Input Current	INH	6 9	Cin			350 350	8.8	5.6	μAdc μAdc	6 9	_a	13	1 18+4+	1,14 1,14	7 7
Logic "1" Output Voltage	VoH ①	3 4 11 12	4.000	4.160	4.040	4.190	4.100	4.280	Vdc	6.0 4.6 5.4-	-8 -8	8,0 8,0 15,8 15,8	1 15+12 16+3- 16-11	1,14	7
Logic "0" Output Voltage	VOL ①	3 4 11 12	3.190	3.430	3.210	3.440	3.230	3.470	Vdc	-0:8 -d:A -8:4	-A -A -B	2.69 2.09 1.43	4+01-1 21+07 4+01-1	1,14	7
Logic "1" Threshold Voltage	VOHA 2	3 8 4 9 11 12	3.980	1 - 1	4.020		4.080	I	Vdc	1:1	- 8 - 8 - A	6,9	167 187 - 1871 -	1,14	7
Logic "0" Threshold Voltage	VOLA 2	3 4 11 12		3.450	-	3.460	1111	3.490	Vdc	1.88	_A _B _B	9 6 9 6	6 9 6 9	1,14	7

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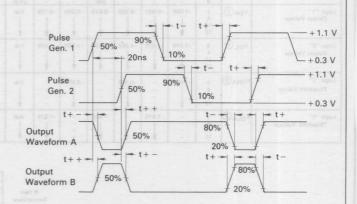
PRF = 5.0 mHz



To Scope Channel B -0 D \overline{D} 0.1 µF 六 $0 \text{ V}_{\text{FF}} = -3.2 \text{ or } -3.0 \text{ V}$

NOTES:

- 1. All input and output cables to the scope are equal lengths of 50 Ω coaxial cable.
- 2. Unused input and outputs are connected to a 50 Ω resistor to ground.
- 3. The device under test must be preconditioned before performing the ac tests. Preconditioning may be accomplished by applying pulse generator 1 for a minimum of two pulses prior to pulse generator 2. The device must be preconditioned again when inputs to pins 6 and 9 are interchanged. The same technique



	NATEU BIN		UWA BOAT	OW TEST	MC12040		0	MC12540		Po	TEST VOLTAGES/WAVEFORMS APPLIED TO PINS LISTED BELOW:						
Characteristic	MADY .	Pin	Output	0°C	+25°C	+75°C	-55°C	+25°C	+125°C	5147	Pulse	Pulse	VEE	Vcc			
	Symbol		Waveform	Max	Max	Max	Max	Max	Max	Unit	Gen. 1	Gen. 2	-3.0 or -3.2 V				
Propagation Delay	t6+4+	6,4	В	4.6	4.6	5.6	4.6	4.6	5.0	ns	6	9	7	1,14			
	t6+12+	6,12	A	6.0	6.0	7.2	6.0	6.0	6.6		9	6					
	t6+3-	6,3	A	4.5	4.5	5.5	4.5	4.5	4.9	1 100	6	9	and the second of	1 3 8			
	t6+11-	6,11	В	6.4	6.4	7.7	6.4	6.4	7.0		9	6					
	t9+11+	9,11	В	4.6	4.6	5.6	4.6	4.6	5.0	1 1	9	6					
	t9+3+	9,3	A	6.0	6.0	7.2	6.0	6.0	6.6	107	6	9		0.0			
	t9+12-	9.12	A	4.5	4.5	5.5	4.5	4.5	4.9		9	6	Server S	agrain.			
	t9+4-	9,4	В	6.4	6.4	7.7	6.4	6.4	7.0		6	9	*	1			
Output Rise Time	t3+	3	A	3.4	3.4	3.8	3.4	3.4	3.8	ns	6	9	7	1,14			
	t4+	4	В	1	parv -		083.4	0.00	0 1	488	6	9	1	1			
	t11+	11	В							1.11	9	6	sol nov sky	2507			
	t12+	12	A	*	1		1		4		9	6	*				
Output Fall Time	t3-	3	A	3.4	3.4	3.8	3.4	3.4	3.8	ns	6	9	7	1,14			
	t4-	4	В	1-				1 1	1	1	6	9	1	1			
	t11-	11	В					1 1 3			9	6	TEN VOI BIR	TO SEE			
	t12-	12	- A	1		. 1	1				9	6	*	1			

APPLICATIONS INFORMATION

The MC12040 is a logic network designed for use as a phase comparator for MECL-compatible input signals. It determines the "lead" or "lag" phase relationship and the time difference between the leading edges of the waveforms. Since these edges occur only once per cycle, the detector has a range of $\pm 2\pi$ radians.

Operation of the device may be illustrated by assuming two waveforms, R and V (Figure 1), of the same frequency but differing in phase. If the logic had established by past history that R was leading V, the U output of the detector (pin 4) would produce a positive pulse width equal to the phase difference and the D output (pin 11) would simply remain low.

On the other hand, it is also possible that V was leading R (Figure 1), giving rise to a positive pulse on the D output and a constant low level on the U output pin. Both outputs for the sample condition are valid since the determination of lead or lag is dependent on past edge crossing and initial conditions at start-up. A stable phase-locked loop will result from either condition.

Phase error information is contained in the output duty cycle — that is, the ratio of the output pulse width to total period. By integrating or low-pass filtering the outputs of the detector and shifting the level to accommodate ECL swings, usable analog information for the voltage-controlled oscillator can be developed. A circuit useful for this function is shown in Figure 2.

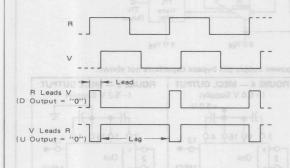
Proper level shifting is accomplished by differentially

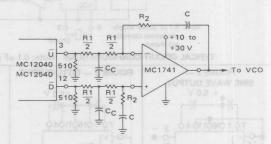
FIGURE 1 - TIMING DIAGRAM

driving the operational amplifier from the normally high outputs of the phase detector (\overline{U} and \overline{D}). Using this technique the quiescent differential voltage to the operational amplifier is zero (assuming matched "1" levels from the phase detector). The \overline{U} and \overline{D} outputs are then used to pass along phase information to the operational amplifier. Phase error summing is accomplished through resistors R1 connected to the inputs of the operational amplifier. Some R-C filtering imbedded within the input network (Figure 2) may be very beneficial since the very narrow correctional pulses of the MC12040 would not normally be integrated by the amplifier. General design guides for calculating R1, R2, and C are included in the MC4044 data sheet. Phase detector gain for this configuration is approximately 0.16 volts/radian.

System phase error stems from input offset voltage in the operational amplifier, mismatching of nominally equal resistors, and mismatching of phase detector "high" states between the outputs used for threshold setting and phase measuring. All these effects are reflected in the gain constant. For example, a 16 mV offset voltage in the amplifier would cause an error of 0.016/0.16 = 0.1 radian or 5.7 degrees of error. Phase error can be trimmed to zero initially by trimming either input offset or one of the threshold resistors (R1 in Figure 2). Phase error over temperature depends on how much the offending parameters drift.

FIGURE 2 — TYPICAL FILTER AND SUMMING NETWORK



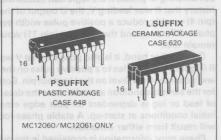


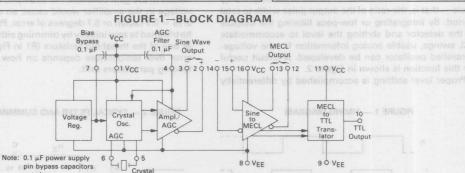
CRYSTAL OSCILLATOR

The MC12060/12560 and MC12061/12561 are for use with an external crystal to form a crystal controlled oscillator. In addition to the fundamental series mode crystal, two bypass capacitors are required (plus usual power supply pin bypass capacitors). Translators are provided internally for MECL and TTL outputs.

- Frequency Range = 100 KHz to 2.0 MHz for MC12060/12560
 2.0 MHz to 20 MHz for MC12061/12561
- Temperature Range = -55°C to +125°C for MC12560/561 0°C to +70°C for MC12060/061
- Single Supply Operation: +5.0 Vdc or -5.2 Vdc
 - Three Outputs Available:
- 1. Complementary Sine Wave (600 mVp-p typ)
- 2. Complementary MECL
- 3. Single Ended TTL

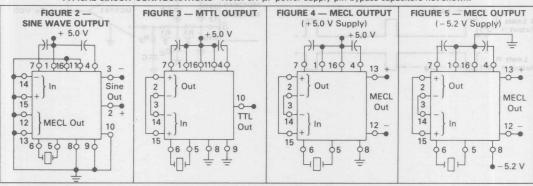
CRYSTAL OSCILLATOR





PPEICATIONS INFORMATIC

TYPICAL CIRCUIT CONFIGURATIONS Note: 0.1 μF power supply pin bypass capacitors not shown.

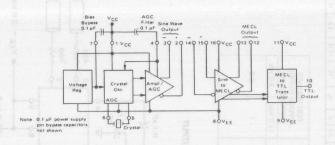


CRYSTAL REQUIREMENTS

Note: Start-up stabilization time is a function of crystal series resistance. The lower the resistance, the faster the circuit stabilizes.

Characteristic	MC12060/12560	MC12061/12561
Mode of Operation	Fundamental S	eries Resonance
Frequency Range	100 kHz — 2.0 MHz	2.0 MHz — 20 MHz
Series Resistance, R1	Minimum at	Fundamental
Maximum Effective Resistance RE(max)	4k ohms	155 ohms

ELECTRICAL CHARACTERISTICS

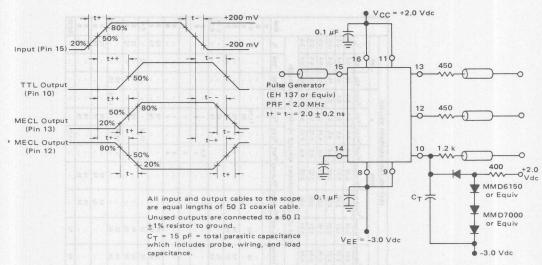


			di.	TEST	VOLTAG	E/CUR	RENT	VALL	JES				
			Volts										
	Test	VIHmax	VILmin	VIHAmin	VILAmax	VIHT	VCCL	vcc	VCCH	lor	OL OH I		
	-55°C	4.07	3 18	3.72	3.49	4.0	4.5	5.0	5.5	16	-0.4	-2.5	
MC12560 MC12561	+25°C	4.19	3.21	3.90	3.52	4.0	4.5	5.0	5.5	16	-0.4	-2.5	
WC 12501	+125°C	4.37	3.25	4.03	3.60	4.0	4.5	5.0	5.5	16	-0.4	-2.5	
	0°C	4.16	3.19	3.86	3.51	4.0	4.75	5.0	5.25	16	-0.4	-2.5	
MC12060 MC12061	+25°C	4.19	3.21	3.90	3.52	4.0	4.75	5.0	5.25	16	-0.4	-2.5	
MC12001	+75°C	4.28	3.23	3.96	3.55	4.0	4.75	5.0	5.25	16	-0.4	-2.5	

					1					7.91	144				C1200	+7	5°C	4.28	3.23	3.96	3.55	4.0	4.75	5.0	5.25	16	-0.4	-2.5	
		Pin				2560/1		. 8.5			M. A.	MC1	2060/	12061		7			TEST VO	LTAGE/C	URRENT	APPLI	ED TO	PINS	LISTER	BEL	ow		
		Under	-55	°C		+25°C	0.00	+12	5°C	00	С		+25°C		+75	5°C	10	-		10.00		1				W C			
Characteristic	Symbol	nbol Test	Min	Max	Min	Тур	Max	Min	Max	Min	Max	Min	Тур	Max	Min	Max	Unit	Unit VIHmax	VILmin	VIHAmin	VILAmax	VIHT	VCCL	VCC	VCCH	OL	IOH	1L	Gn
Power Supply MC12060/12560	1cc	1			13	16	19	00.0				13	16	19	7 2 1	14.	mAdo		-					1	All Sea	(2)			8
Drain Current MC12061/12561		11			18	3.0	28 4.0	80.0	-	Line.	8.0	18	23 3.0	28		-		14	15	1-1	=	-	-	1 11,16	-	-	-	6.5	8,9
		16			13	16	19	-		150		13	16	19	-	0.1	V	-	15-	17-5	-	-	- 1	16	-	-	-	-	8
Input Current	INH	14	100			- 2	250 250	21	-	-	8-5	-	1	250 250	8 6		μAdc μAdc	14	15 14	100	-	12	-	16 16	I	2	_	101	8
	INL	14 15					1.0	-	-	-	-			1.0	0.0		μAdc μAdc	15 14	1 -6	4-1	178	-	12	16 16	1	-	1	-	8,1
Differential Offset Voltage MC12061/12561	7 \	4 to 7 2 to 3			40 - 150	0	325 +150	Mi.e	-	Style.	-	40 -200	0	325 +200	-	-	m∨dc	- 1	128		-	5,6 4	-	1	-	-	1	3	8
MC12060/12560		2 to 3	1		-220	0	+220			-		-300	Ball	+300	7 7 %		lali	LUE	10 2			4		1					8
Output Voltage Level	Vout	2 3	3			3.5 3.5		**	-		-	-	3.5 3.5	1	-	-	Vdc Vdc			129	-	4	-	1	=	-	-	-	8
Logic "1" Output Voltage	VOH1.	12	3 92 3 92		4.04	-	4.19		4 37	4.00	4.16	4.04	12	4.19	4.10		Vdc Vdc	14 15	15 14		- 1	-	-	16 16	-	=	I	12 13	8
	VOH2	10	2.4	-	2.4		1 .20	2.4		2.4	-	2.4	-	-	2.4		Vdc	15	14	_	- 10	-	11,16	_	1	-	10	-	8,9
Logic "0" Output Voltage	VOL1	12	297	3.39	3.00	-	3.44	3.04	3.50 3.50	2.98	3.43	3.00		3.44	3.02	3.47	Vdc Vdc	15 14	14 15	-	5	E.	Jos	16 16	1	-	-	12 13	8
	VOL2	10	1000	0.5			0.5	-	0.5	-	0.5	-	=	0.5	-	0.5	Vdc Vdc	14	15 15	-		-	11,16	-	11,16	10	_		8,9
Logic "1" Threshold Voltage	VOHA	12 13	3.90 3.90	-	4.02	-		4.15 4.15	W.	3.98	-	4.02	-	1	4.08	-	Vdc Vdc		-	14 15	15 14	-8	-	16 16	-	-	-	12	8
Logic "0" Threshold Voltage	VOLA	12 13	1	3.41	-	-	3.46 3.46	-	3.52 3.52	-	3.45 3.45	-	-	3.46 3.46	-	3.49	Vdc Vdc	-	-	15 14	14	=	-	16 16	-	-	-	12 13	8
Output Short-Circuit Current	los	10	20	60	20	-	60	20	60	20	60	20	-	60	20	60	mAdo	15	14	_	-	-	11,16	-	-	-	-	15	8,9,1

^{*}Devices will meet standard MECL logic levels using VEE $^{-}$ -5.2 Vdc and VCC $^{-}$ 0.

FIGURE 6 — AC CHARACTERISTICS — MECL AND TTL OUTPUTS



Characteristic	In the sale	Pin	MC12560/12561							MC12060/12061								TEST VOLTAGES/WAVEFORMS						
	TO BE SHOW	Under	-55°C		+25°C		+125°C		0°C		+25°C			+7	5°C		APP	LIED TO P	INS LIST	D BELOV	V:			
	Symbol		Min	Max	Min	Тур	Max	Min	Max	Min	Max	Min	Тур	Max	Min	Max	Unit	Pulse In	Pulse Out	+2.0 Vdc	-3.0 Vdc	Gnd		
Propagation Delay	t15+10+	10	1 -	30		17	25	-	30	-	22	-	17	25	223	27	ns	15	10	11,16	8,9	14		
	115-10-	10	-	22	-	12	18	-	22		19		12	18		18		1	10	1	1	1		
	115+12-	12		5.0	-	4.3	5.5		6.0	-	5.2	12-25	4.3	5.5	-	5.8			12	5 9 h				
	115-12+	12	-	4.8	-	3.7	5.2	-	5.5	14.5	5.0	-	3.7	5.2	-	5.2			12	18 8 8				
	115+13+	13	-	4.6	-	4.0	5.0		5.4	-	4.8	-	4.0	5.0	-	5.2	1	1	13		-	1		
	t15-13-	13	LIE'S	5.0	0.7	4.0	5.0	-	5.2	-	5.0	-	4.0	5.0	-	5.1	V	V	13		V	V		
Rise Time	112+	12	-	3.8	1	3.0	4.0	7.47	5.0	0.5	40	-	3.0	4.0	-	4.4	ns	15	12	11,16	8,9	14		
	t13+	13	-00	3.8		3.0	4.0	-	5.0	-	4.0	-	3.0	4.0		4.4	ns	15	13	11,16	8,9	14		
Fall Time	112-	12	-	3.8	-	3.0	4.0	-	4.5		4.0	-	3.0	4.0	-	4.0	ns	15	12	11,16	8,9	14		
	t13-	13	1	3.8	-	3.0	4.0	-	4.5	-	40	-	3.0	4.0		4.0	ns	15	13	11,16	8,9	14		

	Pin	MC1 MC1	2560 2561	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	2060 2061		TEST VOLTAGE APPLIED TO PINS			
5 2 9 10 9 1	Under	+2!	5°C	+25	5°C		LISTED BELOW			
Characteristic	Test	Min	Тур	Min	Тур	Unit	+2.0 Vdc	-3.0 Vdc		
Sine Wave Amplitude MC12060/12560	2 3	600 600	675 675	500 500	650 650	mVp-p	1	8.9		
MC12061/12561	2 3	700 700	750 750	650 650	750 750					

FIGURE 7 — AC TEST CIRCUIT — SINE WAVE OUTPUT

All output cables to the scope are equal lengths of 50 Ω coaxial cable. All unused cables must be terminated with a 50 $\Omega\pm1\%$ resistor to ground.

 $450\;\Omega$ resistor and the scope termination impedance constitute a 10.1 attenuator probe.

Crystal—Reeves Hoffman Series Mode,

Series Resistance Minimum at Fundamental

Fundamenta

MC12060/12560 MC12061/12561 f = 500 KHz f = 10 MHz

f = 500 KHz R_E = 1 K Ω

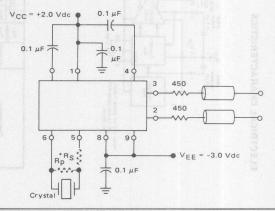
 $R_E = 5 \Omega$

*R_S MC12060/12560 = 3K Ω

MC12061/12561 = 15K Ω is inserted only for test purposes. When used with the above specified crystal, it guarantees oscillation with any crystal which has an equivalent series resistance

 \leqslant 155 Ω for MC12061/12561 and \leqslant 4K Ω for MC12060/12560

 R_{p} : will improve start up problems value: 200-500 Ω



7

OPERATING CHARACTERISTICS

The MC12061/12561 and MC12060/12560 consist of three basic sections: an oscillator with AGC and two translators (Figure 1). Buffered complementary sine wave outputs are available from the oscillator section. The translators convert these sine wave outputs to levels compatible with MECL and/or TTL.

Series mode crystals should be used with the oscillator. If it is necessary or desirable to adjust the crystal frequency, a reactive element can be inserted in series with the crystal—an inductor to lower the frequency or a capacitor to raise it. When such an adjustment is necessary, it is recommended that the crystal be specified slightly lower in frequency and a series trimmer capacitor be added to bring the oscillator back on frequency. As the oscillator frequency is changed from the natural resonance of the crystal, more and more dependence is placed on the external reactance, and temperature drift of the trimming components then affects overall oscillator performance.

The MC12061/12561 and MC12060/12560 are designed to operate from a single supply—either +5.0 Vdc or -5.2 Vdc. Although each translator has separate V_{CC} and V_{EE} supply pins, the circuit is NOT designed to operate from both voltage levels at the same time. The separate V_{EE} pin from the TTL translator helps minimize translent disturbance. If neither translator is being used, all unused pins (9 thru 16) should be connected to V_{EE} (pin 8). With the translators not powered, supply current drain is typically reduced from 42 mA to 23 mA for the MC12061/12561, and 35 mA to 16 mA for the MC12060/12560.

Frequency Stability

Output frequency of different oscillator circuits (of a given device type number) will vary somewhat when used with a given test setup, however the variation should be within approximately ±0.001% from unit to unit.

Frequency variations with temperature (independent of the crystal, which is held at 25°C) are small—about -0.08 ppm/°C for MC12061/12561 operating at 8.0 MHz, and about -0.16 ppm/°C for MC12060/12560 operating at 1.0 MHz (see figure 8).

Signal Characteristics

The sine wave outputs at either pin 2 or pin 3 will typically range from 800 mVp-p (no load) to 500 mVp-p (120 ohm ac load). Approximately 500 mVp-p can be provided across 50 ohms by slightly increasing the dc current in the output buffer by the addition of an external resistor (680 ohms) from pin 2 or 3 to ground, as shown in Figure 9. Frequency drift is typically less than 0.0003% when going from a high-impedance load (1 megohm, 15 pF) to the 50-ohm load of Figure 9. The dc voltage level at pin 2 or 3 is nominally 3.5 Vdc with V_{CC} = +5.0 Vdc.

Harmonic distortion content in the sine wave outputs is crystal as well as circuit dependent, The largest harmonic (third) will usually be at least 15 dB down from the fundamental. The harmonic content is approximately load independent except that the higher harmonic levels (greater than

the fifth) are increased when the MECL translator is being driven.

Typically, the MECL outputs (pins 12 and 13) will drive up to five gates, as defined in Figure 10, and the TTL output (pin 10) will drive up to ten gates, as defined in Figure 11.

Noise Characteristics

Noise level evaluation of the sine wave outputs using the circuit of Figure 12, with operation at 1.0 MHz for MC12060/12560 or 9.0 MHz for MC12061/12561, indicates the following characteristics:

- Noise floor (200 kHz from oscillator center frequency) is approximately -122 dB when referenced to a 1.0 Hz bandwidth. Noise floor is not sensitive to load conditions and/or translator operation.
- Close-in noise (100 Hz from oscillator center frequency) is approximately –88 dB when referenced to a 1.0 Hz bandwidth.

FIGURE 8 — FREQUENCY SHIFT VERSUS TEMPERATURE

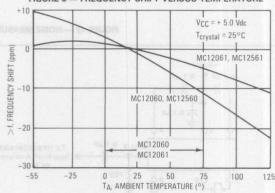
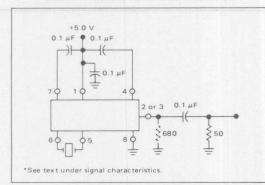
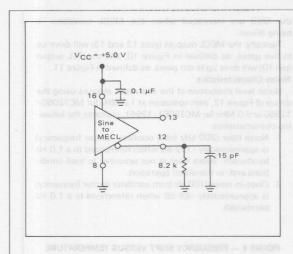


FIGURE 9 — DRIVING LOW-IMPEDANCE LOADS



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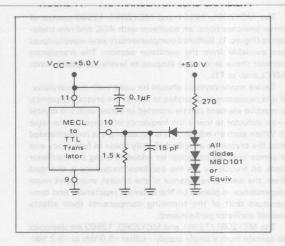
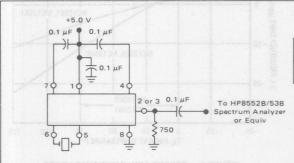
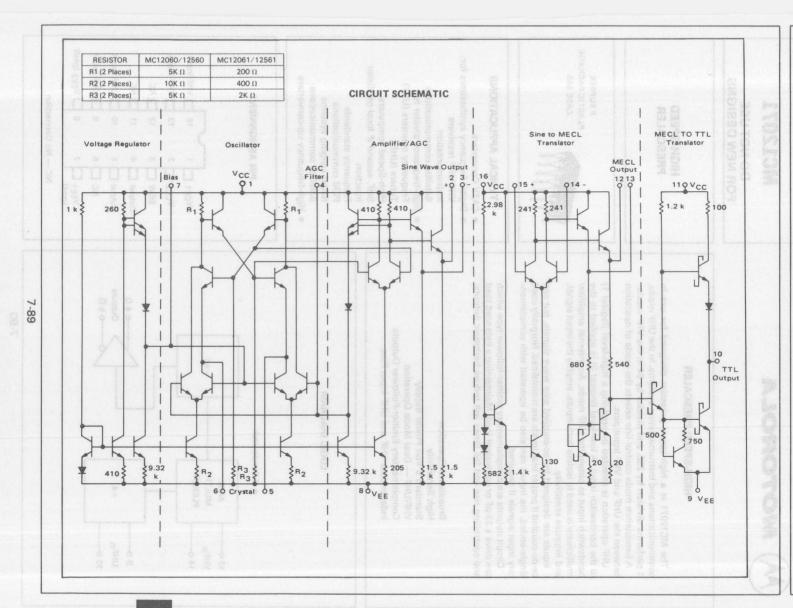


FIGURE 12 — NOISE MEASUREMENT TEST CIRCUIT



Measurement	Sweep	Bandwidth	Video Filter
Noise Floor	50 kHz/div	10 kHz	10 Hz
Close-In Noise	20 kHz/div	10 Hz	10 Hz

7





MC12071

DO NOT USE FOR NEW DESIGNS

HIGH-SPEED PRESCALER

The MC12071 is a high-speed prescaler designed for use in communications and instrumentation systems. In the UHF mode, it performs division by 256, and divides by 64 in the VHF mode.

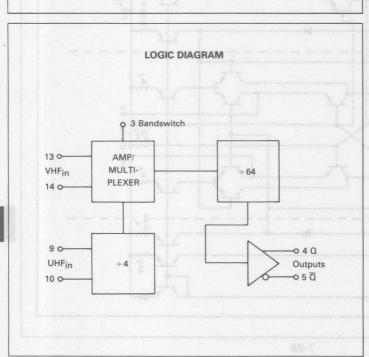
A bandswitch mode control line selects the mode of operation between the UHF and VHF input pins.

UHF operation is selected by applying a high-level (logical 1) to the bandswitch input. A low-level (logical 0) is applied to the bandswitch input to obtain the VHF mode. An internal amplifier/multiplexer is used to isolate both inputs, amplify the input signal, and improve sensitivity.

Inputs are designed for ac-coupled sine wave signals, but can be dc-coupled if proper bias levels are maintained. Normally used single-ended, the inputs can also be operated with complementary input signals if required.

Circuit outputs are complementary emitter-follower type which can drive a 33-pF or equivalent load. Maintaining a balanced load and controlling rise and fall times will reduce harmonic outputs.

Broadband Operation
High Sensitivity
Standard 5 Volt Power Supply
VHF/UHF — Dual Mode Operation
Complementary Emitter-Follower Outputs
Independent VHF and UHF Input Pins



HIGH-SPEED PRESCALER



P SUFFIX
PLASTIC PACKAGE
CASE 646

TYPICAL APPLICATIONS

- CATV Converters
- Digital frequency synthesizers for: VHF/UHF receivers Instrumentation
 Satellite communications
- High-frequency divider for:
 Frequency counters (UHF)
 Timers (UHF)
 High-Speed computers
 SHF, second IF local-oscillator injection
 Frequency standards
 PCM communications
 Radar ranging systems
- Satellite communications

 High-frequency up-converters

PIN ASSIGNMENT VHF Input VCC1 [VCC2 13 VHF Input BSW [12 ☐ NC Output [11 ☐ NC Output [UHF Input UHF Input NC [VEE1 VEE2 (gnd)

NC - No Connection

MOTEORY

MAXIMUM RATING

Rating	Symbol	Value	Unit
Power Supply Voltage	Vcc	7.0	Vdc
Operating Power Supply Voltage	Vcc	5.0 ± 10%	Vdc
Bandswitch Voltage	V _B H	20	Vdc
Input Voltage	Vin	0.5	VRMS
Operating Temperature Range	TA	0 to +70	оС
Storage Temperature Range	T _{stg}	-55 to +125	°C
Junction Temperature	Tj	150	°C

Ratings above which device life may be impaired.

ELECTRICAL CHARACTERISTICS (VCC = 5.0 V, TA = 0°C to +70°C)

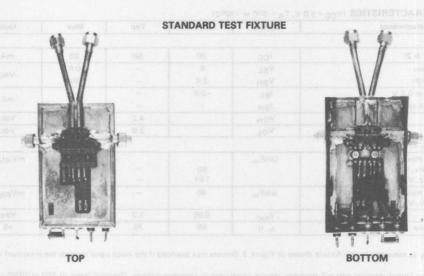
Characteristics	Symbol	Min	Тур	Max	Unit
STATIC				11.1	
Supply Current (Pins 1 & 2)	lcc	30	60	90	mA
Bandswitch Voltage, Low	V _B L	0		0.8	Vdc
High	V _{BH}	2.4	-	20	Vac
Bandswitch current 0 to 0.8 V	IBL	-0.5		-	
2.4 to 20 V	Івн		- 0	0.5	mA
Output Voltage, High	Voн		4.2		Vdc
Output Voltage, Low	VOL		3.0		Vdc
DYNAMIC (See Fig. 2)				Kara Maria	
UHF Input Sensitivity Range (See note)	UHFin				mVRMS
f _{in} = 450 to 950 MHz, V _{BH}		60		*200	
fin = 80 to 450 MHz, V _{BH}		150	- 1	500	
VHF Input Sensitivity Range (See note) fin = 90 to 275 MHz, VBL	VHFin	40	- 1	500	mVRMS
Output Voltage	V _{out}	0.65	1.2	1.6	Vp-p
Output Rise or Fall Time	t _r , t _f	40	70	110	nS

NOTE:

UHF input sensitivity as measured in test fixture shown in Figure 2. Devices may overload if the input signal exceeds the maximum level specified.

* Overload levels are very layout sensitive and will probably require correlation in customer circuits. Overload levels of 500 mVRMS can easily be attained with various layouts.

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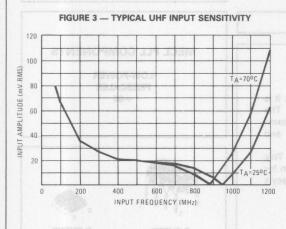
TEST FIXTURE CONSIDERATIONS

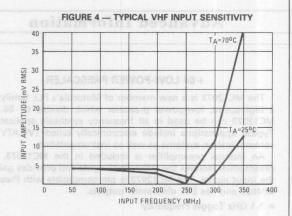
Pictured above is our standard MC12071 test fixture. High-frequency construction and design techniques are a must if the operation of the test fixture is to be stable and repeatable. Listed below are some considerations which must be observed to insure proper operation of the test circuit.

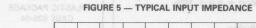
- Use a good ground plane with frequent ground connections.
- Use best available high-frequency type socket.
- Maintain a 50Ω environment on inputs except where it is necessary for the signal to pass through a component.
- Use best available high-frequency components and keep lead length to an absolute minimum. (Chip type ceramic capacitors are preferable.)
- Pin bypasses should be placed as close to the device as possible.

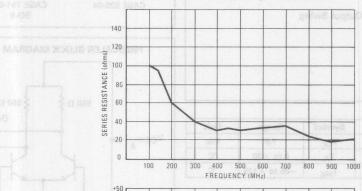
Note: Even after implementing the above fixture design and construction techniques some minimal correlation differences may exist due to inherent highfrequency characteristics variations.

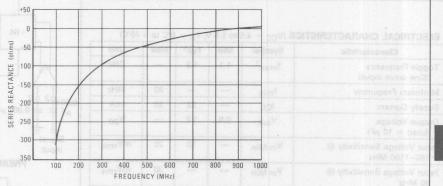
7











SELECTION AND INCOME.

Strenge Temperature Range



MC12073

Advanced Information

÷64 LOW-POWER PRESCALER

The MC12073 is a new member of Motorola's PLL family. It is a high-speed, low-power prescaler which divides by 64. The MC12073 can be used in all frequency synthesis applications. Typical applications include electronically tuned TV/CATV and communication systems as well as instrumentation.

An internal preamplifier is included in the MC12073. This preamplifier isolates the differential inputs and provides gain for the input signal. The MC12073 is pin compatible with Plessey's SP4632 and has ECL differential outputs.

- 1.1 GHz Toggle Frequency
- Low-Power: 23 mA Typical @ V_{CC} = 5.0 V
- \bullet High Input Sensitivity, 20 mV $_{rms}$ @ V $_{CC}$ = 5.0 \pm 10%, T $_{A}$ = 0° to +70°C
- 800 mV Minimum Peak-Peak Output Swing
- ECL Outputs

MAXIMUM RATINGS

MAXIMOM NATINGO			
Characteristic	Symbol	Range	Unit
Power Supply Voltage	Vcc	7.0	Vdc
Operating Temperature Range	TA	0 to +70	°C
Storage Temperature Range	T _{sta}	-65 to +175	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V, T_A = 0°C to +70°C)

Characteristic	Symbol	Min	Typ*	Max	Unit
Toggle Frequency (Sine wave input)	f _{max} 1	1.1	1.3	-	GHz
Minimum Frequency	fmin	-	-	90	MHz
Supply Current	Icc	-	23	30	mA
Output Voltage (Load = 10 pF)	V _{out}	0.8	1.2	-	V _{pp}
Input Voltage Sensitivity @ 150-1100 MHz	V _{in Min}	-	10	20	mV _{rms}
Input Voltage Sensitivity @ 90 MHz	V _{in Min}			30	mV _{rms}
Input Overload	V _{in Max}	200	400	-	mV _{rms}

^{*}Typical measured at +25°C, 5.0 V

¹See Figure 1

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MECL is a trademark of Motorola Inc.

MECL PLL COMPONENTS

LOW-POWER PRESCALER ÷ 64

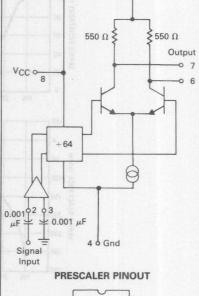


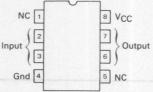
P SUFFIX
PLASTIC PACKAGE
CASE 626-04



D SUFFIX
PLASTIC PACKAGE
CASE 751-01
SO-8

PRESCALER BLOCK DIAGRAM





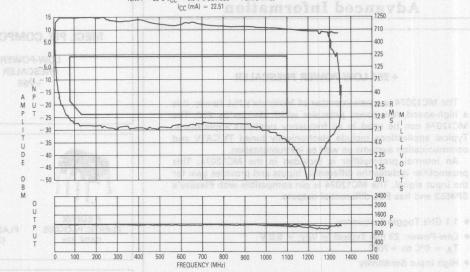
ATULLUM

FIGURE 1

DEVICE MC12073 RATIO 64 MAXIMUM TOGGLE FREQ: MIN = 1348 MEAN = 1348 MAX 1348

TEMP. = 25°C V_{CC} = 5.0 V #DEVICES = 1 DATE 1/7/85

I_{CC} (mA) = 22.51



OUTLINE DIMENSIONS

1. LEAD POSITIONAL TOLERANCE: + φ 0.13 (0.005) M T A M B M 2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL. 3. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS). 4. DIMENSIONS A AND B ARE DATUMS. 5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. P SUFFIX PLASTIC PACKAGE

7 ঘ

G D

SEATING

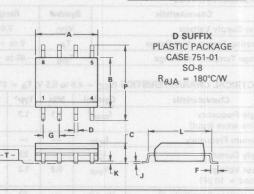
	MILLIN	METERS	INCHES				
DIM	MIN	MAX	MIN	MAX			
A	9.40	10.16	0.370	0.400			
В	6.10	6.60	0.240	0.260			
C	3.94	4.45	0.155	0.175			
D	0.38	0.51	0.015	0.020			
F	1.02	1.52	0.040	0.060			
G	2.54	BSC	0.100 BSC				
H	0.76	1.27	0.030	0.050			
J	0.20	0.30	0.008	0.012			
K	2.92	3.43	0.115	0.135			
L	7.62	BSC	0.300	BSC			
M	_	10°	_	10°			
N	0.51	0.76	0.020	0.030			

CASE 626-04

STYLE 1: PIN 1. AC IN 2. DC + IN 3. DC - IN 4. AC IN 5. GROUND

6. OUTPUT 7. AUXILIARY 8. VCC

	1 1 1 1	MILLIN	METERS	INC	HES
	DIM	MIN	MAX	MIN	MAX
IOTES:	A	4.78	5.00	0.188	0.197
1T- IS SEATING PLANE.	В	3.81	4.01	0.150	0.158
2. DIMENSION A IS DATUM.	C	1.35	1.75	0.053	0.069
3. POSITIONAL TOLERANCE	D	0.35	0.46	0.014	0.018
FOR LEADS:	F	0.67	0.77	0.026	0.030
	G	1.27	BSC	0.050	BSC
♦ 0.25 (0.010) M A S	J	0.19	0.22	0.007	0.009
	K	0.10	0.20	0.004	0.008
	L	4.82	5.21	0.189	0.205
	P	5.79	6.20	0.228	0.244



Advanced Information

÷ 256 LOW-POWER PRESCALER

The MC12074 is a new member of Motorola's PLL family. It is a high-speed, low-power prescaler which divides by 256. The MC12074 can be used in all frequency synthesis applications. Typical applications include electronically tuned TV/CATV and communication systems as well as instrumentation.

An internal preamplifier is included in the MC12074. This preamplifier isolates the differential inputs and provides gain for the input signal. The MC12074 is pin compatible with Plessey's SP4653 and has ECL differential outputs.

- 1.1 GHz Toggle Frequency
- Low-Power: 23 mA Typical @ $V_{CC} = 5.0 \text{ V}$ TA = 0°C to +70°C
- High Input Sensitivity
- 800 mV Minimum Peak-Peak Output Swing
- ECL Outputs

MAXIMUM RATINGS

Characteristic	Symbol	Range	Unit
Power Supply Voltage	Vcc	7.0	Vdc
Operating Temperature Range	TA	0 to +70	°C
Storage Temperature Range	T _{stg}	-65 to +175	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V, T_A = 0°C to +70°C)

Characteristic	Symbol	Min	Тур*	Max	Unit
Toggle Frequency (Sine wave input)	f _{max} 1	1.1	1.3	-	GHz
Minimum Frequency	fmin		_	90	MHz
Supply Current	Icc	-	23	30	mA
Output Voltage (Load = 10 pF)	Vout	0.8	1.2	-	V _{pp}
Input Voltage Sensitivity @ 150-1100 MHz	Vin Min	-	10	20	mV _{rms}
Input Voltage Sensitivity @ 90 MHz	Vin Min	-	-	30	mV _{rms}
Input Overload	Vin Max	200	400	_	mV _{rms}

^{*}Typical measured at +25°C, 5.0 V

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MECL PLL COMPONENTS

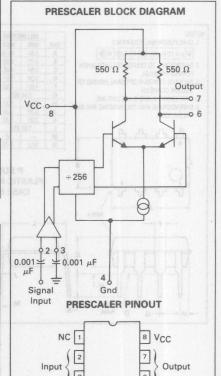
LOW-POWER PRESCALER ÷ 256







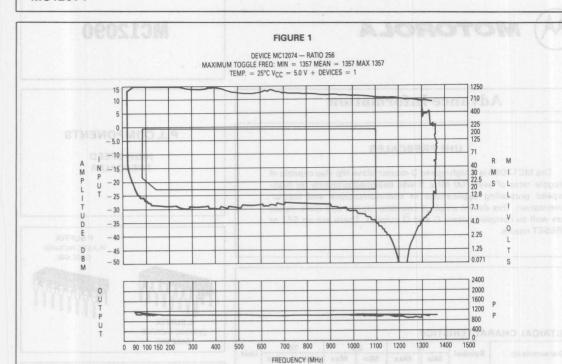
D SUFFIX PLASTIC PACKAGE CASE 751-01



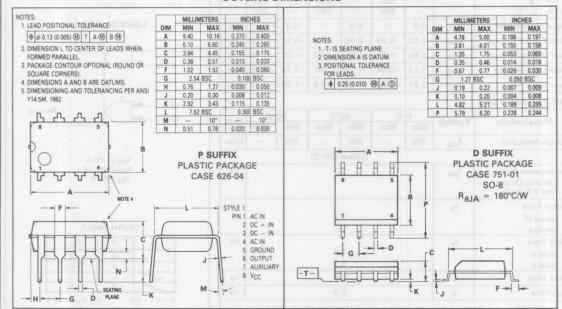
5 NC

7

¹See Figure 1



OUTLINE DIMENSIONS





MC12090

Advance Information

UHF PRESCALER

The MC12090 is a high-speed D master-slave flip-flop capable of toggle rates of over 700 MHz. It was designed primarily for highspeed prescaling applications in communications and instrumentation. This device employs two data inputs, two clock inputs as well as complementary Q and $\overline{\mathsf{Q}}$ outputs. There are no SET or RESET inputs.

ELECTRICAL CHARACTERISTICS

01	0 1 1	()°	2	5°	7	5°	
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	ΙE	-	65		59	-	65	mA
Input Current High Pin 7, 9 Pin 11, 12	linH	-	400 435	_	260 280	M <u>-1</u> 8	260 280	μА
Input Current Low	linL	0.5	_	0.5	-	0.3	-	μА
High Output Voltage	Voн	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	VOL	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	VIH	-1.17	-0.84	-1.13	-0.81	-1.70	-0.735	Vdc
Low Input Voltage	VIL	-1.87	-1.495	-1.85	-1.48	-1.83	-1.45	Vdc

AC PARAMETERS

Characteristic	6 1	0	°C	25	°C	75	°C	
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Toggle Frequency	f _{tog}	700	-	750	-	700	-	МН
	OTOTA 10			Typical	(25°C)			70
Propagation Delay (Clock to Output Pins 7 & 9-2)	t _{pd}			1	.3			ns
Setup Time ^t setup H ^t setup L	t _S		ŀ		.3		970X	ns
Hold Time ^t hold H ^t hold L	th		4+1	0	.3		UNIONE ORIGINA TURNIO RUCEXEA	ns
Rise Time	t _r	LA	.UEII	0	.9		007	ns
Fall Time	tf	X		0	.9		315	ns

PLL COMPONENTS

HIGH-SPEED PRESCALER

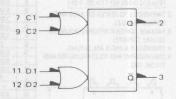
P SUFFIX PLASTIC PACKAGE CASE 648



CERAMIC PACKAGE CASE 620



LOGIC DIAGRAM



VCC1 = Pin 1 V_{CC2} = Pin 16 V_{EE} = Pin 8

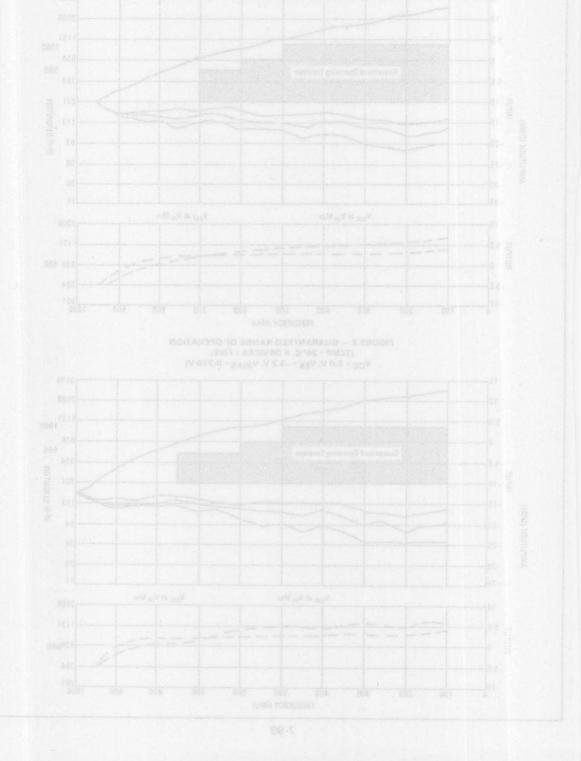
TRUTH TABLE

С	D	Q _{n+1}
L	φ	Qn
Н	φ	Qn
_	L	L
5	Н	Н

C = C1 + C2D = D1 + D2

φ = Don't Care

This document contains information on a new product. Specifications and information herein are subject to change without notice.





Quality and Reliability

The "BETTER" program is offered on ECL in dual-in-line ceramic and plastic packages. Motorola's reliability enhancement program was developed to provide improved levels of reliability for standard commercial products.

Motorola standard commercial integrated circuits are manufactured under stringent inprocess controls and quality inspections combined with the industries' finest outgoing quality inspections. The "BETTER" program offers three levels of extra processing, each tailored to meet different user needs at nominal costs.

The program is designed to:

- Reduces incoming electrical inspection.
- · Eliminate need for independent test labs and associated extra time and costs
- · Reduce field failures
- · Reduce service calls
- Reduce equipment downtime
- · Reduce board and system rework
- · Reduce infant mortality
- Save time and money
- Increase end-customer satisfaction

BETTER PROCESSING -STANDARD PRODUCT PLUS:

LEVEL I (Suffix S)

- 100% temperature cycling per MIL-STD-883. Method 1010, ten cycles from -25°C to +150°C.
- 100% functional and dc parametric tests at maximum rated temperature.

LEVEL II (Suffix D)

- 100% burn-in to MIL-STD-883 test conditions - 160 hours at +125°C or 1.0 eV Arrhenius time/temperature equivalent.
- · 100% post burn-in functional and dc parametric tests at 25°C (or max rated TA at Motorola's option). Maximum PDA of 2% (functional) and 5% (DC and functional)

LEVEL III (Suffix DS)

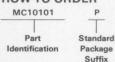
· Combination of Levels I and II above.

"MOTOROLA" AOL GUARANTEES

TEST	CONDITION		AQL1	
PRESE	CONDITION	LEVEL I	LEVEL II	LEVEL III
HIGH TEMPERATURE FUNCTIONAL	$T_A = MAX$	0.05	0.05	0.05
DC PARAMETRIC	T _A = 25°C	0.05	0.05	0.05
DC PARAMETRIC	TA MIN, TA MAX	0.25	0.25	0.25
AC PARAMETRIC	T _A = 25°C	0.05	0.05	0.05
EXTERNAL VISUAL AND MECHANICAL	MAJOR/MINOR	0.05	0.05	0.05
HERMETICITY (NOT APPLICABLE TO PLASTIC PACKAGES)	GROSS/FINE	0.15	0.15	0.15

^{1. &}quot;AQL" values shown are for reference only—"LTPD" type sampling plans are used that are equal to or tighter than values indicated. Also, the guaranteed electrical and visual/mechanical AQL levels will be progressively tightened. Contact Motorola sales office for latest values.

HOW TO ORDER



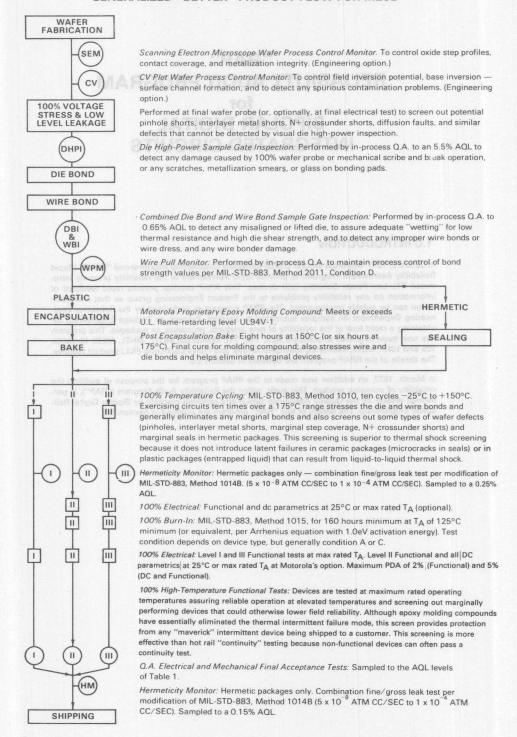
BETTER **PROCESSING** LEVEL I = SUFFIX S LEVEL II = SUFFIX D

LEVEL III = SUFFIX DS

PART MARKING

The Standard Motorola part number with the corresponding "BETTER" suffix can be ordered from your local authorized Motorola distributor or Motorola sales offices. "BETTER" pricing will be quoted as an adder to standard commercial product price.

GENERALIZED "BETTER" PRODUCT FLOW FOR MECL



"RAP" RELIABILITY AUDIT PROGRAM for BIPOLAR DIGITAL INTEGRATED CIRCUITS

1.0 INTRODUCTION

In January, 1977, Motorola Bipolar Digital Reliability Engineering implemented "RRAP" (Rapid Reliability Assessment Program) to provide rapid assessment of the reliability of newly introduced TTL Low-Power Schottky (LS) devices. This RRAP concept permits rapid feedback of information on any reliability problems to the Product Engineering group so that corrective action can be quickly implemented. The RRAP program is performed by the Reliability Engineering Department on samples submitted by Product, Process, or Package Engineering for obtaining a rapid look at the reliability of new products, processes, or packages. This program has now been extended to standard ALS, TTL, TTL Memories, MDTL, MHTL, MECL III, MECL 10K and 10KH, MECL Memories, Macrocell Arrays, and Phase Lock Loop (PLL) product families. The details of the RRAP program are outlined in Section 2.0.

In March, 1977, an addition was made to the RRAP program for the purpose of auditing the reliability of outgoing product. This audit, called the Reliability Audit Program ("RAP"), is performed weekly by the Quality Assurance Group and reported monthly by Bipolar Digital Reliability Engineering. The details of this "RAP" program are outlined in Section 3.0.

2.0 RAPID RELIABILITY ASSESSMENT PROGRAM (RRAP)

2.1 Hermetic Packaged Devices (50 Units minimum per Evaluation Sample)

- Electrical I (initial rejects removed from test) a.
- Temp Cycling -100 cycles (-65°C/+150°C) per Method 1010C
- Electrical I (plus Hermeticity per Method 1014 B & C for package evaluations only)
- "Equivalent" Burn-In for 40 hrs at 145°C per Method 1015 A or C d.
- e

2.2 Plastic Packaged Devices (100 Units minimum per Evaluation Sample)

	S/G 1 (30 Units)	S/G 2 (40 Units)	
a.	Electrical I	a. Electrical I	a. Electrical I
b.	Thermal Shock -200 cycles (-55°C/+125°C -30 Sec. dwell) Method 1011B, modified	 b. 16 hrs, PTHB; Rated V_{CC} or V_{EE} (15 psig, 100% RH, 121°C) Motorola test method 	b. Temp Cycling -100 cycles (-65°C/+150°C). Method 1010C c. Electrical I
c.	Electrical I	c. Electrical I	d. "Equivalent" Burn-In (40 hrs @
			e Flectrical I

NOTES:

- 1. All tests per MIL-STD-883 unless stated otherwise.
- 2. Electrical I = DC @ 25°C and functional @ 25°C Go/No/Go
- 3. 40 hr/145°C burn-in is "equivalent" to 160 hr/125°C burn-in using 1.0 eV activation energy and the Arrhenius equation for determining acceleration factor.
- 16 hrs of PTHB testing is equivalent to approximately 800 hrs of standard 85°C/85% RH THB testing for V_{CC}≤ 15 V, based on comparative tests performed by Motorola Reliability Engineering.
- 5. For each evaluation, the goal is zero failures. Any indicated failure is first verified and then submitted to the Product Analysis Lab for detailed analysis. Results of evaluation, along with analysis of any failure(s), are reviewed promptly with responsible design, product, process and package engineers.

3.0 RELIABILITY AUDIT PROGRAM (RAP) (per Motorola specification 12 MRM15301A)

- 3.1 PTHB 15 psig/121°C/100% RH at rated V_{CC} or V_{EE} for 16 hours performed on a weekly basis 0 rejects allowed out of 45 devices. (To be performed on plastic encapsulated devices only.) 48 hour read out also included for reliability engineering information only.
- 3.2 Temp Cycling MIL-STD-833, Method 1010, 1000 cycles, Condition C,

 —65°C/+150°C. Interim readout at 100 cycles (plastic and hermetic packages). Sample pulled on weekly basis 0 rejects allowed out of 45 devices after 1000 cycles; 1 reject allowed out of 45 devices after 1000 cycles.
- 3.3 Op. Life Test MIL-STD-883, Method 1005, Condition A (Reverse Bias) or C
 (Power plus Reverse Bias), T_A = 145°C; readouts at 40 hrs and 250 hrs
 (plastic and hermetic packages). Sample pulled on weekly basis 1 reject
 allowed out of 55 devices at 40 hr readout. No additional rejects allowed at
 250 hrs. If no rejects at 40 hrs, 1 reject allowed at 250 hrs.
- 3.4 Report Monthly Reliability Engineering computer printout summarizing test results.

NOTES: Machine 1

- 1. All standard 25°C dc and functional parameters will be measured Go/No/Go at each
 - Any indicated failure is first verified and then submitted to the Product Analysis Lab for detailed analysis.
 - If both plastic and hermetic packages are available, package type will be alternated weekly. Hermetic packages will include both cerdip CERDIP and LCC types.
 - 4. Device types sampled will be by generic type within each digital I/C product family (MDTL, MECL, TTL-LS, etc.) and will include all major package assembly options (U/S bond, ball bond, etc.) and all assembly locations (Korea, Philippines, Malaysia, etc.).
 - 5. 16 hrs PTHB is equivalent to approximately 800 hrs of 85°C/85% RH THB for VCC \leqslant 15 V
 - 6. Only moisture related failures (like corrosion) are criteria for failure on PTHB test.
 - 7. 40 hr/145°C Op Life is equivalent to 160 hr/125°C using 1.0 eV in Arrhenius equation.
 - 8. 250 hrs/145°C Op Life is equivalent to 1000 hrs/125°C using 1.0 eV in Arrhenius equation
- Special device specifications (48A's) for digital products will reference
 12MRM15301A as source of generic data for any customer required monthly audit reports.

HIGH RELIABILITY

STANDARD PROGRAMS

MIL-STD-883 OPERATIONS METHOD	PROCESSING PER 5004/5005	HI-REL JE PROCESSED F		MIL-M-38510 JAN QUALIFIED
SCREEN	CLASS B METHOD	CLASS B	CLASS C	CLASS B
Internal Visual (Precap)	2010 Condition B and 38510	100%	100%	100%
Stabilization Bake	1008 Condition C or Equivalent	100%	100%	100%
Temperature Cycling	1010 Condition C	100%	100%	100%
Constant Acceleration	2001 Condition E (min.) Y¹ Plane	100%	100%	100%
Seal (a) Fine (b) Gross	1014, Condition B 1014, Condition C	100% 100%	100% 100%	100% 100%
Interim Electrical Parameters	Per applicable device specification	Optional ¹	2 AO ,8 8a/	Optional ¹
Burn-in Test OM MONTADUSUS	1015 160 Hrs. @ 125° C Min. (4)	100%	EE DEVICE ASS TABLE)	100%
Final Electrical Tests (a) Static tests (1) 25°C (subgroup 1, table 1, 5005) (2) Max. and min. rated operating temp. (subgroups 2 and 3,	Per applicable device specification	100% 100% ⁽⁵⁾	100%	100% 100% ⁽⁵⁾
table 1, 5005) (b) Dynamic tests and/or switching tests @ 25°C (subgroup 4 and 9,		100%	(2)	100%
table 1, 5005) (c) Functional test @ 25°C (subgroup 7, table 1, 5005)	pio Mul 3 Pro	100%	100%	100%
Qualification or Quality Conformance Inspection	5005	Group A ³	Group A ³	per 38510 ³
External Visual	2009	100%	100%	100%

1. When specified in the applicable device specification, 100% of the devices shall be tested at Manufacturer's option.

2. Sample at Group A.

3. Full 5005 Conformance testing performed on Jan qualified product. Group A performed on Motorola HI-REL JEDEC processed product with either Generic or group B, C, D testing available.

 4. Optional 0.44 eV time-temperature "equivalent" burn-in per Figure 1015-1.
 5. AC sample testing at +125°C and -55°C on those types which require subgroup 10 and 11 testing per MIL-M-38510 Slash Sheet Specifications.



JEDEC Processed Product

Screening Levels Available: Class B & Class C

How to order JEDEC **Processed Product***

XXXXX/	A cos	Y	U14 Con Y on C	JC
MOTOROLA	CLASS B, OR C	CASE OUTLINE	LEAD FINISH	JEDEC DESIGNATOR
DEVICE TYPE (WITHOUT	(SEE DEVICE CLASS TABLE)	(SEE CASE OUTLINE TABLE)	(SEE LEAD FINISH TABLE)	PER JEDEC PUBLICATION NO.
LETTER PREFIX)				101

Case Outline Table
Source: MIL-M-38510D Amendment I

Letter	Appendix C Designation	0	Description
Α	F-1	14-lead	FP (1/4" x 1/4")
В	F-3	14-lead	FP (3/16" x 1/4")
C	D-1	14-lead	DIP (1/4" x 3/4")
D	F-2	14-lead	FP (1/4" x 3/8")
E	D-2	16-lead	DIP (1/4" x 7/8")
F	F-5	16-lead	FP (1/4" x 3/8")
G	A-1	8-lead	can
Н	F-4	10-lead	FP (1/4" x 1/4")
1 00	A-2	10-lead	can germen set
J	D-3	24-lead	DIP (1/4" x 1 1/4")
K	F-6	24-lead	FP (3/8" x 5/8")
L	NONE	NONE	estacheve
М	A-3	12-lead	
N	NONE	NONE	
P	D-4	8-lead	DIP (1/4" x 3/8")
Q	D-5	40-lead	DIP (9/16" x 2 1/16")
R	D-8	20-lead	DIP (1/4" x 1 1/16")
S	F-9	20-lead	FP (1/4" x 1/2")
T	NONE	NONE	
U	C-2	20 tern	ninal leadless chip
		carrier	
V	D-6	18-lead	DIP (0.300" x 1")
W	D-7		DIP (0.400" x 1.1")
X	Dual-in-line package	es not liste	ed above
Y	Flat packages not I		
Z	All other configura	tions not lis	sted above.
	Note: When orderi	ng Z Case	outline, Motorola case

Features:

- Lower cost than JAN-Qualified.
- 2. Devices manufactured using design and processing guidelines contained in MIL-M-38510 and MIL-STD-883
- 3. Product supplied with Motorola standard data sheet electricals

Example of JEDEC **Processed Markings**

MARKING: 10501/BEBJC

Lead F	inish	Table
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- A Type A or B Per MIL-M-38510 with hot solder dip
- B Type A or B Per MIL-M-38510 with tin plate
- C Type A or B Per MIL-M-38510 with gold plate
- X Any of the above, for ordering purposes only.



MIL-M-38510 JAN-Qualified Product



Screening Levels Available: Class B & Class C

How to order MIL-M-38510 JAN-Qualified Product

M38510 /XXX XX LEAD DEVICE TYPE CLASS B, OR C CASE INDICATES A MILITARY DETAIL QUALIFIED DESIGNATOR SPECIFICATION WITHIN DETAIL (SEE DEVICE OUTLINE FINISH SPECIFICATION CLASS TABLE) (SEE CASE (SEE LEAD NUMBER DEVICE **OUTLINE TABLE) FINISH TABLE)**

A F-1	Letter	Appendix C Designation	Description
C D-1 D 14-lead DIP (1/4" x 3/4") D F-2 14-lead FP (1/4" x 3/8") E D-2 F F-5 F-5 F-5 G A-1 H F-4 I 0-lead FP (1/4" x 1/4") I A-2 J D-3 K F-6 L NONE NONE M A-3 N NONE P D-4 D-5 B-lead DIP (1/4" x 1/4") I 12-lead can N NONE P D-4 D-5 B-lead DIP (1/4" x 1/4") I 24-lead FP (3/8" x 5/8") NONE P D-4 D-5 B-lead DIP (1/4" x 1/4") I 24-lead FP (3/8" x 5/8") NONE I 24-lead FP (3/8" x 5/8") NONE I 24-lead FP (3/8" x 5/8") NONE I 24-lead FP (3/8" x 5/8") NONE I 24-lead DIP (1/4" x 1/4") I 24-lead DIP (1/4" x 1/4") I 24-lead DIP (1/4" x 1/4") I 24-lead DIP (1/4" x 1/4") I 24-lead DIP (1/4" x 1/4") I 24-lead DIP (1/4" x 1/4") I 24-lead DIP (1/4" x 1/4") I 3-lead DIP (1/4" x	Α	F-1	14-lead FP (1/4" x 1/4")
D F-2 14-lead FP (1/4" x 3/8") E D-2 16-lead DIP (1/4" x 7/8") F F-5 16-lead FP (1/4" x 3/8") G A-1 8-lead can H F-4 10-lead FP (1/4" x 1/4") I A-2 10-lead can J D-3 24-lead DIP (1/4" x 1/4") K F-6 24-lead FP (3/8" x 5/8") NONE NONE M A-3 12-lead can N NONE NONE P D-4 8-lead DIP (1/4" x 3/8") Q D-5 40-lead DIP (1/4" x 3/8") R D-8 20-lead DIP (1/4" x 1 1/16") R D-8 20-lead FP (1/4" x 1/16") T NONE NONE U C-2 20 terminal leadless chip carrier V D-6 18-lead DIP (0.300" x 1")	В	F-3	14-lead FP (3/16" x 1/4")
E D-2 16-lead DIP (1/4" x 7/8") F F-5 16-lead FP (1/4" x 3/8") G A-1 8-lead can H F-4 10-lead FP (1/4" x 1/4") I A-2 10-lead can J D-3 24-lead DIP (1/4" x 1 1/4") K F-6 24-lead FP (3/8" x 5/8") NONE NONE M A-3 12-lead can N NONE NONE P D-4 8-lead DIP (1/4" x 3/8") Q D-5 40-lead DIP (9/16" x 2 1/16") R D-8 20-lead DIP (1/4" x 1 1/16") S F-9 20-lead FP (1/4" x 1/2") T NONE NONE U C-2 20 terminal leadless chip carrier V D-6 18-lead DIP (0.300" x 1")	C	D-1	14-lead DIP (1/4" x 3/4")
F F-5	D	F-2	14-lead FP (1/4" x 3/8")
G A-1 B-lead can 10-lead FP (1/4" x 1/4") I A-2 10-lead can 24-lead DIP (1/4" x 1 1/4") K F-6 24-lead DIP (1/4" x 5/8") NONE NONE M A-3 12-lead can NONE P D-4 B-lead DIP (1/4" x 3/8") Q D-5 40-lead DIP (9/16" x 2 1/16") R D-8 20-lead DIP (1/4" x 1 1/16") S F-9 20-lead FP (1/4" x 1/2") T NONE NONE U C-2 20 terminal leadless chip carrier V D-6 18-lead DIP (0.300" x 1")	E	D-2	16-lead DIP (1/4" x 7/8")
H F-4 10-lead FP (1/4" x 1/4") I A-2 10-lead can J D-3 24-lead DIP (1/4" x 1 1/4") K F-6 24-lead FP (3/8" x 5/8") NONE NONE M A-3 12-lead can N NONE NONE P D-4 8-lead DIP (1/4" x 3/8") Q D-5 40-lead DIP (9/16" x 2 1/16") R D-8 20-lead DIP (1/4" x 1 1/16") S F-9 20-lead FP (1/4" x 1/2") NONE U C-2 20 terminal leadless chip carrier V D-6 18-lead DIP (0.300" x 1")	F	F-5	16-lead FP (1/4" x 3/8")
I	G	A-1	8-lead can
J D-3 24-lead DIP (1/4" x 1 1/4") K F-6 24-lead FP (3/8" x 5/8") NONE NONE M A-3 12-lead can N NONE NONE P D-4 8-lead DIP (1/4" x 3/8") Q D-5 40-lead DIP (9/16" x 2 1/16") R D-8 20-lead DIP (1/4" x 1 1/16") S F-9 20-lead FP (1/4" x 1/2") NONE NONE U C-2 20 terminal leadless chip carrier V D-6 18-lead DIP (0.300" x 1")	Н	F-4	10-lead FP (1/4" x 1/4")
K F-6 L NONE NONE NONE M A-3 12-lead can NONE NONE P D-4 8-lead DIP (1/4" x 3/8") Q D-5 40-lead DIP (9/16" x 2 1/16") R D-8 20-lead DIP (1/4" x 1 1/16") S F-9 20-lead FP (1/4" x 1/2") T NONE NONE U C-2 20 terminal leadless chip carrier V D-6 18-lead DIP (0.300" x 1")	1	A-2	10-lead can
L NONE NONE M A-3 12-lead can N NONE P D-4 8-lead DIP (1/4" x 3/8") Q D-5 40-lead DIP (9/16" x 2 1/16") R D-8 20-lead DIP (1/4" x 1 1/16") S F-9 20-lead FP (1/4" x 1/2") T NONE NONE U C-2 20 terminal leadless chip carrier V D-6 18-lead DIP (0.300" x 1")	J	D-3	24-lead DIP (1/4" x 1 1/4")
M A-3 NONE NONE NONE P D-4 8-lead DIP (1/4" x 3/8") Q D-5 40-lead DIP (9/16" x 2 1/16") R D-8 20-lead DIP (1/4" x 1 1/16") T NONE NONE U C-2 20 terminal leadless chip carrier V D-6 18-lead DIP (0.300" x 1")	K	F-6	24-lead FP (3/8" x 5/8")
N NONE NONE P D-4 8-lead DIP (1/4" x 3/8") Q D-5 40-lead DIP (9/16" x 2 1/16") R D-8 20-lead DIP (1/4" x 1 1/16") S F-9 20-lead FP (1/4" x 1/2") NONE NONE U C-2 20 terminal leadless chip carrier V D-6 18-lead DIP (0.300" x 1")	L	NONE	NONE
P D-4 8-lead DIP (1/4" x 3/8") Q D-5 40-lead DIP (9/16" x 2 1/16") R D-8 20-lead DIP (1/4" x 1 1/16") T NONE NONE U C-2 20 terminal leadless chip carrier V D-6 18-lead DIP (0.300" x 1")	M	A-3	12-lead can
Q D-5 40-lead DIP (9/16" x 2 1/16") R D-8 20-lead DIP (1/4" x 1 1/16") S F-9 20-lead FP (1/4" x 1/2") T NONE NONE U C-2 20 terminal leadless chip carrier V D-6 18-lead DIP (0.300" x 1")	N	NONE	NONE
R D-8 20-lead DIP (1/4" x 1 1/16"). S F-9 20-lead FP (1/4" x 1/2") T NONE NONE U C-2 20 terminal leadless chip carrier V D-6 18-lead DIP (0.300" x 1")	P	D-4	8-lead DIP (1/4" x 3/8")
S F-9 20-lead FP (1/4" x 1/2") T NONE NONE U C-2 20 terminal leadless chip carrier V D-6 18-lead DIP (0.300" x 1")	Q	D-5	40-lead DIP (9/16" x 2 1/16")
T NONE NONE U C-2 20 terminal leadless chip carrier V D-6 18-lead DIP (0.300" x 1")	R	D-8	20-lead DIP (1/4" x 1 1/16")
U C-2 20 terminal leadless chip carrier V D-6 18-lead DIP (0.300" x 1")	S	F-9	20-lead FP (1/4" x 1/2")
carrier V D-6 18-lead DIP (0.300" x 1")	T	NONE	NONE
10 1000 Dil (0.000 X 1 /	U	C-2	
W D-7 22-lead DIP (0.400" x 1.1")	V	D-6	18-lead DIP (0.300" x 1")
	W	D-7	22-lead DIP (0.400" x 1.1")
			specified in the individual detail
Y outlines which are specified in the individual detail	Z	specifications.	

Features:

- Manufactured in a government-approved facility.
- 2. G.S.I. (Government Source Inspection)

Example of MIL-M-38510 JAN-Qualified markings

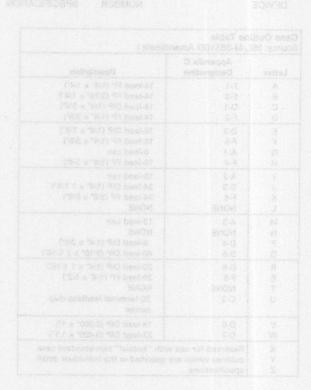
ORDER: JM38510/00104BCB MARKING: JM38510/00104BCB

Lead Fini	sh Table
	A or B Per MIL-M-38510 with hot er dip
В — Туре	A or B Per MIL-M-38510 with tin plate
C — Type	A or B Per MIL-M-38510 with gold
X — Any only	of the above, for ordering purposes

JAN Qualified MECL Devices

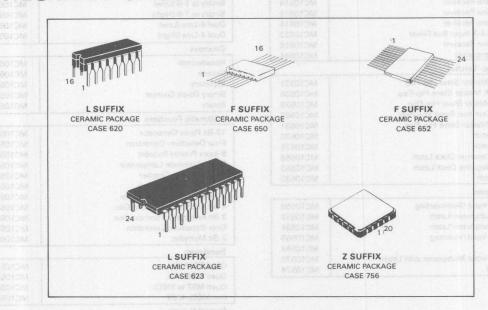
Function and MC10500 Equivalent	MIL-M-38510 Device*
uad OR/NOR Gate (MC10501)	MIL-M-38510/06001
uad 2-Input NOR Gate (MC10502)	MIL-M-38510/06002
ple 2-3-2 OR/NOR Gate (MC10505)	MIL-M-38510/06003
ple 4-3-3 NOR Gate (MC10506)	MIL-M-38510/06004
ple 2-Input Exclusive OR/Exclusive NOR Gate (MC10507)	MIL-M-38510/06005
ual 4-5 Input OR/NOR Gate (MC10509)	MIL-M-38510/06006
uad 2-Input AND (MC10504)	MIL-M-38510/06201
ex AND (MC10597)	MIL-M-38510/06202
and MTTL to MECL Translator (MC10524)	MIL-M-38510/06301
and MECL to MTTL Translator (MC10525)	MIL-M-38510/06302
ial D Flip-Flop (MC10531)	MIL-M-38510/06001
al D Flip-Flop (MC10631)	MIL-M-38510/06002
x D Flip-Flop (MC10576)	MIL-M-38510/06003
ial J-K Flip-Flop (MC10535)	MIL-M-38510/06007

^{*}JAN devices must have complete part number description.



MECL 10K INTEGRATED CIRCUITS

MC10,500/10,600 Series (-55 to +125°C)



Function Selection — (-55°C to +125°C)

NOR Gates

Quad 2-Input Gate Strobe

Quad 2-Input Gate	MC10502
Triple 4-3-3 Input Gate	MC10506
Dual 3-Input 3-Output Gate	MC10611
OR Gates	
Quad 2-Input Gate	MC10503
Dual 3-Input 3-Output Gate	MC10610
AND Gates	
Quad 2-Input Gate	MC10504
Hex Gate	MC10597
Complex	
Quad OR/NOR Gate	MC10501
Triple 2-3-2 Input OR/NOR Gate	MC10505
Dual 4-5 Input OR/NOR Gate	MC10509
Dual 3-Input 3-Output OR/NOR Gate	MC10612
Exclusive Triple 2-Input Gate	MC10507
Exclusive Quad 2-Input Gate	MC10513
Complex OR/AND Gate Function	MC10517
Complex OR/AND Gate Function	MC10518
Complex OR/AND Gate Function	MC10519
Complex OR/AND Gate Function	MC10521

MC10500

MC10595

All devices have standard case 620 or 650.

Buffers/Inverters

Hex Inverter/Buffer

The second secon		Decoders	SATIAL
Triple Line Receiver Quad Line Receiver Triple Line Receiver Triple 4-3-3-Input Bus Driver	MC10514 MC10515 MC10516 MC10523	Binary to 1-8 (Low) Binary to 1-8 (High) Dual 4-Line (Low) Dual 4-Line (High)	MC10561 MC10562 MC10571 MC10572
Triple Line Receiver Dual Transceiver	MC10616 MC10594	Counters	
Flip-Flop/Latches	MC10594	Hexadecimal	MC10536
Dual D Master Slave Flip-Flop Dual J-K Master Slave Flip-Flop Hex D Master Slave Flip-Flop	MC10531 MC10535 MC10576	Decade Biquinary Binary Down Counter Binary	MC10537 MC10538 MC10554 MC10578
Hex D Common Reset Flip-Flop	MC10586	Arithmetic Functions	
ad Latch	MC10631 MC10533 MC10575 MC10568 MC10553 MC10530	12-Bit Parity Generator Error Detection/Correction 8-Input Priority Encoder 5-Bit Magnitude Comparator 9 + 2 Bit Parity Checker	MC10560 MC10563 MC10565 MC10566 MC10570
Multiplexer		Look Ahead Carry Block Dual 2-Bit Adder/Subtractor	MC10579 MC10580
Quad 2 Input/Noninverting Dual Multiplexer/Latch Dual Multiplexer/Latch Quad 2-Input/Inverting	MC10558 MC10532 MC10534 MC10559	4-Bit Arithmetic Function Gen. 2-Bit Arithmetic Function Gen. Error Detection/Correction 2-Bit Multiplier	MC10581 MC10582 MC10593 MC10687
8-Line	MC10564	Translators	
Quad 2-Input Multiplexer with Latch Dual 4-1	MC10573 MC10574	Quad TTL-MECL Quad MECL-TTL Quad MST to MECL Hex MECL-MST	MC10524 MC10525 MC10590 MC10591
		Special Function	
		4-Bit Shift Register	MC10541

^{*}Contact your Motorola sales office or Motorola distributor for details on availability of special packages.

All devices have standard case 620 or 650.

MC10500/10600 Series

The MC10500/10600 series is a military temperature range (-55°C to +125°C) version of the MC10100/10200 series. Much of the design information contained in the to the MC10500/10600 series. However, specified limits differ over the extended temperature range. The are specified driving loads of 100 ohms to -2.0 V.

MC10500/10600 series selector guide lists the device and case types available.

Table I defines the forcing functions and associated General Information Section of this book is applicable dc parameters at the operating temperature limits of the MC10500/10600 series. The dc parameters of Table I

Table I — MC10500/10600 Series Transfer Data for Temperature Variations

Forcing Function	Parameter	-55°C 1	25°C 1	125°C 1	Unit	
		MC10500 MC10600	MC10500 MC10600	MC10500 MC10600		
VIHmax	VOHmax VOHmin	- 0.880 - 1.080	-0.780 -0.930	- 0.630 - 0.825	Vdc	
VIHAmin	VOHAmin	- 1.100 - 1.255	- 0.950 - 1.105			
VILAmax	VOLAmax	- 1.510 - 1.635	-1.475 -1.400 -1.600 -1.525		Vdc	
V _{ILmin}	V _{OLmax} V _{OLmin}	- 1.655 - 1.920	- 1.620 - 1.545 - 1.850 - 1.820		Vdc	
V _{ILmin}	INLmin	0.5	0.5	0.3	μΑ	

NOTES: 1 MC10500, MC10600, and series specified driving 100 Ω to -2.0 V.

	- 1.635 - 1.635		